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Current-voltage analytical model and multiobjective optimization of design of a short channel gate-all-around-junctionless MOSFET

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Abstract

In this paper we investigate the optimized design of a short channel gate-all-around-junctionless (GAAJ) metal-oxide-semiconductor field-effect-transistor (MOSFET), including the source-drain extensions, by means of genetic algorithm solutions applied to a compact current-voltage analytical model. In fact, due to the complex device structure, it seems useful to exploit a metaheuristic-based approach to search the optimal combination of the fundamental geometrical and physical parameters that lead to an improved performance. Through this analysis, different parameter constraints are imposed for the calculation of specific objective functions. In particular, for a fixed gate-drain bias level, the task pursues the maximization of the drain current and cut-off frequency while limiting the short channel (SC) effects. The MOSFET series resistance is also evaluated in the transition region of the $I_d - V_{gs}$ characteristics which appear, however, strongly affected by SC effects. The accuracy of the model is verified by comparison with experimental data reported in literature.

Keywords: GAAJ MOSFET; short channel; drain current; series resistance; cut-off frequency.

1. Introduction

In modern power electronics, the continuous geometrical downscaling of the metal-oxide-semiconductor (MOS) structures is needful for the realization of high-performance MOS field-effect-transistors (FETs) to be used in both analog and digital fields. However, the ultra large scale of integration for MOSFET technology leads to undesired short channel (SC) effects, which penalize the device performance mainly in terms of carrier saturation velocity, leakage current, and power dissipation. To overcome these technological issues, different silicon (Si)-based FETs have been suggested and characterized in literature [1-6]. In particular, gate-all-around-junctionless (GAAJ) MOSFETs have been recognized as attractive structures for high performance devices by considering their improved carrier transport mechanisms, outstanding scalability, and leakage current (gate voltage) controllability [7-10]. Moreover, GAAS structures, avoiding the realization of abrupt p-n junctions, are in principle well suited to increase the device immunity to SC effects and therefore the MOSFET current capabilities [11-14]. However, the design of a GAAS MOSFET, which can involve also pin and/or Schottky structures, still requires the deployment of rigorous modelling efforts based either on empirical computations or analytical (numerical) simulations to meet specific application constraints [15-22].

In this paper, the optimized design of a SC GAAJ MOSFET including source-drain extensions is investigated by combining a compact current-voltage analytical model and a multiobjective genetic algorithm (MGA) for the

calculation of the geometrical and physical parameters that improve the device performance. In particular, starting from a reference device, the obtained results provide significant improvements in terms of important figures of merit (FOM) such as the drive current, series resistance, and cut-off frequency. The theoretical background for the computation methodology is also presented.

The analytical model taken into account has been validated with numerical simulations in a recent manuscript of ours where preliminary results on different GAAJ structures have been investigated and the need of an exhaustive design optimization approach has been introduced [23].

2. GAAJ MOSFET structure

A schematic 2D cross-sectional view of the cylindrical GAAJ MOSFET considered in this work is shown in figure 1 along with the notation adopted for the fundamental geometrical parameters.

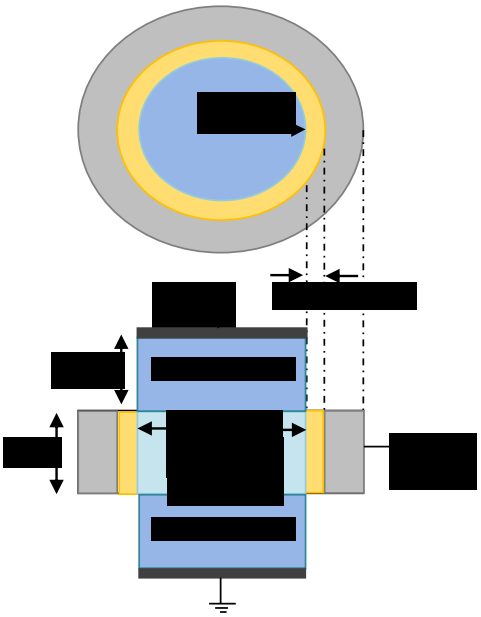

Figure 1. Schematic 2D cross-sectional view of the considered GAAJ MOSFET.

In more detail, t_{ox} is the oxide thickness, R is the channel radius, L is the channel length (gate length), and L_{ext} is the extension length of the drain (source) region. In addition, we can note that the source and drain extensions are assumed with a doping level higher than that of the channel-body region. In fact, the use of a uniform doping concentration limits the drain current introducing a severe series resistance related to the extension regions [24]. The device reference parameters used as entry data for modelling are listed in Table 1.

The doping concentrations are in accordance with theoretical and experimental results reported in literature [24-26]. A radius in the inferior limit of 7.5 nm is assumed to prevent quantum phenomena as suggested in [27] and references therein. Also, lower values of R tend to increase the SC effects.

Table 1. GAAJ MOSFET reference parameters.

Channel radius, R (nm)	7.5
Silicon oxide thickness, t_{ox} (nm)	2
Metal work function, Φ_m (eV)	5.27
Channel length, L (nm)	30
N-type channel doping, N_d (cm^{-3})	1×10^{19}
Extension length, L_{ext} (nm)	10
N-type extension doping, N_{dext} (cm^{-3})	5×10^{19}

3. Current-voltage analytical model

Starting from Poisson equation in cylindrical coordinates, the GAAJ MOSFET drain current equation in on-state with grounded source can be expressed as follows [14]:

$$I_d = 2\pi \frac{R\,\mu_n\,V_T}{L}\left(F(V_i) - F(V_i + V_{ds})\right) \tag{1}$$

where, labelled V_i the built-in potential at the source/channel junction ($V_i = V_T \ln(N_{dext}/n_i)$ [27,28]) and V_{ds} the applied bias at the drain contact, the terms $F(V)$ are in the form [28]

$$F(V) = \frac{(Q_{cp} + C_{OX}V_T)\,Q_{mob}(V)^2}{2Q_{cp}C_{OX}V_T} + 2Q_{mob}(V) - CQ_{mob}(V)\ln\left[1+\exp\left(\frac{Q_{mob}(V)-Q_{fix}}{2CQ_{cp}}\right)\right] + Q_{fix}\ln\frac{Q_{mob}(V)-Q_{fix}}{2Q_{cp}\exp\left(\frac{Q_{mob}(V)-Q_{fix}}{2Q_{cp}}-1\right)} \tag{2}$$

Here, V_T is the thermal voltage, $Q_{fix} = q\,N_d\,R/2$ refers to the fixed charges in the channel region, $C_{OX} = \varepsilon_{OX}/R\ln(1+t_{OX}/R)$, $Q_{cp} = 2\varepsilon_0\varepsilon_{Si}V_T/R$, and the mobile charge $Q_{mob}(V)$ is given by an accurate expression for SC devices, i.e.

$$Q_{mob}(V) = \frac{Q_{cp}C_{OX}V_T}{(Q_{cp}+C_{OX}V_T)}LW\left[\frac{(Q_{cp}+C_{OX}V_T)\,Q_{fix}Q_{cp}}{Q_{cp}C_{OX}V_T}\frac{\exp\left(\frac{Q_m^0-Q_{fix}}{Q_{cp}}\right)-1}{Q_m^0-Q_{fix}}\exp\left(v+\frac{Q_{fix}}{f\,Q_{cp}}\right)\right] \tag{3}$$

where LW stands for the Lambert function approximation [29]

$$LW(z) = \ln(1+z)\left(1-\frac{\ln(1+\ln(1+z))}{2+\ln(1+z)}\right), \tag{4}$$

$f = 1 + \frac{Q_m^0}{5Q_{fix}} \exp(-\frac{Q_m^0}{Q_{fix}})$, and $v = (V_{gs} + V_{fb} + Q_{cp} / C_{OX} - V) / V_T$ is a term that contains all the voltage dependences. In particular, $V_{fb} = \Phi_{ms} + V_T \ln(N_d / n_i)$ is the flat-band voltage depending on the channel doping concentration, the intrinsic carrier concentration (n_i), and the difference between the metal gate and semiconductor work-function, namely $\Phi_{ms} = \Phi_m - \Phi_s = \Phi_m - (\chi + E_g / 2q)$ [14,30] where χ and E_g are the electron affinity and bandgap of Si, respectively. Finally, in (3), Q_m^0 is given by [14]

$$Q_m^0 = C_{OX} V_T \, LW \left\{ \frac{Q_{fix} Q_{cp}}{C_{OX} V_T} \frac{\left[1 - \exp\left(\frac{Q_{fix} - Q_{m1}}{Q_{cp}} \right) \right]}{Q_{m1} - Q_{fix}} \right\} \exp(v) \tag{5}$$

where

$$Q_{m1} = \frac{Q_{cp} C_{OX} V_T}{(Q_{cp} + C_{OX} V_T)} LW \left[\frac{(Q_{cp} + C_{OX} V_T) Q_{fix} Q_{cp}}{Q_{cp} C_{OX} V_T} \frac{\exp\left(\frac{Q_{fix} - Q_{m2}}{Q_{cp}} \right)}{Q_{m2} - Q_{fix}} \exp(v) \right], \tag{6}$$

$$Q_{m2} = 2 C_{OX} V_T \, LW \left[\frac{\sqrt{Q_{fix} Q_{cp}}}{C_{OX} V_T} \exp(v/2) \right]. \tag{7}$$

The doping dependent carrier mobility in (1) is modelled by the Caughey-Thomas equation at room temperature:

$$\mu_n = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N_d}{N_{crit}} \right)^{\alpha}} \tag{8}$$

where N_{crit} is the doping concentration reference parameter at which the mobility is halfway between its maximum and its minimum value [31,32]. For a Si-based device, we have $\mu_{\max}$ = 1400 cm^2/Vs, $\mu_{\min}$ = 688 cm^2/Vs, α = 0.71, and $N_{crit} = 1 \times 10^{18}$ cm^3. In addition, to account for the mobility degradation in a SC device due to the carrier saturation velocity ($v_{sat} = 1 \times 10^7$ cm/s), an effective carrier mobility μ_{eff} is assumed as follows [33,34]

$$\mu_{eff} = \frac{\mu_n}{\left[1 + \left(\frac{\mu_n V_{deff}}{L v_{sat}} \right)^{\beta} \right]^{\frac{1}{\beta}}} \tag{9}$$

where β = 2 for electrons, and V_{deff} is the effective drain voltage which saturates the drain current at a value V_{dsat} calculated as [28]:

$$V_{dsat} = \frac{V_x}{\frac{V_x}{V_{crit}} + 1} \tag{10}$$

by assuming

$$V_x = \frac{Q_{mob}(0)}{C_{OX}} + \frac{V_{crit}}{\frac{V_{crit}}{2V_T} - 1} \tag{11}$$

$$V_{crit} = 2\frac{v_{sat}}{\mu_n} L \ . \tag{12}$$

In accordance with [28], V_{deff} is in the form:

$$V_{deff} = V_{dsat} - V_{dsat} \frac{\ln\left\{1 + \exp\left[B\left(1 - \frac{V_{ds}}{V_{dsat}}\right)\right]\right\}}{\ln\left(1 + \exp B\right)} \tag{13}$$

where *B* is a smoothness parameter equal to 3 for SC devices.

4. Theoretical basis for MGAs

Multiobjective genetic algorithms are a flexible approach for the optimal solution of constrained and unconstrained problems where different objective functions must be evaluated simultaneously [35-39]. These techniques allow the selection of a suitable set of solutions according to the problem application field and provide a simple implementation also dealing with a huge quantity of information. Genetic algorithms take their origin from natural evolution of species. In other words, starting from an initial population, they randomly select individuals and create new generations called children. This procedure is repeated along for different generations to meet the stopping criteria that produce the optimal solution. A simplified flowchart for MGAs is shown in figure 2. Selection, crossover, and mutation are the fundamental operations imposed on a certain generation to allow the procedure to evolve.

Using the MGA terminology, the initial population corresponds to the GAAJ MOSFET geometrical and physical parameters, such as the oxide thickness, channel radius, channel length, and doping concentrations, which play a key role in determining the effective device performance.

Further details about the MGA approach and the simulation models for MOSFETs are provided in recent author manuscripts [41-44].

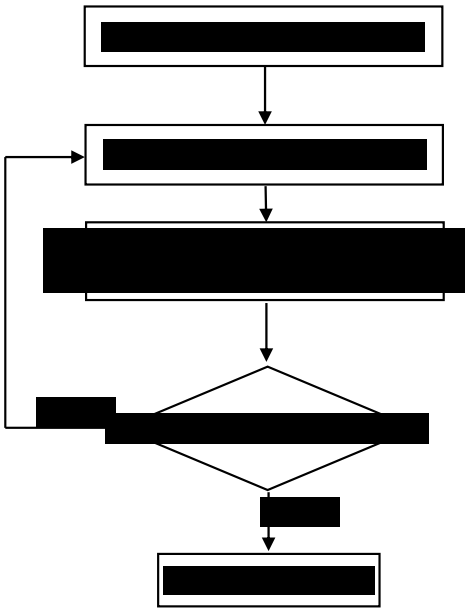

Figure 2. Flowchart for MGA.

5. Results and discussion

5.1 Reference device

For the GAAJ MOSFET described in Table 1, the I_d-V_{gs} curves calculated at two different drain voltages (i.e., V_{ds} = 1 V and V_{ds} = 0.05 V) are shown in figure 3. In accordance with [24], the device is supposed to work at V_{gs} < 2 V to avoid starting an overestimation of I_d by neglecting the anomalous distributions of the potential in the MOSFET active regions for high gate voltages.

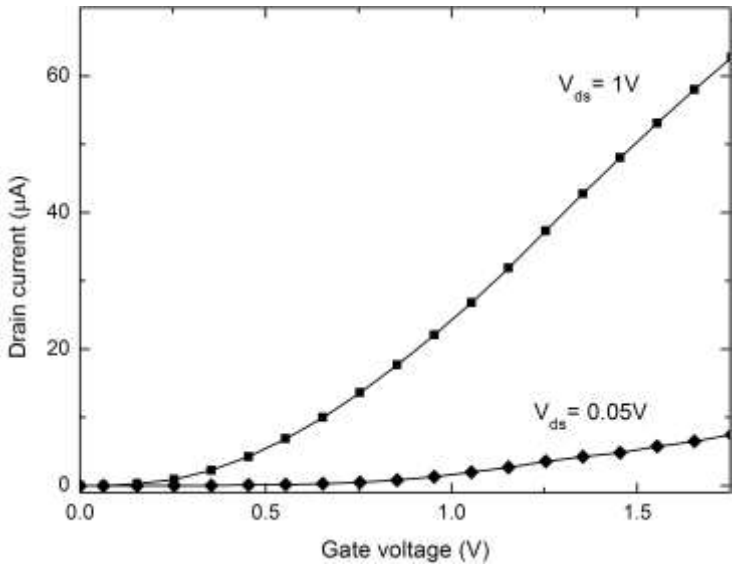

Figure 3. I_d-V_{gs} curves for the GAAJ MOSFET in Table 1.

As we can see, above the threshold voltage, the drain current increase is strongly limited by the combined effects

of the device series resistance and carrier saturation velocity in the channel region. The I_d-V_{ds} characteristics for different values of V_{gs} are plotted in figure 4.

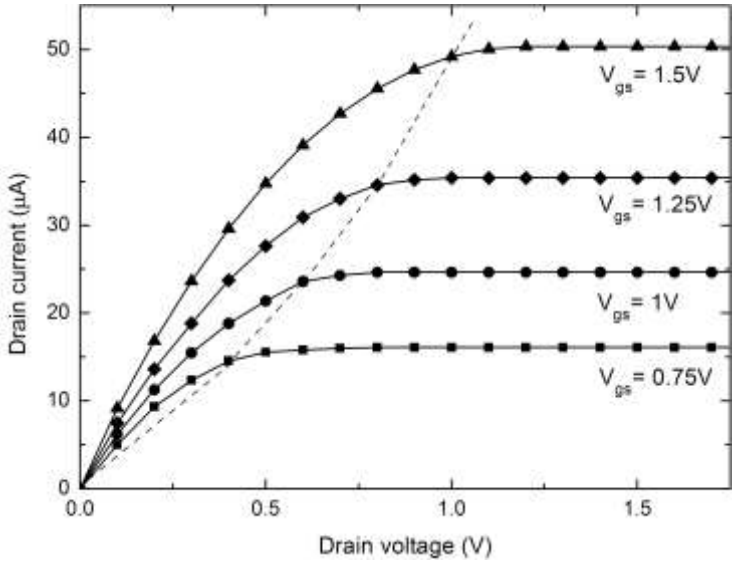

Figure 4. I_d-V_{ds} curves for the GAAJ MOSFET in Table 1.

In figure 4, the dashed line marks the transition region determined by the carrier saturation velocity. For instance, for V_{gs} = 1.5 V and V_{ds} = 1 V the drain current is close to the saturation value of 50 μA, which corresponds to a series resistance on the order of 3.53 Ω×μm^2. The series resistance behaviour as a function of V_{gs} in the V_{ds} transition region is shown in in figure 5. This behaviour mainly depends on the effective device length (i.e., L+2L_{ext}) and doping concentration in the drain and source extensions.

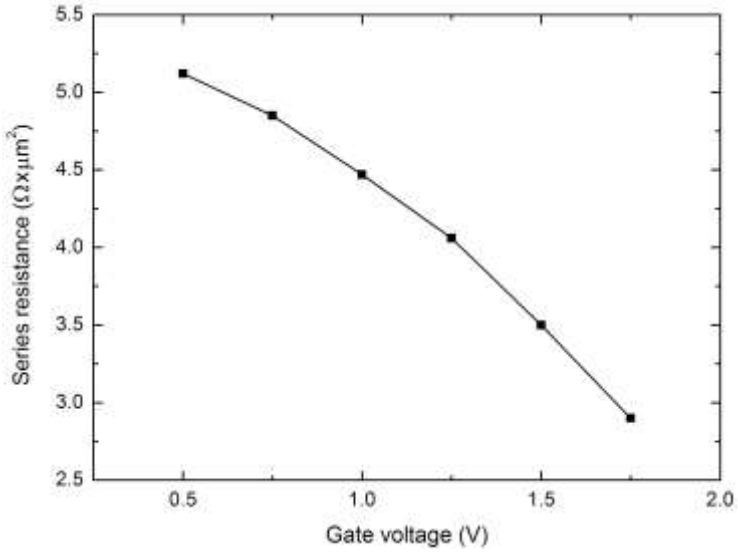

Figure 5. Series resistance behaviour as a function of V_{gs} in the transition region of the I_d - V_{ds} characteristics.

The transconductance is another important FOM that determines the ability of the device to amplify a signal. It is

calculated by the first derivative of the drain current, i.e. $g_m = \partial I_{ds} / \partial V_{gs}$. The g_m curve as a function of V_{gs} for V_{ds} = 1 V and V_{ds} = 0.05 V (deep triode region) is shown in figure 6.

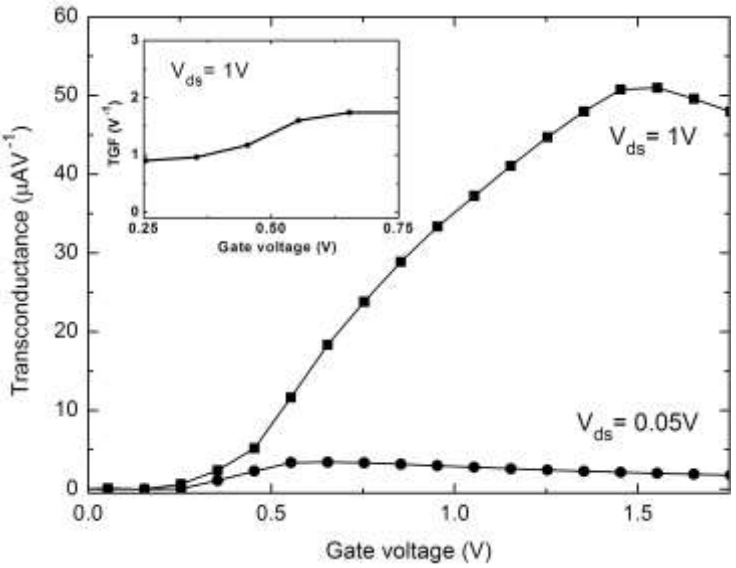

Figure 6. Transconductance characteristics for the GAAJ MOSFET in Table 1. The inset shows the transconductance generation factor (TGF) around the threshold voltage for V_{ds} = 1 V .

High values of g_m can be achieved when V_{ds} rises and V_{gs} is firmly above the device threshold voltage ($V_{gs} \geq$ 0.3 V for V_{ds} = 1 V). A g_m peak close to 51 μAV^{-1} is calculated for V_{ds} = 1 V and V_{gs} = 1.5 V. This value of g_m corresponds to a cut-off frequency of 220 GHz, estimated with the standard expression

$$f_c = \frac{g_m}{2\pi\ C_G} \tag{14}$$

assuming, for the sake of simplicity, the total amount of the input capacitance C_G equal to C_{OX}. In fact, although C_G is a term strictly dependent on the bias level, for the considered operating voltages V_{gs} = 1.5 V and V_{ds} = 1V, this appears as a reasonable approximation. However, additional capacitance contributions neglected in this first-level analysis could reduce the value of f_c and therefore it has to be considered as an upper limit for the device.

Another significant parameter is the transconductance generation factor (TGF) which aids to fix the role of the drain current in determining g_m. In fact, TGF is defined as the ratio g_m/I_d and it can be evaluated starting from the weak inversion regime, namely for a V_{gs} around the threshold voltage, as shown in the inset of figure 6 for 0.25V≤ V_{gs} ≤0.75V and V_{ds} = 1 V. In particular, we TGF values are on the order of 1 V^{-1} confirming that the proposed MOSFET could operate efficiently at low supply voltages.

5.2 Design optimization

The optimization of the GAAJ structure is a complex task due to the interrelated geometrical and physical parameters that influence the device performance. A systematic investigation aimed to find the optimal design parameters can be made by using the MGA approach introduced previously. In more details, in this work the MGA-based optimization framework deals with the statement of three objective functions, namely the drain

current, the cut-off frequency, and the subthreshold slope (*SS*), which are in the form of $I_d(X)$, $f_c(X)$, and $SS(X)$ where $X = (R, L, L_{ext}, t_{ox}, \Phi_m, N_d, N_{dext}, V_{gs}, V_{ds})$ is a vector of device parameters. Therefore, for each fixed gate-drain bias level, the task is related to the following criteria: maximize the drain current and cut-off frequency while minimizing the *SS* difference calculated with respect to the ideal value of 60 mV/dec in order to limit the SC effects. Proper constraints that define each parameter within a specific range of values are imposed during the computations as summarized in Table 2.

Table 2. Range of values in defining the vector *X*.

R (nm)	7 - 14
L (nm)	20 - 30
L_{ext} (nm)	8.5 - 10
t_{ox} (nm)	2 - 4
Φ_m (eV)	4.6 - 5.27
N_d (cm^{-3})	1×10^{18} - 5×10^{19}
N_{dext} (cm^{-3})	1×10^{19} - 1×10^{20}
V_{gs} (V)	0 - 1.75
V_{ds} (V)	0 - 1

Referring to the MGA flowchart in figure 2, we can state that the number of variables is 9 (dimension of *X*), and the assumed population size is 100. Finally, for evolving during consecutive generations the genetic operations are tournament-type selection, constraint dependent crossover, and scattered mutation. In addition, to optimize the procedure computational time the weighted sum approach is used in order to incorporate the different objective functions in a mono-objective function given by

$$F(X) = w_1 f_c + w_2 I_d + w_3 SS \tag{15}$$

where the optimal solution is calculated setting the no-preference method for the weighting factors, i.e. $w_1 = w_2 = w_3 = 0.333$. The behaviour of $F(X)$ as a function of the evolving generations is shown in figure 7.

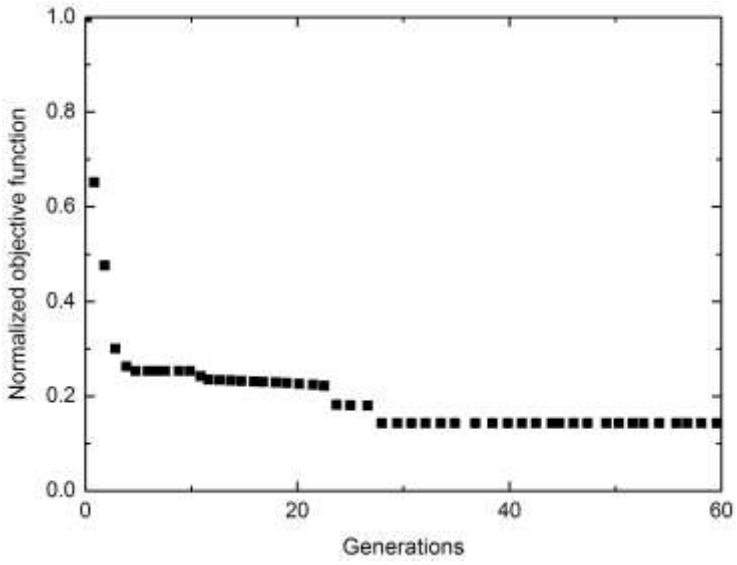

Figure 7. $F(X)$ behaviour as a function of the evolving generations.

The convergence occurs in the 26th generation requiring a computational time of about 15 min by using an updated personal computer. Then, the achieved fitness function corresponds to the optimal solution that provides the best device performance.

The optimized design of the GAAJ MOSFET and the extracted SC and FOM parameters are summarized in Table 3. Here, the results of the reference device in Table 1 are also reported for comparison. In particular, the value of the drain induced barrier lowering (DIBL) is calculated as ratio of the threshold voltage reduction to the applied change in V_{ds} assuming V_{ds} = 0.05 V and V_{ds} = 1 V, respectively. Similarly, the subthreshold slope is defined as the change in V_{gs} that must be applied in the subthreshold regime to determine a drain current increase of one decade starting from the off-state current calculated for V_{gs} = 0 V. The obtained value of *SS* is in the limit of 80 mV/dec and it is consistent with literature data [24,45].

Table 3. MGA-based optimization.

	Reference device	**Optimized device**
Design parameters		
Channel radius, R (nm)	7.5	11
Silicon oxide thickness, t_{ox} (nm)	2	2
Metal work function, Φ_m (eV)	5.27	4.6
Channel length, L (nm)	30	20
N-type channel doping, N_d (cm^{-3})	1×10^{19}	2.5×10^{18}
Extension length, L_{ext} (nm)	10	8.6
N-type extension doping, N_{dext} (cm^{-3})	5×10^{19}	7.5×10^{19}
SC effects @ V_{ds} = 1 V		
Threshold voltage (V)	0.3	0.25
Off-state current density ($\mu A/\mu m^2$)	2.26	2.63
DIBL (mV/V)	315	336
Subthreshold slope (mV/dec)	75	79
FOM @ V_{gs} = 1.5 V and V_{ds} = 1 V		
On-state current density ($mA/\mu m^2$)	283	342
Series resistance ($\Omega\times\mu m^2$)	3.53	2.92
Cut-off frequency (GHz)	220	337

From Table 3, we can note that the optimized design includes highly doped source-drain extensions and a lower channel doping concentration. Also, the overall MOSFET length is scaled of 12.8 nm, namely 10 nm in the channel region and 1.4 nm in each extension. In principle, the use of highly doped extensions is a technologically feasible approach that requires only an appropriate ion implantation process. At the same time, for the mature technology of Si, the transistor scaling is well addressed to nanoscale devices. Finally, whereas the reference value of the work function is related to the conventional polysilicon, the optimized Φ_m = 4.6 eV could be obtained by using chromium as gate material [46].

The comparison between the drain current variation with respect to V_{gs} for the reference device and the MGA-based design is shown in figure 8. Here, three experimental points extracted from the current-voltage

characteristics measured in [25] for a GAAJ transistor structure, which is almost similar to the reference device are also reported. The experimental MOSFET presents a channel thickness of 6 nm, a channel length of 50 nm, a oxide thickness of 13 nm, and a uniform donor doping concentration of 1×10^{19} cm^{-3}. It was characterized for V_{gs} up to 1 V showing a comparable threshold voltage level.

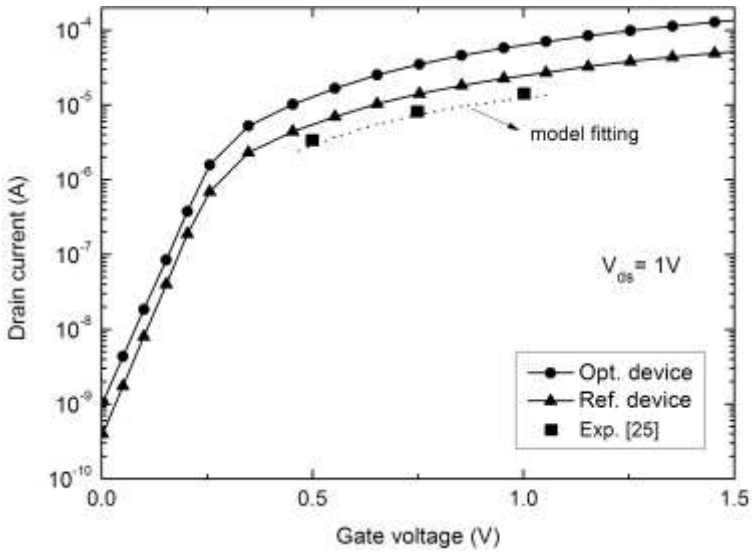

Figure 8. Variation of I_d with respect to V_{gs} for the reference device and the MGA-based design.

The consistency of the results in figure 8 validates the prediction capabilities of the used analytical model. Also, the optimized GAAJ MOSFET exhibits a drain current higher than that of the reference device in the whole explored V_{gs} range. In particular, it performs 17% and 54% improvement in series resistance and cut-off frequency, respectively. At the same time, the increase of the SC effects appears rather limited. The proposed optimization technique could be therefore considered as an attractive design strategy.

6. Conclusion

A genetic algorithm approach for the design optimization of a GAAJ MOSFET has been presented supporting the calculations of a compact current-voltage analytical model. In fact, fundamental design parameters such as the channel radius, channel length, donor doping concentrations, and oxide characteristics are interrelated geometrical and physical parameters that influence the effective device performance. The drain current, cut-off frequency, and subthreshold slope have been assumed as fitness functions. The MOSFET series resistance has been also calculated in the transition region of the I_d -V_{gs} curves. The optimized device achieves a cut-off frequency of 337 GHz and a series resistance of 2.92 $\Omega\times\mu m^2$. By comparing these results with the performance of the reference structure, we can state that the suggested design strategy appears as an attractive practical tool for the design of high-performance GAAJ MOSFETs, offering a reasonable computational time and low complexity. These transistors could be considered well suited for modern radio frequency systems such as signal mixers operating in the gigahertz regime, and frequency multipliers that are widely used in digital/analog communications as well as radio astronomy and terahertz sensing applications.

References

[1] Yao J, Li J, Luo K, Yu J, Zhang Q, Hou Z, Gu J, Yang W, Wu Z, Yin H, Wang W. Physical insights on quantum confinement and carrier mobility in Si, $Si_{0.45}Ge_{0.55}$, Ge gate-all-around NSFET for 5 nm technology node. IEEE J. Electron Dev. 2018; 6:841-848.

[2] Nirmal D, Kumar PV, Joy D, Jebalin BK, Kumar NM. Nanoscale tri-gate MOSFET for ultra low power applications using high-k dielectrics. In Proc. IEEE 5th Int. Conf. on Nanoelectronics -INEC, 2013; 12-19.

[3] Pezzimenti F, Bellone S, Della Corte FG, Nipoti R. Steady-state analysis of a normally-off 4H-SiC trench bipolar-mode FET. Mater. Sci. Forum 2013; 740:942-945.

[4] Kranti A, Armstrong GA. Design and optimization of FinFETs for ultra-low-voltage analog applications. IEEE Trans. Electron Dev. 2007; 54:3308-3316.

[5] Pezzimenti F, Della Corte FG. Static and transient analysis of a 4H-SiC trench Bipolar Mode FET with normally-off characteristics. In Proc. IEEE Int. Semiconductor Conf. – CAS, 2012; 347-350.

[6] Della Corte FG, Pezzimenti F, Bellone S, Nipoti R. Numerical simulations of a 4H-SiC BMFET power transistor with normally-off characteristics. Mater. Sci. Forum 2011; 679:621-624.

[7] Djeffal F, Ghoggali Z, Dibi Z, Lakhdar N. Analytical analysis of nanoscale multiple gate MOSFETs including effects of hot-carrier induced interface charges. Microelectron. Reliab. 2009; 49:377-381.

[8] Ghosh D, Kranti A. Impact of channel doping and spacer architecture on Analog/RF performance for low power junctionless MOSFETs. Semicond. Sci. Tech. 2014; 30:1-11.

[9] Liu TY, Pan FM, Sheu JT. Characteristics of gate-all-around junctionless polysilicon nanowire transistors with twin 20-nm gates. IEEE J. Electron Devi. 2015; 3:405-409.

[10] Djeffal F, Lakhdar N, Yousfi A. An optimized design of 10-nm-scale dual-material surrounded gate MOSFETs for digital circuit applications. Physica E 2011; 44:339-344.

[11] Dubey S, Tiwari PK, Jit S. On-current modeling of short channel double gate (DG) MOSFETs with a vertical Gaussian - like doping profile. J. Semicond. 2013; 34:1-8.

[12] Su CJ, Tsai TI, Liou YL, Lin ZM, Lin HC, Chao TS. Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels. IEEE Electr. Device L. 2011; 32:521-523.

[13] Jin X, Liu X, Wu M, Chuai R, Lee JH, Lee JH. Modelling of the nanoscale channel length effect on the subthreshold characteristics of junctionless field-effect transistors with a symmetric double-gate structure. J. Phys. D Appl. Phys. 2012; 45:1-4.

[14] Lime F, Moldovan O, Iñiguez B. A compact explicit model for long-channel gate-all-around junctionless MOSFETs. Part I: dc characteristics. IEEE Trans. Electron Dev. 2014; 61:3036-3041.

[15] Ho CY, Chang YJ. Evaluation of Schottky barrier source/drain contact on gate-all-around polycrystalline silicon nanowire MOSFET. Mat. Sci. Semicon. Proc. 2017; 61:150-155.

[16] Zeghdar K, Dehimi L, Pezzimenti F, Rao S, Della Corte FG. Simulation and analysis of the current-voltage-temperature characteristics of Al/Ti/4H-SiC Schottky barrier diodes. Jpn. J. Appl. Phys. 2019; 58:014002.

[17] Bouzid F, Pezzimenti F, Dehimi L, Megherbi ML, Della Corte FG. Numerical simulations of the electrical transport characteristics of a Pt/n-GaN Schottky diode. Jpn. J. Appl. Phys. 2017; 56:094301.

[18] Megherbi ML, Pezzimenti F, Dehimi L, Saadoune A, Della Corte FG. Analysis of the Forward I–V Characteristics of Al-Implanted 4H-SiC p-i-n Diodes with Modeling of Recombination and Trapping Effects Due to Intrinsic and Doping-Induced Defect States. J. Electron. Mater. 2018; 47:1414–1420.

[19] Fritah A, Dehimi L, Pezzimenti F, Saadoune A, Abay B. Analysis of I–V–T Characteristics of Au/n-InP Schottky Barrier Diodes with Modeling of Nanometer-Sized Patches at Low Temperature. J. Electron Mater. 2019; 48:3692-3698.

[20] Megherbi ML, Pezzimenti F, Dehimi L, Rao S, Della Corte FG. Analysis of different forward current-voltage behaviours of Al implanted 4H-SiC vertical p-i-n diodes. Solid-State Electron. 2015; 109:12-16.

[21] Bellone S, Della Corte FG, Albanese LF, Pezzimenti F. An analytical model of the forward I-V characteristics of 4H-SiC p-i-n diodes valid for a wide range of temperature and current. IEEE T. Power Electr. 2011; 26:2835-2843.

[22] Duarte JP, Kim MS, Choi SJ, Choi YK. A compact model of quantum electron density at the subthreshold region for double-gate junctionless transistors. IEEE Trans. Electron Dev. 2012; 59:1008-1012.

[23] Yousfi A, Dibi Z, Aissi S, Bencherif H, Saidi L. RF/analog performances enhancement of short channel GAAJ MOSFET using source/drain extensions and metaheuristic optimization-based approach. J. Telecomm. Electron. Comp. Eng. 2018; 10:81-90.

[24] Cerdeira A, Ávila Herrera F, Cardoso Paz B, Estrada M, Pavanello MA. Role of the extensions in Double-Gate Junctionless MOSFETs in the drain current at high gate voltage. In Proc. IEEE 30th Symposium on Microelectronics Technology and Devices – SBMicro, 2015; 1-4.

[25] Choi SJ, Moon DI, Kim S, Duarte JP, Choi YK. Sensitivity of threshold voltage to nanowire width variation in junctionless transistors. IEEE Electron Device Letters 2011; 32:125-127.

[26] Parihar MS, Kranti A. Revisiting the doping requirement for low power junctionless MOSFETs. Semicond. Sci. Technol. 2014; 29:075006.
[27] Mokkapati S, Jaiswal N, Gupta M, Kranti A. Gate-All-Around Nanowire Junctionless Transistor-Based Hydrogen Gas Sensor. IEEE Sens. J. 2019; 19:4758-4764.
[28] Lime F, Ávila Herrera F, Cerdeira A, Iñiguez B. A compact explicit DC model for short channel gate-all-around junctionless MOSFETs. Solid State Electron. 2017; 131:24-29.
[29] Winitzki S. Uniform Approximations for Transcendental Functions. Springer-Verlag, 2003.
[30] Nandi A, Pandey N, Dasgupta S. Analytical Modeling of DG-MOSFET in Subthreshold Regime by Green's Function Approach. IEEE Trans. Electron Dev. 2017; 64:3056-3062.
[31] Megherbi ML, Pezzimenti F, Dehimi L, Saadoune MA, Della Corte FG. Analysis of trapping effects on the forward current-voltage characteristics of al-implanted 4H-SiC p-i-n Diodes. IEEE Trans. Electron Dev. 2018; 65:3371-3378.
[32] Pezzimenti F, Della Corte FG. Design and modeling of a novel 4H-SiC normally-off BMFET transistor for power applications. In Proc. Mediterranean Electrotechnical Conf. – MELECON, 2010; 1129-1134.
[33] Pezzimenti F. Modeling of the steady state and switching characteristics of a normally-off 4H-SiC trench bipolar-mode FET. IEEE Trans. Electron Dev. 2013; 60:1404-1411.
[34] Bouzid F, Dehimi L, Pezzimenti F. Performance Analysis of a Pt/n-GaN Schottky Barrier UV Detector. J. Electron Mater. 2017; 46:6563-6570.
[35] Jin Z, Gao L, Zhou Q, Wang J. High-performance flexible ultraviolet photoconductors based on solution-processed ultrathin ZnO/Au nanoparticle composite films. Sci. Rep. 2014; 4268:1-8.
[36] Bencherif H, Dehimi L, Pezzimenti F, Yousfi A. Analytical model for the light trapping effect on ZnO:Al/c-Si/SiGe/c-Si solar cells with an optimized design. In Proc. Int. Conf. on Applied Smart Systems - ICASS, 2018; 1–6.
[37] Bouzid F, Pezzimenti F, Dehimi L, Della Corte FG, Hadjab M, Larbi AH. Analytical modeling of dual-junction tandem solar cells based on an InGaP/GaAs heterojunction stacked on a Ge substrate. J. Electron. Materials 2019; 48:4107-4116.
[38] Marouf Y, Dehimi L, Pezzimenti F. Simulation study for the current matching optimization in In0.48Ga0.52N/In0.74Ga0.26N dual junction solar cells. Superlattice. Microst. 2019; 130:377-389.
[39] Bencherif H, Dehimi L, Pezzimenti F, Della Corte FG. Improving the efficiency of a-Si:H/c-Si thin heterojunction solar cells by using both antireflection coating engineering and diffraction grating. Optik 2019; 182:682–693.
[40] Bencherif H, Dehimi L, Pezzimenti F, De Martino G, Della Corte FG. Multiobjective optimization of design of 4H-SiC power MOSFETs for specific applications. J. Electron. Mater. 2019; 48:3871-3880.
[41] Bencherif H, Dehimi L, Pezzimenti F, Della Corte FG. Temperature and SiO2/4H-SiC interface trap effects on the electrical characteristics of low breakdown voltage MOSFETs. Appl. Phys. A-Mater. 2019; 125:294.
[42] De Martino G, Pezzimenti F, Della Corte FG. Interface trap effects in the design of a 4H-SiC MOSFET for low voltage applications. In Proc. IEEE Int. Semiconductor Conf. – CAS, 2018; 147-150.
[43] De Martino G, Pezzimenti F, Della Corte FG, Adinolfi G, Graditi G. Design and numerical characterization of a low voltage power MOSFET in 4H-SiC for photovoltaic applications. In Proc. IEEE Int. Conf. Ph. D. Research in Microelectronics and Electronics - PRIME, 2017; 221-224.
[44] Della Corte FG, De Martino G, Pezzimenti F, Adinolfi G, Graditi G. Numerical simulation study of a low breakdown voltage 4H-SiC MOSFET for photovoltaic module-level applications. IEEE Trans. Electron Dev. 2018; 65:3352-3360.
[45] Fiori G, Iannaccone G. A Three-Dimensional simulation study of the performance of carbon nanotube Field-Effect Transistors with doped reservoirs and realistic geometry. IEEE Trans. Electron Dev. 2006; 53: 1782-1788.
[46] Saxena M, Haldar S, Gupta M, Gupta RS. Physics-based analytical modeling of potential and electrical field distribution in dual material gate (DMG)-MOSFET for improved hot-electron effect and carrier transport efficiency. IEEE Trans. Electron Dev. 2002; 49:1928–1938.