DOCTORAL SCHOOL
MEDITERRANEA UNIVERSITY OF REGGIO CALABRIA

DEPARTMENT OF INFORMATION ENGINEERING, INFRASTRUCTURES AND SUSTAINABLE ENERGY
(DIIES)

PHD IN
INFORMATION ENGINEERING

S.S.D. ING-INF/01
XXVI CYCLE

HIGH EFFICIENCY DC-AC CONVERTERS FOR RENEWABLE ENERGY SYSTEMS

CANDIDATE
Demetrio IERO

ADVISOR
Prof. Francesco Giuseppe DELLA CORTE

COORDINATOR
Prof. Claudio DE CAPUA

REGGIO CALABRIA, FEBRUARY 2014

Demetrio Iero

HIGH EFFICIENCY DC-AC CONVERTERS FOR RENEWABLE ENERGY SYSTEMS

The Teaching Staff of the PhD course in
INFORMATION ENGINEERING
consists of:

Claudio DE CAPUA(coordinator)
Raffaele ALBANESE
Francesco BUCCAFURRI
Salvatore COCO
Francesco DELLA CORTE
Domenico GATTUSO
Giovanna IDONE
Antonio IERA
Tommaso ISERNIA
Giovanni LEONE
Massimiliano MATTEI
Carlo MORABITO
Francesco RUSSO
Riccardo CAROTENUTO
Domenico FAMULARO
Antonella MOLINARO
Maria Nadia POSTORINO
Francesco RICCIARDELLI
Domenico URSINO
Mario VERSACI
Antonino VITETTA
Giovanni ANGIULLI
Giuseppe ARANITI
Giacomo CAPIZZI
Rosario CARBONE
Sofia GIUFFRÈ
Fabio LA FORESTA
Gianluca LAX
Luigi MORETTI
Fortunato PEZZIMENTI
Giuseppe MUSOLINO
Domenico ROSACI
Giuseppe RUGGERI
Giuseppe SARNÈ
Ivo RENDINA
Lubomir DOBOS

Contents

List of Figures

IV

1 Introduction

1.1 Introduction

The increasing global energy demand requires the use of new energy sources to cover the future needs. The cost of renewable energies is dropping and renewable energies technologies are gaining competitiveness over traditional energetic sources.

Photovoltaics (PV), which directly converts sunlight into electrical current, is one the most popular renewable energy source. It is gaining competitiveness over traditional energetic sources, and nowadays is well developed, reliable, and almost cost competitive with conventional sources.

The growing PV market has resulted in the need of high efficiency, reliable and inexpensive power conversion systems to convert the DC PV power in AC power (inverters). The inverter acts as the load of PV modules and convert their power into sinusoidal current to feed a load or inject the current into the grid.

Multilevel inverters (MLI) are gaining interest in PV systems because they bring several advantages over traditional inverters. They synthesise an AC output voltage from several DC sources, reproducing a staircase waveform that approximates the sinusoidal signal. Multilevel inverters allow to obtain high-quality waveforms even operating at low frequencies, which translates into high efficiency and less stress for the devices and therefore into an improvement of the reliability. As the number of levels increase, the quality of the output waveform improves and the dV/dt that the switches have to handle is lower due to the reduced steps size.

The multilevel approach is particularly suited for PV systems because the separated DC sources required for these topologies can be easily obtained with a proper connection of PV cells. Multilevel inverters provide also interesting

opportunities in the control strategy of distributed power systems, because they can be designed to control the amplitude and the phase of the output sinusoid and therefore the real and reactive power flow into the grid.

One disadvantage of the MLI is the greater number of power semiconductor switches needed, which increases costs and complexity of the system. Therefore, it is important to reduce the number of switches and gate driver circuits. Moreover, when MLI are connected to PV sources there is another problem that might reduce the global efficiency of the system; in fact, periodically some PV sources are disconnected from the rest of the system and do not produce power. It is essential the usage of proper storage elements that store the PV energy in these time slots.

The objective of this thesis is to develop a PV system based on a MLI topology with a low number of switches and a control algorithm that ensure low power losses while maintaining high the quality of output waveform.

A SPICE simulation model of a complete PV system has been developed, including a model of PV cells, a multilevel inverter, and energy storage elements. Simulations of the complete system allow to readily evaluate the effects on its performances of the variation of the component parameters, the load, the solar irradiation, and the temperature. These simulation are also particularly useful to evaluate the role of storage elements on the global conversion efficiency and the quality of the output waveform for various operating conditions.

A prototype of the MLI has been built and tested with the objective to evaluate the actual behaviour of the inverter. The prototype uses a distributed architecture, with a control circuit associated with each source, that allows to achieve high flexibility and robustness.

The thesis includes also the description and implementation of a calorimetric method based on an heat-flux sensor that allows the estimation of the power dissipated by a switching device. The precise measurement of the power dissipated by a semiconductor device is important for evaluating system efficiency and reliability, but can be difficult when the losses are extremely low. In fact, measurement errors can be introduced by traditional measurement instruments due to limited bandwidth, sampling errors and non-linearities of

the acquisition circuits. As the power losses are dissipated as heat, it is possible to calculate them by measuring the heat produced by the device; this method allows a measure of the losses that is independent from electrical quantities. The realized set-up, simpler than other calorimetric methods, is based on a custom made heat-flux sensor coupled with a thermoelectric module that keep the switching device at room temperature minimizing the heat exchanged with the ambient.

1.2 Organization

The thesis is organized as follows.

Chapter 2 gives an overview of the market and status of PV energy. Principles of operation of the PV cells and modules are explained and an historical overview of materials and technologies used in the construction of the PV cell is also provided. Two different electrical models (single and double diode) of the PV cell are discussed.

Chapter 3 gives an overview of the multilevel inverter topologies with a description of the advantages that they provide over traditional inverters. A comparison of the advantages and drawbacks of the three basic topologies of multilevel inverters, and a multi-cell cascade topology that solve some of their issues is also provided. Furthermore, a control technique for the inverter that allows to achieve good quality in the output waveform while maintain low the power losses is presented. Additionally, there is an analysis of some of the components used in a multilevel inverter, and their losses; in particular the power MOSFET is analysed and a thermal model is provided. Finally some technologies and materials that could allow to overcome the limits of traditional silicon power devices, and increase their efficiency, are described.

In chapter 4 is presented the calorimetric method based on a micro-machined dual-sensor heat-flux measurement device. The chapter include an introduction to the problematic that could affect the power loss measurement with traditional methods, and an overview of existing calorimetric methods. The realized calorimetric apparatus, its working principle

and the heat-flux sensor are then presented, and some simulation and measurements are provided.

Chapter 5 includes a description of the multilevel inverter topology used in this thesis work, with its characteristic and differences with literature topologies. Moreover, the control technique used to command the switches of the inverter is described with details about the calculation of the switching angles.

In chapter 6 a SPICE simulation model of a complete photovoltaic system is presented, including a detailed model of photovoltaic cells, a multilevel inverter, and energy storage elements. The conversion efficiency and the total harmonic distortion (THD) of the output waveform are analysed. The role and sizing criteria of a storage element, placed at the PV module output, are also analysed for various operating conditions. Furthermore, there is an analysis of the efficiency and power losses distribution across the various components of the inverter.

Chapter 7 is about the realization of the multilevel inverter prototype based on the previous described topology. A description of the design and characteristics of the various elements that constitute the inverter is provided; hardware and software of the three main parts of the inverter are described in detail. In the last paragraphs, measurements made on the multilevel inverter prototype, for different number of levels, are provided.

Finally, conclusions summarize the thesis work and provide an overview of possible future improvements.

2 Renewable energy from photovoltaics

The energy captured by the PV cells is renewable, unlimited, and environment friendly, but its cost is high and only recently it is becoming competitive with other energy sources. This chapter introduces the PV cell, with a short review of its working principles and an historical overview of materials and technologies used in the construction of the PV cell. Particularly attention is addressed at the electrical model of the PV cell, its parasitic elements and the factors that limit the cell efficiency; a single diode model and a double diode model of the PV cell are discussed.

2.1 Introduction

The global energy demand is steadily increasing, and the renewable energies are gaining competitiveness over traditional energetic sources. The cost of renewable energies is dropping and further reductions will be possible as demand and production increase. Nowadays, renewable energy technologies are well developed, reliable, and cost competitive with the conventional sources.

Among renewable energies, one of the most important source is the photovoltaic energy. The PV technology is essentially the conversion of the energy radiated from the sun into usable electrical form though the use of PV solar cells.

In the last twenty years, the photovoltaic market has seen an exponential development with a global installation of over 100 GW all over the world (Fig. 2.1) [1]. Even in a context of reduced incentives, Germany, with 7.6 GW installed in 2012, leads the market. Italy is in second place with 3.6 GW installed in 2012, down from the tremendous record of 9.3 GW in 2011, due to

regulatory changes and reached financial cap set to limit the cost of the incentives. China and USA follow, with China trying to push its internal PV market, to reach 35 GW by the year 2015. Fig. 2.2 shows how the global PV market and cumulative installed capacities are distributed in the world in 2012.

It has been estimated that in Italy, the 16.4 GW installed have produced about 7% of the electricity demand of the country in 2013; as shown in Fig. 2.3, it is an undisputed world record. Italy used Feed-in Tariffs[1] (FiT) to develop the PV market; the cost of the FiT is mutualised in the electricity bill and the stimulus have been stopped when the annual costs of all FiTs reached 6.7 billion of euros a year, which happens in 2013. The Italian PV development will now have to rely on self-consumption. In 2011 a self-consumption regulation has been added, the "Scambio Sul Posto" which provides an economic remuneration for the energy injected into the grid and consumed instantaneously. With high solar resources, especially in the south, and relatively high electricity prices, Italy could become a benchmark for self-consumption installations.

In 2012, the average price of PV systems was around 2.8 USD/W, about 22% lower than the average 2011 price (3.6 USD/W). PV modules were in the past the major contributor to the cost of the systems, but the massive increase in production capacity yield a downward tendency in the price of the modules, as can be seen in Fig. 2.4. In 2012, the average price of PV modules was about 1.16 USD/W, a decrease of almost 16% compared to 2011, following a decrease of 50% in the previous year. Now the average price is below 1 USD/W.

Several progresses have been made to reduce the cost and increase efficiency of PV systems. However, in order to compete with traditional energy sources, it is also essential to develop high efficiency and low costs power conversion systems to convert the PV-generated power, which is DC, in AC power to feed the grid or supply electric equipment.

---

[1] With Feed-in Tariffs, electricity produced and injected into the grid is paid at a predefined price guaranteed for a certain period.
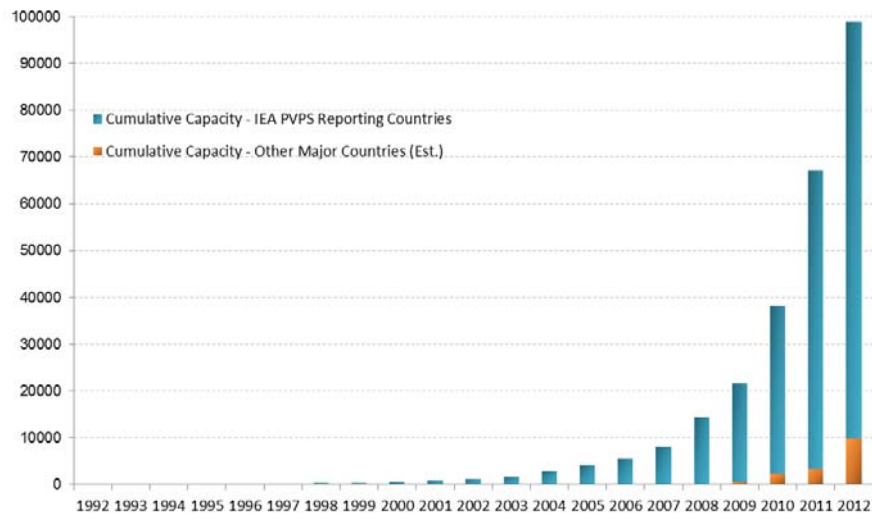
Fig. 2.1 Evolution of cumulative PV capacity (MW) from 1992 to 2012 [1]

(a)   (b)
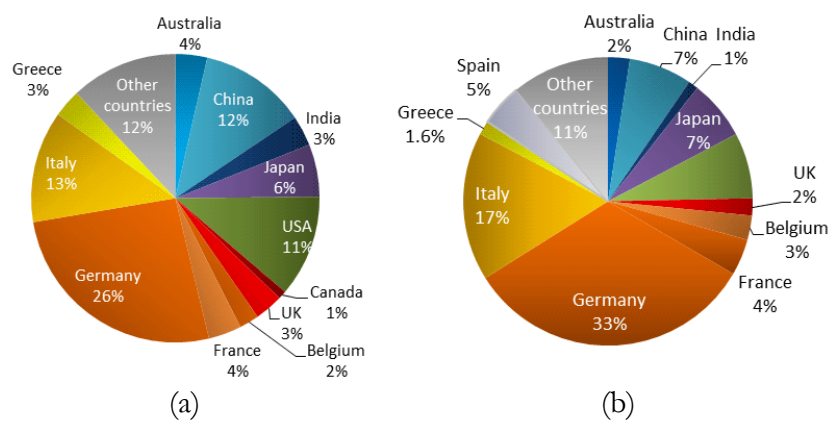
Fig. 2.2 PV market share: a) global market in 2012; b) cumulative installed capacities in 2012 [1]
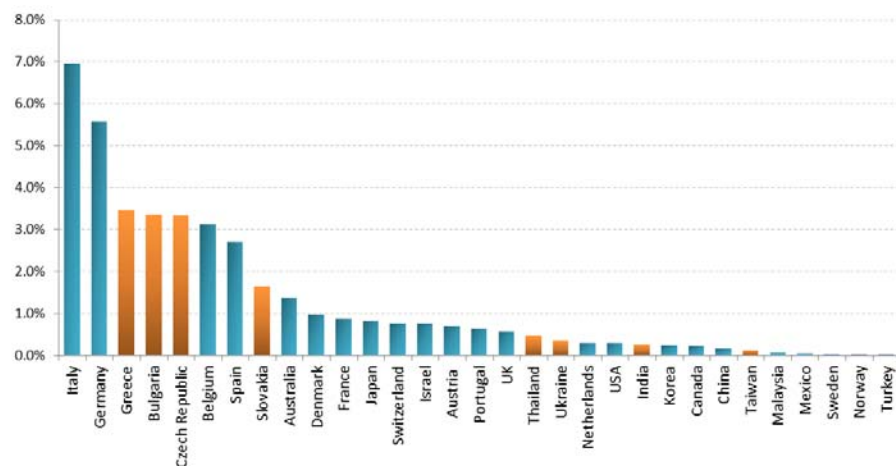
Fig. 2.3 Theoretical PV electricity production based on installed capacity at the end of 2012 [1]
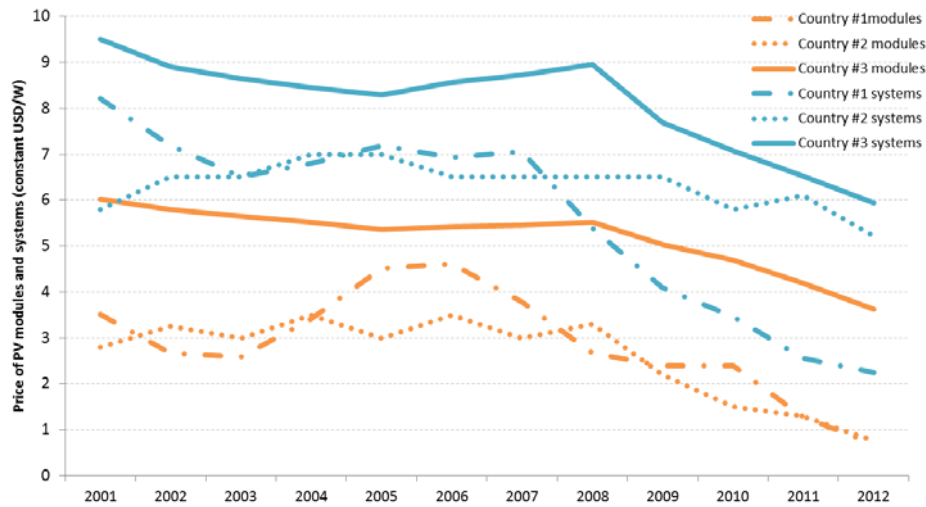
Fig. 2.4 Evolution of prices of PV modules and residential PV systems in selected countries from 2001 to 2012 [1]

2.2 Photovoltaic cells and modules

Photovoltaic systems use solar energy to produce electricity though the electronic properties of semiconductor materials. The photovoltaic effect is the phenomenon, related to the photoelectric effect, that allows the formation of a voltage, and a corresponding electric current, in a material upon exposure to light.

Photovoltaic cells can be made with various semiconductor materials in which carrier generation takes place in excess when they are exposed to heat or light. A common PV cell is basically a large P-N junction made from Silicon. The silicon atom contains four electrons in the outer shell which bind the atom with four other silicon atoms. When doped with boron which has three electrons in the outer shell, the electron deficit creates a "hole" in the silicon lattice, obtaining a surplus of positive charge carriers that can move around in the lattice (P-type material). When doped with phosphorus, which has five electrons in the outer shell, there is a surplus of negative carriers (N-type material). A P-N junction is formed when two layers with different doping are put in contact; a diffusion of electrons takes place in this moment from the N side to the P side of the junction where they recombine with holes and, similarly, a diffusion of holes from the P side to the N side takes place. The

carriers amass on the two side of the junction establishing an electric field that arises a drift current opposite to the diffusion one. Eventually an equilibrium is reached whereby a depletion region (space charge region) without free charge carriers is formed.

The generation of current in a PV cell involves two processes: absorption of the photons and collection of the charges. When a photon hit the cell and its energy is higher than the silicon band gap value, it is absorbed and "excites" an electron from the valence band into the conduction band generating an electron-hole pair which is separated by the electrical field (collection of carriers by the junction). If the generated minority carrier reaches the junction, it is swept through the junction by the electric field and become a majority carrier. If the outer circuit is closed, the photo-generated carriers flow through the external circuit as shown in Fig. 2.5.

The energy of incoming photons is:

$$E_{photon} = \frac{h\,c}{\lambda}, \tag{2.1}$$

where h is the Planck constant ($h = 6.625 \times 10^{-34}$ J·s), c is the speed of light ($c = 2.998 \times 10^{8}$ m/s), and λ is the wavelength of the incoming photon. The majority of suns spectrum is between 400 nm to 1500 nm that corresponds to an energy between 0.83 eV and 3.10 eV, whereas the energy band gap of Silicon is about 1.12 eV. The majority of the radiation is therefore composed of photons with energies greater than the band gap, and when these photons are absorbed the difference in energy with the silicon band gap is converted into heat, lowering the conversion efficiency.
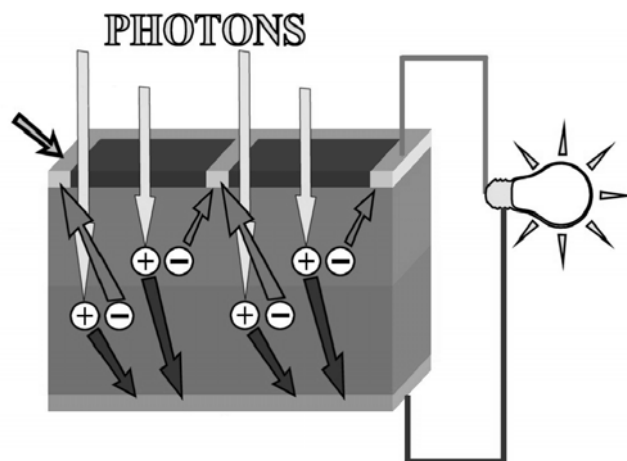
Fig. 2.5 Operating principle of a PV cell

An electrical voltage is produced at the cell contacts and, when a load is connected, the photocurrent generated in the cell can flow. The voltage depends on the design and the material of the cell, whereas the current depends especially on the solar radiation intensity and the cell area. A simplified equivalent circuit of a PV cell consists of a current source in parallel with an ideal diode as shown in Fig. 2.6. The ideal I-V characteristic can be expressed with the following ideal formula:

$$I = I_{PH} - I_0 \left(e^{\frac{qV}{kT}} - 1 \right), \tag{2.2}$$

where I_{PH} is the photocurrent that depends linearly on the solar irradiance, I_0 is the reverse saturation current of the diode, q is the electron charge ($q = 1.6 \times 10^{-19}$ C), k is the Boltzmann constant ($k = 8.62 \times 10^{-5}$ eV·K^{-1}), and T is the solar cell operating temperature (K). The I-V characteristic of a PV cell is equivalent to an "inverted" diode curve (Fig. 2.6) and in the dark ($I_{PH} = 0$) the cell behave exactly like a diode.

The short-circuit current (I_{SC}) is the maximum current generated by a solar cell, obtained when the two terminals of the cell are short-circuited ($V = 0$) and therefore the entire photocurrent generated can flows out. When the load of the cell is increased, a quota of the photocurrent flows through the diode and the output current decrease. The open-circuit voltage (V_{OC}) is the maximum voltage of a solar cell, measured when the net current through the device is zero; if the cell is open-circuited, the output current is zero and the entire current flows through the diode.
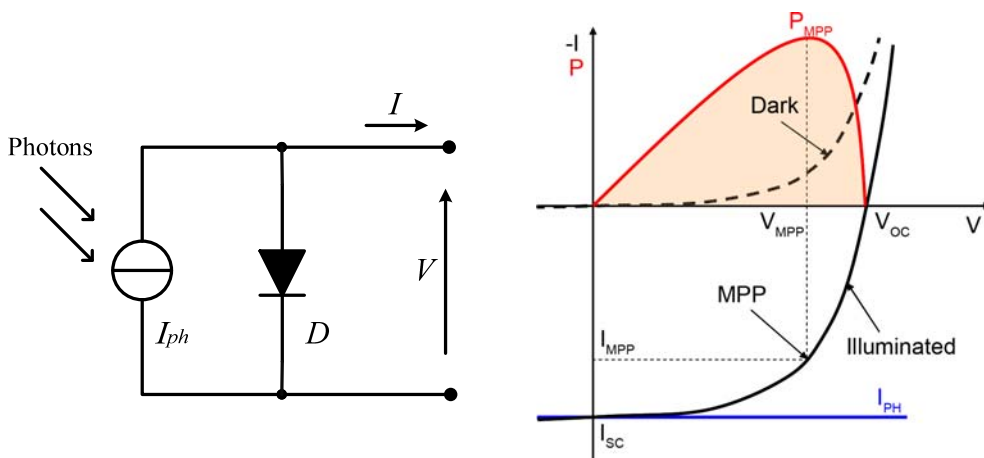
Fig. 2.6 Simplified equivalent circuit for a solar cell and I-V characteristic

2.2.1 Maximum Power Point and effect of irradiation and temperature

As a power source, the PV cells have an optimal working point called Maximum Power Point (MPP) at V_{MPP}, I_{MPP}. As shown in Fig. 2.6, the power produced by a cell increases as the voltage increases, reaching a maximum, i.e. the MPP, where the load matches the cell resistance. The I-V characteristic changes with solar irradiance and the temperature (Fig. 2.7) and therefore the MPP is not a fixed point. Maximum Power Point Tracking (MPPT) circuits can be used to follow the MPP and to extract the maximum available power from the cells even in variable conditions.

With an increase of the solar irradiance, the open-circuit voltage (V_{OC}) increases with a logarithmic law, whereas the short-circuit current increases linearly.

The temperature affects the equation (2.2) directly, though the exponential term, and indirectly via its effect on the saturation current I_0, with a net effect to reduce the open-circuit voltage due to the reduction of the band gap of the semiconductor. The photocurrent increases slightly with increasing temperature due to an increase of the number of thermally generated carriers. However, since the voltage exhibits a much larger change than the current, the overall effect is a decrease of the efficiency of the solar cell. The other terms of the equation are also effected by the temperature, but in a far less significantly way.
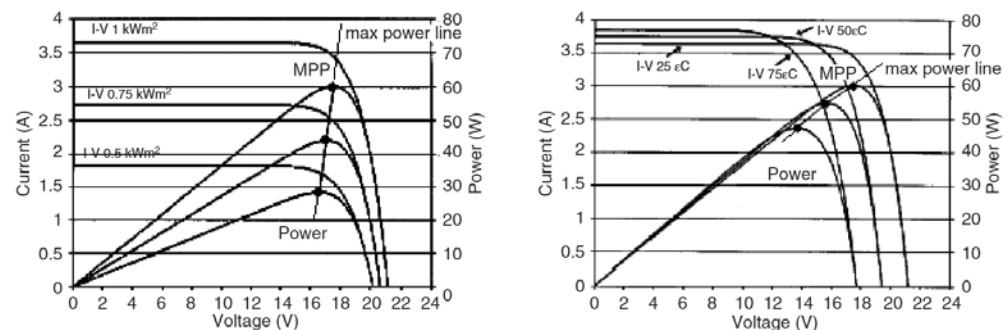
Fig. 2.7 PV cell I-V characteristics at variable solar irradiance and temperature

2.2.2 Efficiency of solar cells

The conversion efficiency of a PV cell is the percentage of the solar energy that is converted into electrical energy, and it is sensitive to variations of power and spectrum of the incident radiation.

Solar radiation approximates a black body radiator at about 5800 K, but the spectrum is modified due to scattering and absorption as the sunlight passes through the atmosphere. The density of power radiated from the sun is denoted as "solar energy constant" and its average value in the outer atmosphere is 1.361 kW/m^2 [2]. It is measured at a fixed distance of one astronomical unit and therefore the actual solar irradiance fluctuates by about 7% during a year due to the varying distance between the Earth and the Sun. However, the solar radiation received on the surface of the Earth depends on the location, the state of the atmosphere, and the time of day. Therefore, the final incident radiation on Earth's surface has a peak of about 1 kW/m^2 at noon in the tropics.

A standard spectrum and power density has been defined to facilitate the comparison between solar cells. The air mass (AM) coefficient, which corresponds to the direct optical path length through the atmosphere related to the zenith path length, is commonly used to characterize the performance of solar cells. "AM0" is the spectrum outside the atmosphere, whereas "AM1" is the spectrum at sea level with the sunlight directly perpendicular. "AM1.5" corresponds to a zenith angle of 48.2° and is as industry standard to represent the yearly average for mid-latitudes. Fig. 2.8 shows the solar radiation spectrum for AM0 and AM1.5.

After the generation, electrons in the P-layer and holes in the N-layer are minority carrier that will exist only for a limited time (minority carrier lifetime) before they recombine. If a carrier recombines before being collected, the electron-hole pair is lost and does not contribute to electric power production. The probability of recombination depends on the distance that a carrier has to travel compared to the diffusion length (average distance a carrier travels until it recombines), and also on the surface properties of the device. The collection probability, i.e. the probability that a carrier generated by light is collected by

the junction and contributes to the photo-generated current, is highest in the depletion region and drops away from the junction.

The overall efficiency of a solar cell is limited by recombination of charge carrier, reflectance, and conductivity of material and contacts. Two parameters usually used to measure the efficiency of a PV cell are the quantum efficiency (QE) and fill factor (FF).

Quantum efficiency is the percentage of photons that are converted to electric current at a given wavelength. QE is one when all the photons of a given wavelength are absorbed and the generated minority carriers are collected (ideal cell), whereas it is zero for photons with energy below the band gap. The QE is reduced as result of recombination effects and optical losses due to reflection and transmission. In a silicon cell, QE is reduced in particular at low wavelengths, due to surface recombination (blue light is absorbed close to the surface), and at high wavelengths (red portion of the spectrum) where it is affected by rear surface recombination and reduced absorption due to the low energy of the photons. An overall reduction of QE is furthermore caused by the reflection and the low diffusion lengths. Fig. 2.9 shows the typical quantum efficiency curve of a silicon solar cell.

The **fill factor** (FF) is a measure of the "squareness" of the I-V characteristic (Fig. 2.10) and is defined as:

$$FF = \frac{V_{MPP} \cdot I_{MPP}}{V_{OC} \cdot I_{SC}}. \qquad (2.3)$$

Cells with a high fill factor have a low equivalent parasitic resistances (cf. paragraph 2.4) and therefore lower losses and higher output power, closer to their theoretical maximum.

The efficiency can be defined as the ratio between the cell maximum output power and the solar radiation on the cell surface P_i:

$$\eta = \frac{P_{MPP}}{P_i} = \frac{V_{MPP} \cdot I_{MPP}}{G \cdot A_C} = FF \frac{V_{OC} \cdot I_{SC}}{G \cdot A_C}, \qquad (2.4)$$

where G is the solar irradiance (W/m^2) and A_C is the cell surface (m^2). The efficiency depends on the spectrum and intensity of the incident radiation and

the temperature of the solar cell, therefore it is usually measured under standard test conditions[2] (STC) to allow performance comparison.

The material used to construct the cell has a great impact on the efficiency; materials with high energy-gap have higher V_{OC}, but I_{SC} is lower because they collect a lower portion of the solar spectrum. The theoretical limit for a single-junction crystalline silicon cells is about 30%, whereas stacked multi-junction structures can reach much higher efficiency, with a theoretical limit of 86% for concentrated sunlight [3].
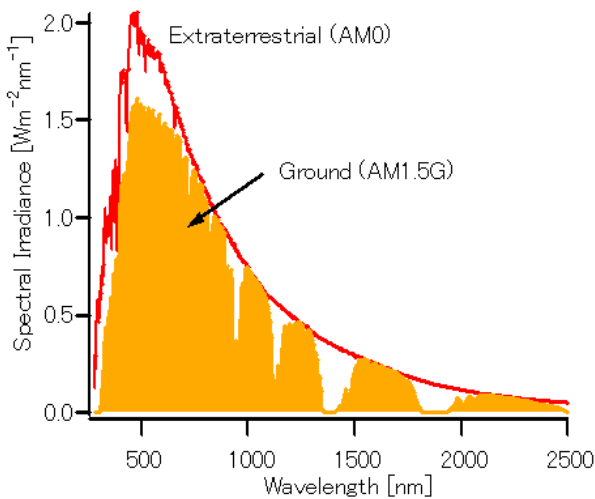
Fig. 2.8 Solar radiation spectrum at AM0 and AM1.5
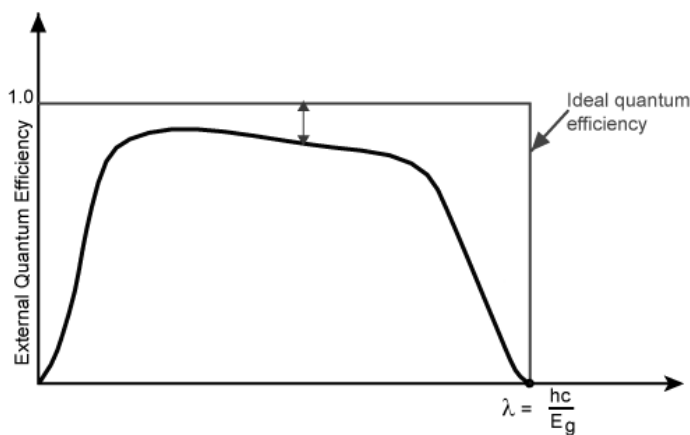
Fig. 2.9 Typical quantum efficiency of a silicon solar cell

---

[2] Standard Test Conditions specifies an irradiance of 1000 W/m^2 and a temperature of 25 °C, with an AM1.5 spectrum and a wind of 0 m/s.
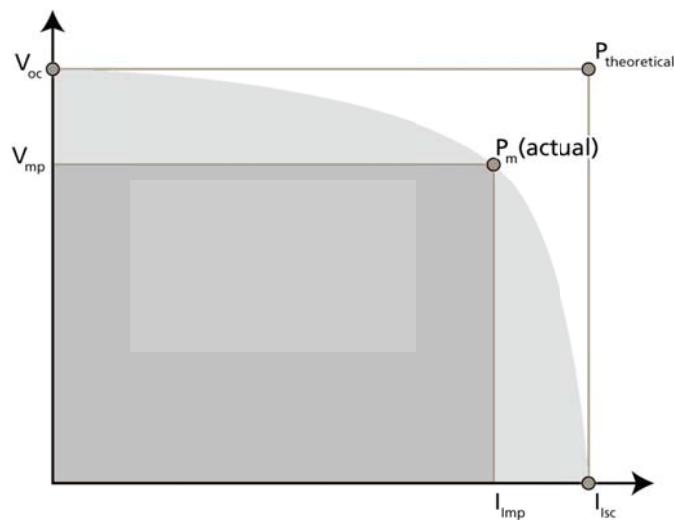
Fig. 2.10 Graph that shows the key point for the calculation of the fill factor

2.2.3 PV modules

For a silicon cell under standard test conditions, V_{OC} is typically 0.5-0.7 V, and I_{SC} is typically 20-40 mA per cm^2. To achieve higher voltages and currents, it is possible to connect together more cells into a series (higher voltages) or parallel connection (higher currents) to set up a PV module. A group of PV modules connected together compose a PV array or string.

A PV module (Fig. 2.11) consists of a number of interconnected solar cells packed in a single structure with the purpose to isolate and protect the cells that are extremely thin and fragile, ensuring operation even in harsh environmental conditions.

PV modules structures differ for different types of solar cells and applications. They are basically constituted of: a transparent top surface, an encapsulant, a rear layer, and a frame. The top layer, which is usually glass, should be transparent at the wavelength of the solar spectrum, resistant to protect the cells, and with low-reflectivity. The encapsulant is used to stick the cells at the top and the rear surface, and the frame complete the module package.

Solar cells in commercial modules are usually connected in series to achieve higher voltage, whereas higher currents are obtained increasing the cells area. Mismatching properties of the cells or shadows that cover some of

the cells can cause serious issues because the output of the entire module is limited by the "weak" cell. When a cell is shadowed it become reversed biased and, if the reverse voltage is high enough the avalanche current that will flow, dissipated as heat, can result in hot-spots that may damage the module.

To avoid mismatch problems it is possible to use bypass diodes connected in anti-parallel with the cells (or modules), that exclude the weaker cells (or modules) and allow the flow of the current generated by the other cells in the external circuit. Since the use of a bypass diode of each cell is not practical, the diodes are usually placed across groups of solar cells with various possible configurations.

Partial shadow produces also an irregular I-V curve, in which there are local MPP that can treat the MPPT algorithms.
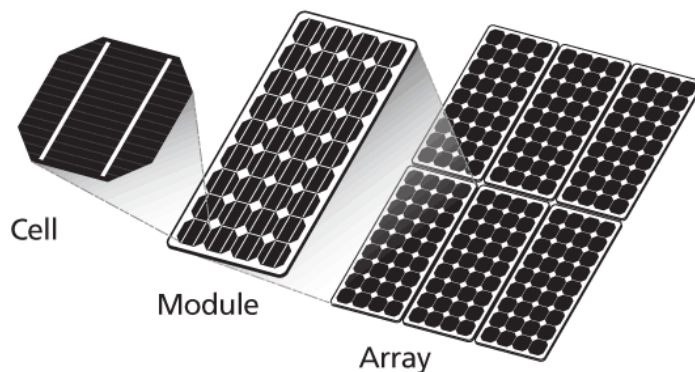
Fig. 2.11 PV cell, module and array

2.3   History and materials overview

The photovoltaic effect is a quantum-mechanical process which regards the creation of a voltage, or a corresponding electric current, in a material upon exposure to light. It was first observed in 1839 by A. E. Becquerel, whereas C. Fritts built the first solid state photovoltaic cell in 1883. Only in 1954, Person, Fuller, and Chapin obtained the first practical photovoltaic cell based on Silicon P-N junction capable to reach 6% efficiency. In 1960, with the development of semiconductor industry and the mass production of solar cells, it was possible to increase the efficiency up to 14%.

Even due to the high cost, one of the first applications in those years were the power of artificial satellites and the majority of studies were committed to improving the resistance of the cells to the interplanetary space conditions. Since the cells were made with the same manufacturing processes of semiconductors, as the wafers price fell, the price of the cells did as well. In 1971 cell price were still over 100 USD per watt, but in those years the research focused on the reduction of the production cost and in few years the cost was decimated.

Berman and his team (Solar Power Corporation, Exxon) realized that some modification at the manufacturing process could be made to eliminate a few steps regarding e.g. the anti-reflective surface and electrodes printing. Also the mounting techniques were improved by eliminating expensive materials. These modification, and the use of lower quality wafers casted off by the electronics industry, allow them to reach by 1973 a production cost of 10 USD/W.

In the '90s, polysilicon cells became popular thanks to the reduced production cost compared to the more efficient monosilicon counterparts. Further improvements in recent years brought the production costs of a module below 1 USD/W. New technologies with increasing efficiencies and reduced price will lead to a future, where PV power will be price competitive with conventional power sources.

The most common types of PV cells use silicon, however a number of semiconductor materials match the spectrum of available light and are suitable for the manufacturing of solar cells. Among the different constructive typologies, the most commons include: crystalline silicon (monocrystalline or polycrystalline), thin films (amorphous silicon, cadmium telluride, copper indium selenide, etc.), hybrid and multijunction cells.

The first generation of solar cells include devices in crystalline silicon built on the concept of a simple P-N junction. The majority of PV cell in the market use silicon also because it is possible to use processes already used in electronic industry and to "recycle" ingot with impurities that are not suitable for electronic manufacturing processes.

Monocrystalline silicon cells use wafer cut from cylindrical ingots, usually made using the Czochralski process and, because of the manufacturing processes required, it is the most expensive type of silicon cell. The cells have an ordered crystal structure and exhibits uniform behaviour with a well-defined band structure. Being grow from cylindrical ingots, the cells have a circular or semi-square shape, so they can be more efficiently packed into a module. These cells have a typical efficiency of about 15-20% with a best research efficiency of 25% [4].

Poly- or **multi-crystalline** silicon cells are produced with simpler and cheaper techniques than those required for mono-crystal material and therefore are less expensive. However, the quality is lower than that of single crystalline due to the presence of grain boundaries that produce recombination regions (energy levels in the bandgap) and reduce the carrier flows. The worsen electronic properties yield to a decrease of the efficiency, which has typical values of 13-16%, with 20.4% reached in laboratory [4]. These cells are usually made from slab of polycrystalline material produced by cooling molten silicon, cut in smaller bricks and then rectangular wafers that best fit PV modules, minimizing material waste. Other production techniques e.g. sheet and ribbon, allow to further reduce production costs.

Usually the term multicrystalline is used to indicate material with grain greater than 1 mm, whereas polycrystalline is used for material with grain between 1 µm and 1 mm, usually produced through chemical-vapour deposition (CVD). Finally, the term microcrystalline is used for material with grain < 1 µm, obtained though plasma deposition (PE-CVD) [5].

Thin-films solar cells represent a relevant market share; they have generally significantly lower conversion efficiencies than the crystalline ones, and for this reason have not become a mainstream product. The three main thin-film technologies are Amorphous Silicon (a-Si), Cadmium Telluride (CdTe), Copper Indium Gallium Selenide (CIGS). CIGS technology has the higher laboratory efficiency (20.8%) [4], whereas CdTe is the most cost effective and widely used [6]. CdTe solar cell can rival crystalline silicon in cost/watt but the tellurium is rare material and cadmium is toxic if released.

Single junction GaAs thin-film cells are at the moment the most efficient thin-film technology, with a record of 28.8% [4].

Silicon thin-film cells can be divided in amorphous, and nano- or micro-crystalline silicon. They are generally made with CVD, and can be deposited at low temperatures, enabling production on flexible and low-cost substrates. Amorphous silicon own a disordered structure that extends the absorption rate in a thicker layers compared to crystalline cells, resulting in a less material required to make a solar cell [7]. However, this material presents a lot of defects, e.g. recombination centers that reduce the carrier lifetime, that significantly low the conversion efficiency. The efficiency is higher in micro-crystalline silicon that provides, thanks to the presence of small crystals and therefore a more ordered structure compared to amorphous.

Hybrid technologies combine thin layers, creating a layered cell called "**tandem**" that has a better utilization of the solar spectrum. Amorphous silicon has a higher bandgap (1.7-1.9 eV) than crystalline silicon (1.12 eV) and therefore it absorbs manly the visible part of the solar spectrum. Micro-crystalline has about the same bandgap of crystalline silicon and can therefore absorbs also the infrared portion of the spectrum. These two materials can be combined in thin layers, where the top a-Si cell absorbs the visible light and the bottom cell the infrared part of the spectrum. This can increase considerably the efficiency of amorphous cells.

Multi-junction technology consist of multiple thin films grown on top of each other, where each junction is tuned to absorbs a specific wavelength bands in the solar spectrum. On the top there is the material with largest bandgap that absorb the short wavelength (the blue part of the spectrum), and transmit the portion of the spectrum with longer wavelength to subsequent layers where materials with lower bandgap absorb them (Fig. 2.12). Each type of semiconductor has a bandgap which allows it to absorb electromagnetic radiation most efficiently in a portion of the spectrum. Multi-junction is the technology that offer the maximum efficiency and is used especially with solar concentrators.

The concentrated PV systems use mirrors or lenses to concentrate a large amount of sunlight onto a small area. This technology allows to reach much a higher efficiency and is usually used in conjunction with small multi-junction cells that have an high cost per area. The cost per watt of a concentrated system could be lower than a traditional one since only a small active area is needed. However, efforts must be carried out to optimize optics, solar trackers, and cooling systems; because of these costs this technology has not been largely adapted on the market yet.

GaAs based triple junction cells are the most efficient devices to date with an efficiency record of 44.7% measured at a concentration of 297 suns (a sun corresponds to 1 kW/m^2) [8].
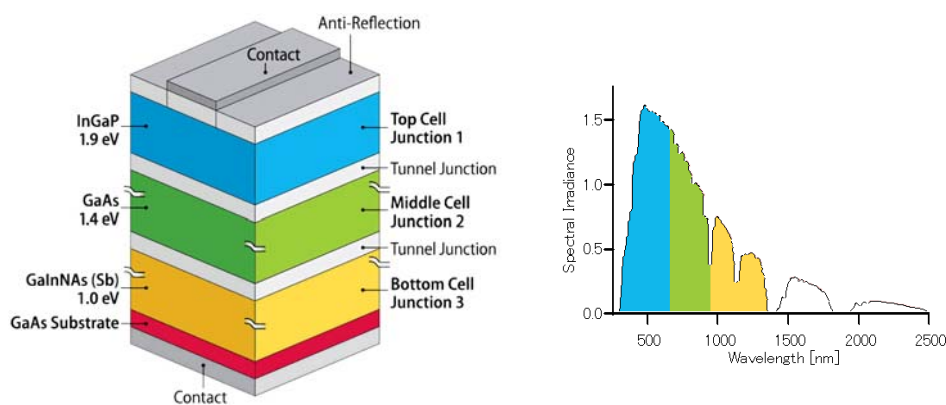
Fig. 2.12 A multi-junction cell

Besides, semiconductors research, a lot of development has been done on the cell design. The top contact area can be minimized to reduce the coverage of the cell area, e.g. buried contacts, rear contact solar cells.

Surface recombination can be reduced with surface passivation and heavy doping at contact area. This high dosage keeps minority carriers away from the high recombination zone, and reduce contact resistance.

Anti-reflective coatings can be applied to reduce reflections and transmit all light into the semiconductor, whereas texturing the surface of the cell allows the refracted light to hit the surface again, thus reducing the overall light reflected out. Light trapping schemes, which use for example textured surface

and back-reflector, can enhance the absorption of sunlight by maintaining a long optical path also for device with reduced thickness.

2.4 Model of the PV cell

The characteristic of a solar cell working as a current generator is similar to that of a diode, with the current depending in an exponential way on the voltage. The basic equation that analytically describes the I-V characteristic of the ideal PV cell is derived by solving the minority carrier diffusion equation. In particular, the solution can be used to evaluate the minority carrier current density equation [9].

The ideal model of the PV cell (2.2) does not take into account some fundamental aspects that affects the device behaviour, e.g. parasitic resistances. The most common parasitic resistances are series resistance (R_S) and shunt resistance (R_{SH}), whose inclusion results in the circuit of Fig. 2.13.
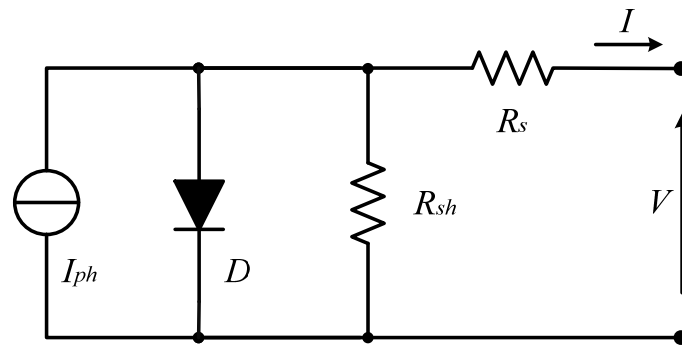
Fig. 2.13 Equivalent circuit of PV cell with parasitic resistances

The characteristic equation of a cell, equivalent to the above circuit, is:

$$I = I_{ph} - I_0 \left(e^{\frac{V + IR_S}{nV_T}} - 1 \right) - \frac{V + IR_S}{R_{sh}}, \qquad (2.5)$$

where n is the ideality factor of the diode, V_T is the thermal voltage ($V_T = k \cdot T / q = 25.9$ mV at 300 K). I_0, R_S, and R_{SH} depend on the physical size of the solar cell: an increase of the cell area increase proportionally I_0, and

decrease R_S, and R_{SH}. The value of these parameters cannot be measured directly, but could be extracted through a nonlinear regression of the equation on the basis of their effect on the cell behaviour.

The **open-circuit voltage** V_{OC} is the maximum cell voltage, obtained when the external current is zero ($I=0$). From the (2.5):

$$0 = I_{ph} - I_0 \left(e^{\frac{V_{oc}}{nV_T}} - 1 \right) - \frac{V_{oc}}{R_{sh}}, \tag{2.6}$$

assuming the R_{SH} high enough to be neglect:

$$V_{oc} \approx \frac{nkT}{q} \ln \left(\frac{I_{ph}}{I_0} + 1 \right). \tag{2.7}$$

The (2.7) shows that V_{OC} depends on the saturation current and the photo-generated current. The saturation current I_0, which depends on the recombination in the solar cell and can vary by orders of magnitude, has the biggest impact on V_{OC}.

The **short-circuit current** I_{SC} is the current that flows in the cell when its short circuited ($V=0$). From the (2.5):

$$I_{SC} = I_{ph} - I_0 \left(e^{\frac{I_{SC}R_s}{nV_T}} - 1 \right) - \frac{I_{SC}R_s}{R_{sh}}, \tag{2.8}$$

if R_S and I_0 are low and R_{SH} high, then $I_{SC} \approx I_{ph}$, and therefore it depends on a the area of the solar cell, the light intensity and spectrum, and the collection probability.

The **series resistance** represents the losses due to the resistivity of the emitter and base layers, the contact resistance between the silicon and the metal, and the resistance of the top contact grid and rear contacts. Its key impact is the reduction of the fill factor; very high values may also reduce the short-circuit current (Fig. 2.14a). An estimation of the series resistance can be made by finding the slope of the I-V curve at the open-circuit voltage point (Fig. 2.15):

$$\left(\frac{dI}{dV} \right)_{I=0} = -\frac{1}{R_s}. \tag{2.9}$$

The **shunt resistance** schematizes the effect of manufacturing defects that provides an alternate path for the photo-generated current. This, in turn, reduces the amount of current flowing through the junction and also the voltage of the solar cell (Fig. 2.14b). An estimation of its value can be made from the slope of the IV curve in the short-circuit current point (Fig. 2.15):

$$\left(\frac{dI}{dV}\right)_{V=0} = -\frac{1}{R_{sh}}. \tag{2.10}$$

(a)   (b)
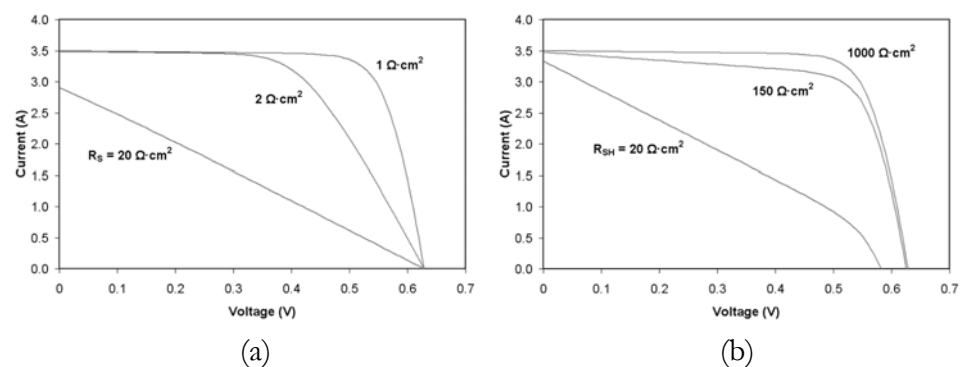
Fig. 2.14 Effect of series (a) and shunt (b) resistance on the I-V characteristic
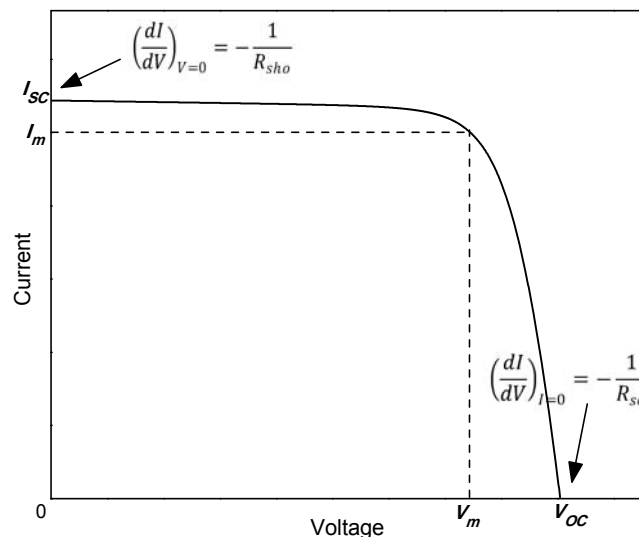
Fig. 2.15 Key features of a solar cell I-V curve

The **ideality factor** (n) is a measure of the junction quality and the type of recombination, which describes how closely the diode follows the ideal equation. The ideal diode equation ($n = 1$) assumes that all the recombination occurs away from the junction and band-to-band. However, recombination

does occur also within the space-charge region and there are intermediate energy levels within the bandgap that act as recombination centers. The ideality factor provides a way to describe these second order effects that are not considered in the ideal diode. The ideality factor is 2 for the recombination in the depletion region and therefore when recombination that happens in the junction dominates other recombination.

A high ideality factor impacts on the FF and reduce the efficiency. Most solar cells exhibit near ideal behaviour ($n \approx 1$) under STC, but under certain circumstances the process may be dominated by recombination in the depletion region. In this case there is a substantial increase of I_0 and ideality factor ($n \approx 2$); the latter increases V_{OC} while the former tends to erode it and is usually the predominant effect.

In the double diode model there is a second diode that model the recombination on the space-charge region. This model, described in the next paragraph, allows therefore to obtain a better approximation, especially for low polarization levels.

2.5 Double diode model

The single diode model assumes a constant value for the ideality factor, but actually it is a function of the cell voltage. The recombination in the bulk regions is prevalent at high voltage, and the ideality factor is close to one, whereas the recombination in the junction dominates at lower voltages, and the ideality factor approaches two. The junction recombination can be modelled by adding a second diode with ideality factor set to two.

The exponential double-diode model (Fig. 2.16), which takes into account some intrinsic non-ideality factors typical of photovoltaic devices, is often used [10].

The model includes two diodes that model the diffusion and recombination processes.

$$I = I_{ph} - I_{01}\left(e^{\frac{V+IR_S}{nV_T}} - 1\right) - I_{02}\left(e^{\frac{V+IR_S}{mV_T}} - 1\right) - \frac{V+IR_S}{R_{sh}}, \qquad (2.11)$$

where:

- I_{01} is the dark saturation current due to recombination in the quasi-neutral region (diffusion);
- I_{02} is the dark saturation current due to recombination in the space charge region;
- n is the non-ideality factor of the first diode;
- m is the non-ideality factor of the second diode.
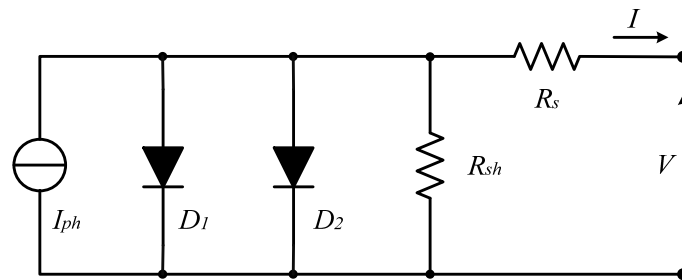
Fig. 2.16 Equivalent circuit of the solar cell (double-diode exponential model).

This model represents the total diode current as the superposition of two currents, separately modelling the contributions of two different conduction mechanisms [11]. The saturation current I_{02} is typically 3-7 orders of magnitude larger than I_{01}. The ideality factor n of the first diode is approximated to 1, whereas the ideality factor m is equal to 2 for the approximation corresponding to the Shockley-Read-Hall recombination of the current in the space charge region [12].

The model parameters depend on environmental conditions and on the materials the cell is made of. By comparison to the experimental I-V characteristic, it is possible to extract the values of the model parameters [13]. The model is non-linear and implicit and therefore it is necessary to use an iterative method to find the coefficients of the analytical expression. The parameters I_{01}, I_{02}, R_s, R_{sh}, I_{ph} can be obtained, for given temperature and irradiance, through an iterative method from the values V_{OC}, I_{SC}, I_{MPP}, V_{MPP}, R_{S0}, R_{SH0} of the I-V characteristic, where R_{S0} and R_{SH0} can be calculated from (2.9) and (2.10).

To take into account the variable atmospheric conditions, the dependence of temperature and irradiance can be introduced in the model. The

photo-generated current is function of the irradiance G (W/m²) and the temperature T (K) at the cell surface:

$$I_{ph}(T, G) = I_{ph,ref}\left(\frac{G}{G_{ref}}\right) + \alpha\left(T - T_{ref}\right), \tag{2.12}$$

where G_{ref}, $I_{ph,ref}$, T_{ref} are respectively the irradiance, the photo-generated current and the temperature in reference conditions and α is the current temperature coefficient.

The parameter most affected by the temperature is the open-circuit voltage, which decreases with temperature because of the temperature dependence of I_0. The two saturation currents I_{01} and I_{02} depend on the temperature through the following relation:

$$I_0(T) = I_0\left(T_{ref}\right)\left(\frac{T}{T_{ref}}\right)^3 e^{\left(\frac{E_g(T)\left(T - T_{ref}\right)}{V_T n T_{ref}}\right)}, \tag{2.13}$$

where energy gap in turn has the following temperature dependence:

$$E_g(T) = E_g(0) - \frac{aT^2}{T+b}, \tag{2.14}$$

with a and b are material constants.

3 Multilevel Inverters

The growing PV market has resulted in the need of high efficiency DC-AC conversion systems. Among the various inverters topologies, multilevel inverters bring several advantages among which the lower switching frequency, meaning in turn less stress for the devices and a lower harmonic content in the output voltage. This chapter includes an overview of the multilevel topologies and the description of a control technique that allows to achieve high-quality waveforms. Finally, some of the components used in a inverter are considered and some comments are provided about technologies and materials that allow to improve the efficiency of semiconductor devices.

3.1 Introduction

An inverter allows to convert a continuous voltage or current into an alternating voltage or current. They are used in different applications as for example: to convert the battery voltage into an AC power in UPS (Uninterruptible Power Supply); to regulate the velocity of electric motors; for static VAR compensation; in the field of renewable energy plants, to convert the generated energy into AC power and deliver it into the grid in grid-connected plants, or to supply a load in stand-alone plants.

There exist different typologies of inverters that allow to obtain an output square-wave, or a quasi-sinusoidal, or a sinusoidal waveform. They can be classified in Voltage Source Inverter (VSI), widely used because many source generally behave as voltage sources, and Current Source Inverter (CSI), the output of which is a current waveform, that are used mainly in system that requires high-quality voltage waveforms.

The output of a VSI is characterized by a voltage waveform with discrete values; an inductive load on VSI inverter allows to produce a smooth current waveform. Although the waveform is not sinusoidal, its fundamental component behaves as such. It is possible to obtain a sinusoidal approximation by using adapt structures and modulation techniques that control the timing and the switching sequence.

A three-level output waveform can only be used for low or medium voltage system due to the high dv/dt that would apply to the load. An alternative approach that allows to improve the quality of the output waveform is the multilevel one that allows to reduce the dv/dt.

Multilevel inverters (MLI) approximate the sinusoidal signal by synthesising the output voltage as a staircase waveform. They allows to obtain high-quality waveforms even operating at low frequencies, which translates into higher efficiency and less stress for the devices and therefore into an improvement of reliability.

In the following there will be analysed the two most common traditional inverter topologies, i.e. Half and Full Bridge, and then the multilevel inverters with special attention to the topology used in this thesis. The chapter closes with an analysis of the modulation techniques and the most important components in a multilevel inverter.

3.2   Half and Full Bridge Inverters

Single-phase VSI can be divided in half-bridge and full-bridge topologies. The **Half-Bridge** inverter is constituted of two switches and two large capacitors that provides a neutral point at $V_{DC}/2$ (Fig. 3.1a).

When Q1 is on and Q2 is OFF the output is $+V_{DC}/2$; conversely, when Q1 is OFF and Q2 is ON the output is $-V_{DC}/2$. To avoid a short circuit between V_{DC} and ground, the switches must be controlled so to ensure that they are never in conduction at the same time. Also the condition Q1-Q2 OFF should be avoided because lead to an undefined state.

The allowed states are shown in Table 3.1, and the output waveform in Fig. 3.1b for a simple square-wave control scheme in which every switch is ON for one half-cycle.

(a)   (b)
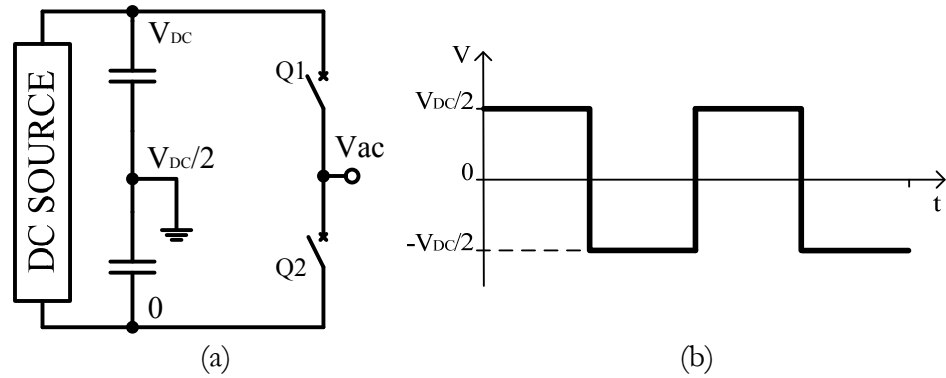
Fig. 3.1 Simplified schematics of single-phase Half-Bridge Inverter and its output waveform

Table 3.1 Switching states for an Half-Bridge inverter

Q1	Q2	Vac
1	0	$+V_{DC}/2$
0	1	$-V_{DC}/2$

The **Full-Bridge** inverter, also called "H-Bridge" is used for higher power systems because the AC output voltage can assume a maximum value that is the double of that of the Half-Bridge. It is similar to the Half-Bridge inverter, but there is a second leg that provides the neutral point to the load. The topology use four switches connected as shown in Fig. 3.2.
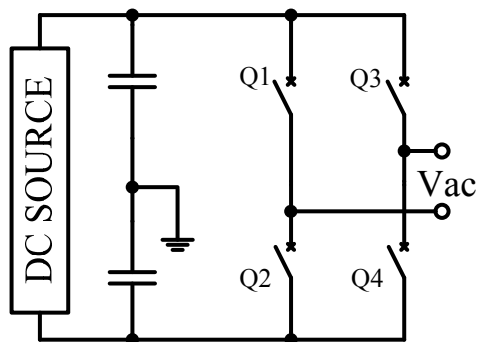
Fig. 3.2 Simplified schematics of single-phase Full-Bridge Inverter

With Q1 and Q4 ON and Q2 and Q3 OFF the output voltage on the load is $+V_{DC}$, whereas when Q1-Q4 are OFF and Q2-Q3 are ON the output voltage is $-V_{DC}$. By turning ON only Q1-Q3 or Q2-Q4 it is possible to achieve a zero output voltage.

The two switch in each leg (Q1-Q2 and Q3-Q4) can never be ON at the same time to avoid a short circuit between V_{DC} and ground. The condition with all the switches OFF is an undefined state and should be avoided.

The possible states of the switches are recapped in Table 3.2. This inverter can be controlled to produce two ($+V_{DC}$, $-V_{DC}$) or three ($+V_{DC}$, 0, $-V_{DC}$) output voltage levels. Fig. 3.3 shows two output voltage waveforms that is possible to produce with the Full-Bridge inverter without the use of high frequency PWM control: a) simple square-wave, b) 3-levels sinusoidal approximation.

Table 3.2 Switching states for an Full-Bridge inverter

Q1	Q2	Q3	Q4	Vac
1	0	0	1	$+V_{DC}$
1	0	1	0	0
0	1	0	1	0
0	1	1	0	$-V_{DC}$

(a)   (b)
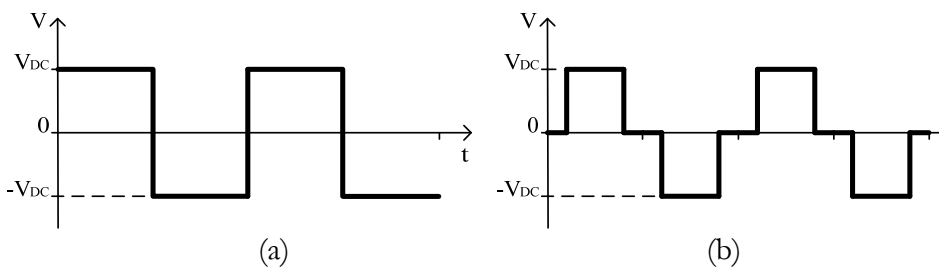
Fig. 3.3 Two possible output waveform of single-phase Full-Bridge Inverter

3.3   Overview of the multilevel inverter topologies

Multilevel inverters use a series of properly connected power static switches to synthesise an AC output voltage from several low voltage DC sources; this allows to reproduce a staircase waveform approximating a sinusoidal signal. The concept of multilevel inverters is known since 1975 [14] and several topologies have been developed over the years [15]–[24].

They are gaining interest in grid connected photovoltaic systems because they bring several advantages over traditional inverters that uses high frequency pulse width modulation (PWM). The lower switching speed of the solid state switching elements turns into less stress for these devices and therefore into an improvement of reliability, a higher efficiency, a low dV/dt, lower electro-magnetic interferences (EMI) and a lower harmonic content in the output waveform, with consequently smaller output filters [25]. Furthermore, multilevel structures allows to reach high voltages without the use transformers or of high breakdown voltage switches [26] because the output voltage is obtained by serialising DC blocks each governed by low breakdown voltage switches.

The multilevel approach is particularly suited for PV systems because the multiple DC sources required for these topologies can be obtained connecting the proper number of PV cells or modules in a series configuration.

Moreover, multilevel inverters can be designed to control both the amplitude and the phase of the output sinusoid and therefore the real and reactive power flow, providing interesting opportunities in the control strategy of distributed power systems [26]. This feature might give small and medium sized power plants an active role in the control of the real and reactive power flow through the grid, as well as of the power quality in case of voltage drops or instabilities, and spurious harmonics [26], [27].

As the number of levels increase, the quality of the output waveform improves because the staircase waveform contains more steps and better approaches the sinusoid without the use of output filters. Furthermore, the dV/dt that the switches have to handle at each commutation is lower because the steps are smaller. However, the higher the number of levels, the higher the

number of switching devices and therefore the cost and complexity of the system. So it is important to reduce the number of switches and gate driver circuits.

There are three basic topologies of multilevel voltage-source inverters: Neutral Point Clamped (diode-clamped) [18], Flying Capacitors (capacitor-clamped) [16], [28], and Cascaded H-bridge [14]–[16].

Other emerging multilevel inverter topologies include hybrid and/or asymmetric multilevel cells [15], [23], [24], [29], [30]. The hybrid structures join the best characteristics of different power converters to increase the number of levels of the output waveform with the minimum number of switches, capacitors or diodes. These configurations can be derived by combining basic multilevel structures, by using different (asymmetric) DC supplies, or by combining different modulation principles. A drawbacks of these hybrid configurations can be their control complexity.

A Multi-cell Modified Cascade topology [22], [31], [32] and the control strategy based on Selective Harmonic Elimination technique (SHE) [33] are afterwards presented. This topology and control strategy approach will be the basis for the subsequent analysis.

3.4   Neutral Point Clamped (NPC)

The NPC topology for a 3-level inverter is shown in Fig. 3.4a; it can commutate three different voltage values, and has a neutral point at zero voltage that can be connected to the output. The diodes have the function to clamp the voltage, and therefore this inverter is also called Diode-Clamped.

If multiple DC-sources are not available, the dc-bus voltage can be split using series-connected bulk capacitors, and the middle point of the two capacitors can be used as the neutral point. The switch are controlled to achieve three voltage levels: when Q1 and Q2 are ON the voltage $+V_{DC}$ is applied to the output, when Q2 and Q3 are ON the output is zero (neutral point), and when Q3 and Q4 are ON the output is $-V_{DC}$. The switching combinations is given in Table 3.3.
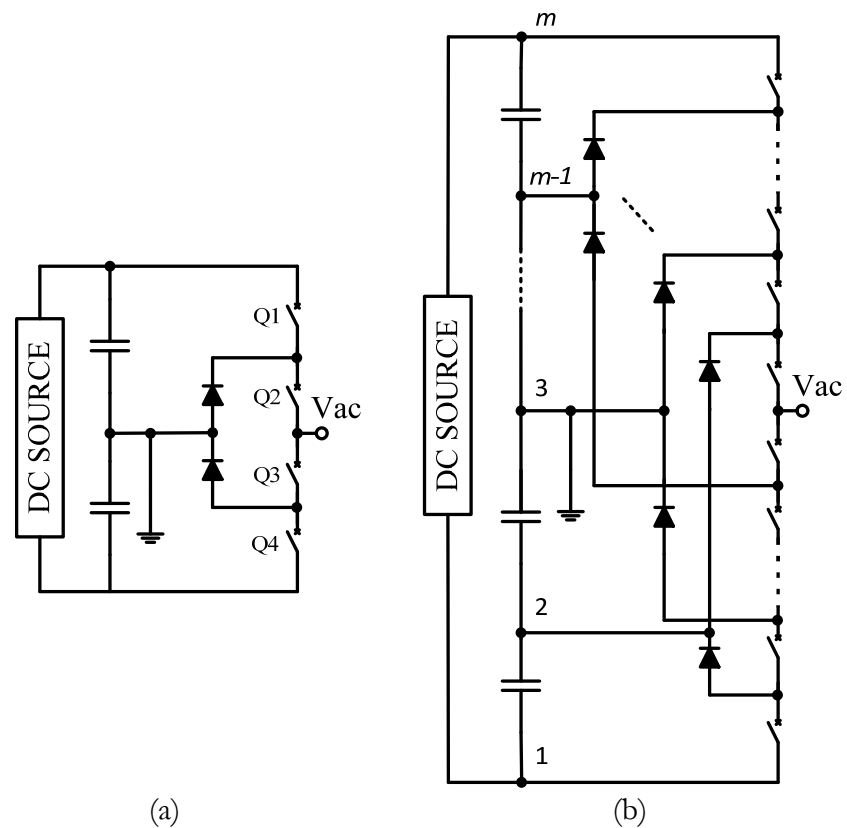
Fig. 3.4 Simplified schematics of single-phase 3-level (a) and *m*-level (b) Neutral Point Clamped Inverter

Table 3.3 Switching states for 3-level Neutral Point Clamped Inverter

Q1	Q2	Q3	Q4	Vac
1	1	0	0	$+V_{DC}/2$
0	1	1	0	0
0	0	1	1	$-V_{DC}/2$

The major benefit of this topology is that each power switch has to stand lower voltages compared to the conventional H-bridge inverter with the same DC bus voltage. In a three level inverter, each switch has to handle only one half of the DC bus voltage. For an *m* level inverter (Fig. 3.4), it is necessary to use *2·(m-1)* switches, which must withstand a voltage equal to a single voltage level, *2·(m-2)* clamping diodes, and *m-1* splitting capacitors if separated sources are not available. The clamping diodes require different blocking voltage rating and therefore, if diodes with the same voltage rating of switches are used, more

diodes must be connected in series and their number rises to *(m-1)·(m-2)*. This makes the implementation unpractical when the number of levels is high [15].

Another problem is that the switches are not evenly used: the internal switches (i.e. the switches close to the output) conduct for longer time than external switches and the difference increases with the number of levels. These drawbacks limit the number of levels in practice to five [34].

As can be observed in Table 3.3 there are only three valid combinations for 3-levels inverter; other permutations lead to undefined output and therefore there are no redundant states, i.e. different switching combinations that lead to the same output level. The control must also ensure that the four switches are never ON at the same time to avoid a short-circuit.

Since the output current provided by each capacitors in unbalanced, this configuration has the necessity to ensure that the voltage is equally distributed in the capacitors. This problem can be solved connecting each capacitor to a separated DC source, or with a feedback control to maintain null the average current in the neutral point [16], [35].

Finally, the structure is not modular: to increase the number of levels it is necessary to reconfigure the entire circuit.

3.5   Flying Capacitor (FC)

The Flying Capacitor (FC) topology, also called also called Capacitor-Clamped, is similar to the previously discussed NPC, except that the clamping diodes are replaced with capacitors that are connected in series with the DC supply to obtain the various levels. The topology for a 3-level capacitor clamped is shown in Fig. 3.5a. The capacitors have the same function of the clamping diodes in the NPC inverter: they lock the voltage between the lines to which they are connected.

The switching combinations is given in Table 3.4. When Q1 and Q2 are ON, the voltage $+V_{DC}$ is applied to the output, whereas when Q3 and Q4 are ON the output is $-V_{DC}$. The zero level is obtained placing into conduction Q1-Q3 (clamped capacitor is charged) or Q2-Q4 (clamped capacitor is

discharged); this allow to alternate the switching combination to balance the charge on the clamped capacitor. To avoid a short-circuit of the source it is not possible to turn ON all the switches at the same time. Moreover, the two internal switches (Q2-Q3) must not be turned ON simultaneously to avoid to short-circuit the capacitor.

A benefit of this topology is the redundant property because there exist more combinations to create the same output voltage. The redundancy can be used as a degrees of freedom for control and optimization purposes, and allow to equally distribute the stresses among the switches [35].

Another benefit of the FC topology is the modularity that allows to easily extended the structure to obtain more output voltage levels. In fact the base cell is constituted by two switches and a capacitor, as can be observed in Fig. 3.5b.
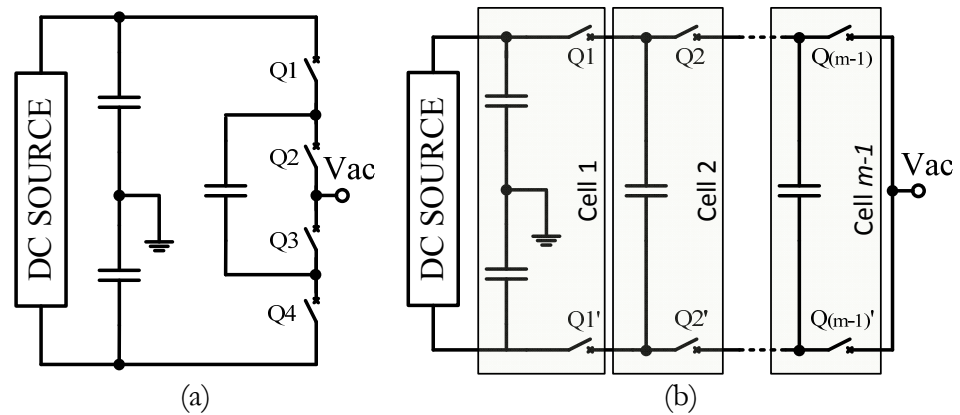
Fig. 3.5 Simplified schematics of single-phase 3-level (a) and *m*-level (b) Flying Capacitor Inverter

Table 3.4 Switching states for 3-level Flying Capacitor Inverter

Q1	Q2	Q3	Q4	Vac
1	1	0	0	$+V_{DC}/2$
1	0	1	0	0
0	1	0	1	0
0	0	1	1	$-V_{DC}/2$

As the Diode-Clamped topology, for an *m* level inverter, it is necessary to use *2·(m-1)* switches. In addition to the *(m-1)* splitting capacitors on the DC-bus, the number of storage capacitors required is *(m-2)*. By using capacitors with the same voltage rating of the switches, *(m-1)(m-2)/2* clamping capacitors are necessary. Since the switching frequency is low (carrier frequency), the high number and value of the capacitors is the major drawback of the inverter.

The inverter control is complicated as capacitors are charged at different values, and the correct sizing of these component results in expensive and bulky systems, because of high voltages across some of the capacitors [16]. In addition, as in the NPC topology, the switches are unevenly used. These problems, along with the problem of initialization of the converter with the correct charge level on the capacitors, has limited the use of this circuit.

3.6 Cascaded H-Bridge

This topology is based on the series connection of single-phase H-Bridge inverters discussed in 3.2, and requires *n* separate DC sources to produce *2n+1* levels in the output voltage. It uses *n* full-bridges connected in series for a total of *4n* switches, as shown in Fig. 3.6. For *n = 1* (3 levels) the structure is a simple H-bridge inverter.

Each bridge can generate three different voltage levels $(+V_{DC}, 0, -V_{DC})$: switches Q1-Q4 are turned ON to obtain $+V_{DC}$, and Q2-Q3 are turned ON to obtain $-V_{DC}$, while by turning ON Q1-Q3 or Q2-Q4 it is possible to achieve a zero output voltage (Table 3.5). Each additional H-bridge inserted into the inverter adds two new levels. The sum of AC output of each bridge produces an output that is a step approximation of a sinusoidal waveform with all voltage levels between $+n·V_{DC}$ and $-n·V_{DC}$ in steps of V_{DC} (Fig. 3.7).

The main advantage of this topology is the modular character that allows higher flexibility and higher reliability [26], whereas the larger number of power switches needed is the main drawback. This is counterbalanced by the fact that, with a high number of levels, it is possible to use switches rated at a lower

blocking voltage. In fact, the higher the number of levels, the lower the voltage that the switches have to handle; this leads to low switching stress and the possibility to use efficient switches rated at a lower voltage. These characteristics allow to use this topology for systems where high power and output voltages are required.
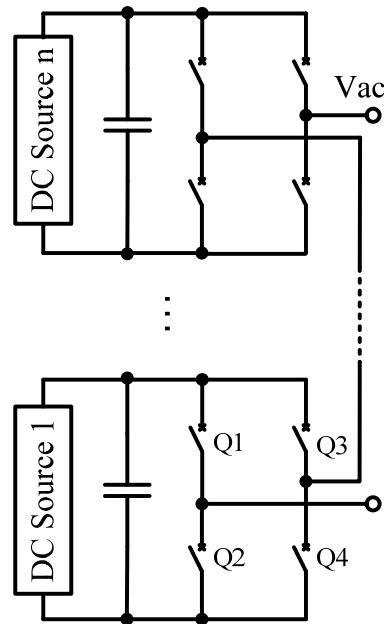
Fig. 3.6 Simplified schematics of single-phase *2n+1* levels Cascaded H-Bridge Inverter

Table 3.5 Switching states for 3-level Cascaded H-Bridge Inverter

Q1	Q2	Q3	Q4	Vac
1	0	0	1	$+V_{DC}$
1	0	1	0	0
0	1	0	1	0
0	1	1	0	$-V_{DC}$

Cascaded multilevel inverters are based on a series connection of several H-bridge modules with the same circuit topology and the same control technique, therefore reducing the costs and increasing the robustness of the system [36]. Each bridge can be controlled independently from the others with

a synchronization between them, therefore the controller structure is simpler than NPC and FC-MLI . In case of fault of a module, it is possible to replace it easily and, with a suitable control strategy, it is possible to bypass the faulty module without stopping the load. Moreover, introducing redundant voltage levels it is possible to keep the inverter operating even with the loss of a DC source or a power semiconductor devices of the H-bridge [26].

With a proper control strategy is possible to equally load all switches and to balance capacitor voltages of the DC sources. However, since the power that flows from the sources have a big oscillatory component, to maintain V_{DC} constant, it is necessary to use large values capacitors.

The DC sources of the various H-bridges must be separated, and therefore this kind of topology is particularly suited for photovoltaic systems where the multiple DC sources can be obtained connecting the proper number of PV modules [37], [38]. When multiple sources are not available it is possible to use a transformer with multiple isolated secondary windings and diode rectifiers.
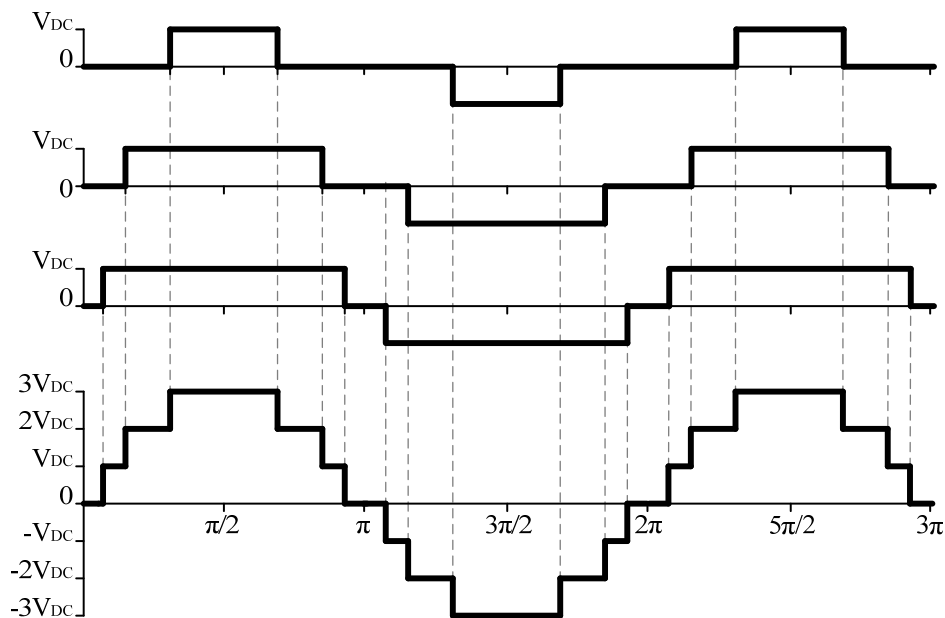
Fig. 3.7 Output voltage waveform of a 7-levels Cascaded H-Bridge Inverter and voltage waveform of each H-bridge

3.7 Multi-cell Modified Cascaded Inverter

One disadvantage of traditional multilevel inverters is the large number of switches needed. Reducing the number of switches is therefore important to reduce the complexity and cut the circuit costs, and may lead to an improvement of the efficiency. The "DC-link" topologies [22] allow to increase the number of voltage levels using few switches; they are based on a positive DC-link stepped voltage and a single-phase inverter.

The Multi-cell Modified Cascaded Inverter is based on the same principle. The structure, shown in Fig. 3.8 for 7-levels and *2n+1* levels, consist in a series connection of conversion cells (DC-blocks) that replace the H-bridge of the cascade configuration. Each DC-block, composed of a controlled switch and a diode, is associated with a DC source. The blocks are connected in cascade to produce an output voltage waveform with several voltage levels and positive polarity. The single H-bridge connected after the DC blocks allows to generate the voltage inversion at the load terminals.

The switching combinations is given in Table 3.6 for a 7-level inverter. With all switches OFF, the voltage produced by the series of the DC blocks is zero. When S1 is ON and S2-S3 are OFF, the first level is obtained, corresponding to an output voltage of $+V_{DC}$. When S1-S2 are switched ON and S3 is OFF, the second voltage level ($+2V_{DC}$) is produced, whereas with all switches ON, the voltage produced by the series is $+3V_{DC}$. The positive waveform produced by the sum of these blocks (DC-link voltage) is cyclically inverted by the H-bridge, which outputs an almost sinusoidal waveform by switching Q1-Q4 ON and Q2-Q3 OFF for the positive half cycle, and Q1-Q4 OFF and Q2-Q3 ON for the negative half cycle.

Fig. 3.9 show the output voltage waveform of each DC-block, the DC-link voltage, and the output voltage of the inverter.

The main advantage of this topology consists of the possibility to obtain the same number of levels of the Cascaded H-bridge structure ($2n+1$), using a reduced number of switches ($n+4$ switches and n diodes). This allows to reduce the cost, the circuit and control complexity and the switching losses. By using a number of switches comparable to that of the Cascaded H-bridge topology, it

is possible to obtain a waveform with an higher number of levels and reduced total harmonic distortion.

As this topology is based on the series connection of several DC-blocks with the same circuit topology, it maintains the characteristic of modularity that allows to easily extend the structure and obtain more output voltage levels.

The diodes in this schematic allow to bypass the DC-blocks when the switches are closed and therefore the relative sources not connected to the H-Bridge. The topology can also be generalized by using MOSFETs instead of diodes in each cell [22], [31], to work with reactive loads. In fact, the diodes do not allow the energy stored in the inductive load to circulate when the switches are closed; this can produce an overvoltage on the output waveform. Replacing the diodes with MOSFETs, the current can flow in the opposite direction even when the switches S1-S2-S3 are OFF, without affecting the output waveform.

In the described configuration, each source has the same voltage value. However, by choosing different voltages for the DC-sources it is possible to increase the number of voltage levels without any additional switch. For example, with a two DC-blocks system with voltages of V_{DC} and $2V_{DC}$, it is possible to obtain 7 level (0, V_{DC}, $2V_{DC}$, $3V_{DC}$ and their negatives).
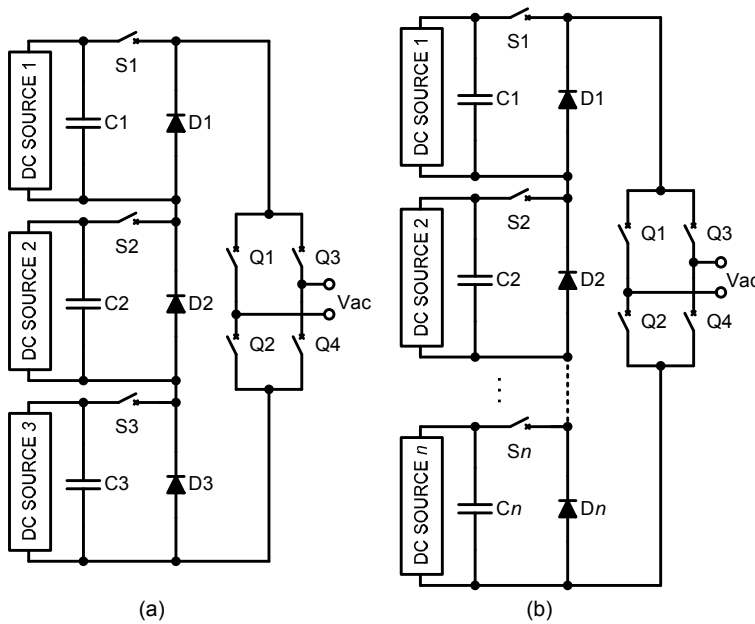
Fig. 3.8 Simplified schematics of single-phase 7-levels (a) and *2n+1* levels (b) Modified Cascaded multilevel Inverter

Table 3.6 Switching states for 7-level Modified Cascaded multilevel Inverter

| Multi-conversion cells | | H-Bridge | | Vac Output |
ON switches	OFF switches	ON switches	OFF switches	
S1, S2, S3	-	Q1, Q4	Q2, Q3	$+3V_{DC}$
S1, S2	S3	Q1, Q4	Q2, Q3	$+2V_{DC}$
S1	S2, S3	Q1, Q4	Q2, Q3	$+V_{DC}$
-	S1, S2, S3	Q1, Q4	Q2, Q3	0
-	S1, S2, S3	Q2, Q3	Q1, Q4	0
S1	S2, S3	Q2, Q3	Q1, Q4	$-V_{DC}$
S1, S2	S3	Q2, Q3	Q1, Q4	$-2V_{DC}$
S1, S2, S3	-	Q2, Q3	Q1, Q4	$-3V_{DC}$
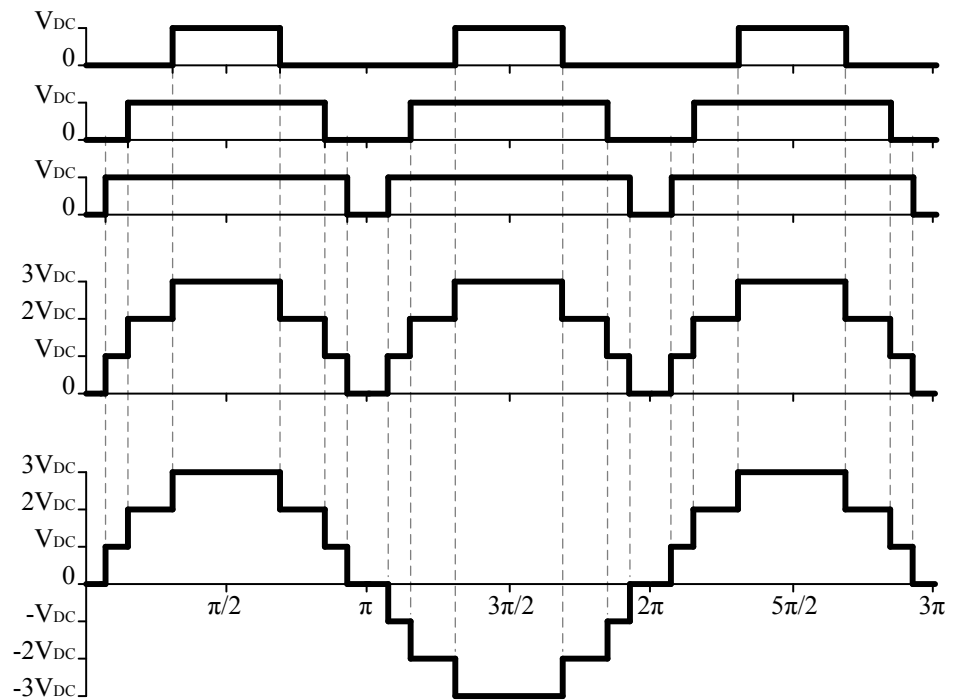
Fig. 3.9 Output voltage waveform of DC-blocks, DC-link voltage, and output voltage of a 7-levels Modified Cascaded multilevel Inverter

3.8 Control strategies for multilevel inverters

There are different modulation techniques that can be used to control a multilevel inverter; they can be classified according to the switching frequency into low and high switching frequency [15].

In low switching frequency techniques, only one or two commutations of the switches are performed during one cycle of the output waveform. They include the Space Vector Control (SVC) and the Selective Harmonic Elimination (SHE) that is one of the most employed techniques and will be discussed in detail.

In high switching frequency techniques, many commutations of the switches are performed during one cycle of the output waveform. They include carrier-based the Sinusoidal PWM (SPWM), the Space Vector Modulation PWM (SVM-PWM), and the Selective Harmonic Elimination PWM (SHE-PWM), a generalized SHE method that switches at higher frequency.

3.8.1 Selective Harmonic Elimination (SHE)

Multilevel inverters switching at the fundamental frequency allow to achieve lower switching losses, and so lead to increased efficiency, but a drawback is that the output waveform has harmonics at frequencies close to the fundamental one that are difficult to filter. The SHE method reduces the total harmonic distortion of the output waveform by cancelling these low frequency harmonics, keeping the efficiency high and allowing to use smaller filters to eliminate the remaining harmonics.

The method, based on the harmonic elimination theory proposed by Patel [39], allows to determine the conducting angles of the switches that minimize the total harmonic distortion of the output waveform, cancelling the predominant low frequency harmonics [26].

Considering a multilevel inverter with n cascaded blocks, the output is a symmetric voltage waveform as in Fig. 3.10. This generalized waveform has no DC component and is an odd function, therefore it does not contain even

harmonics. Using Fourier series expansion, it is possible to express the stepped waveform as the sum of the amplitudes of the odd harmonics:

$$V_{AC}(\omega t) = \frac{4\,V_{DC}}{\pi} \sum_{k=1,3,5,\ldots}^{\infty} (\cos(k\theta_1) + \cdots + \cos(k\theta_n)) \frac{\sin(k\omega t)}{k} \quad (3.1)$$

where n is the number of DC sources, and also the number of switching angles to regulate. The magnitude of the Fourier coefficients of (3.1) are:

$$V_k = \frac{4\,V_{DC}}{k\,\pi}[\cos(k\theta_1) + \cdots + \cos(k\theta_n)], \qquad k = 1,3,5,\ldots \quad (3.2)$$
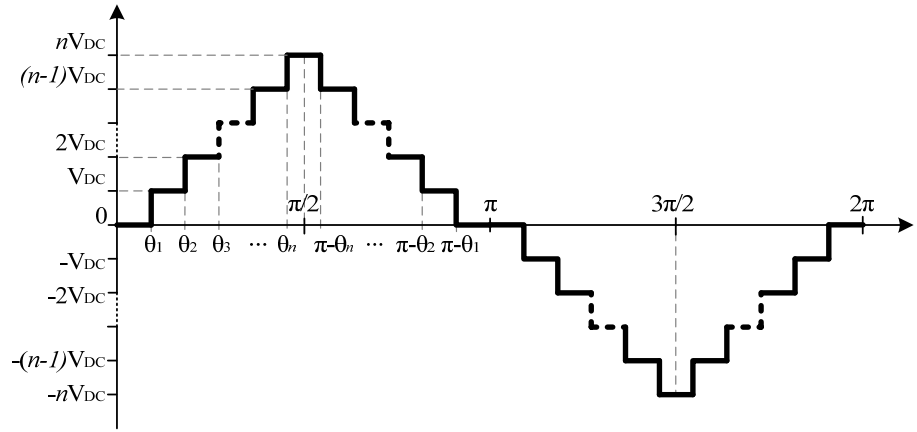
Fig. 3.10 Generalized waveform generated by a multilevel inverter

The conducting angles of the n DC blocks ($\theta_1, \theta_2, \theta_3, \ldots \theta_n$) can be chosen such that the total harmonic distortion is minimum. Generally, the SHE method is used to eliminate the first n odd predominant lower frequency harmonics by choosing the conducting angles, $\theta_1, \theta_2, \ldots \theta_n$, such that $V_K = 0$ (k = 3, 5, …, *2n+1*):

$$\cos(3\theta_1) + \cos(3\theta_2) + \cdots + \cos(3\theta_n) = 0$$
$$\cos(5\theta_1) + \cos(5\theta_2) + \cdots + \cos(5\theta_n) = 0$$
$$\cos(7\theta_1) + \cos(7\theta_2) + \cdots + \cos(7\theta_n) = 0 \qquad\qquad (3.3)$$
$$\ldots$$
$$\cos\big((2n + 1)\theta_1\big) + \cos\big((2n + 1)\theta_2\big) + \cdots + \cos\big((2n + 1)\theta_n\big) = 0$$

with $0 \leq \theta_1 \leq \theta_2 \leq \ldots \leq \theta_n \leq \pi/2$.

Once the DC block number is defined, the set of n nonlinear transcendental equations can be solved by means of numerical techniques, for example the Newton-Raphson iterative method [27], [33].

The SHE technique can be deployed, as shown in [33], for the cancellation of *n-1* harmonics, whereas the remaining degree of freedom is used to adjust the amplitude of the fundamental component. This allows to control the amplitude of the output voltage waveform, and can be useful for controlling the power delivered to the grid in grid-connected systems and to possibly implement an MPPT function.

From the relation (3.2), the maximum voltage of the fundamental component is obtained when all the angles are zero:

$$V_{1,max} = \frac{4nV_{dc}}{\pi} \tag{3.4}$$

The relation between the fundamental voltage (V_1) and the maximum obtainable voltage $(V_{1,max})$ is given by the modulation index:

$$m_I = \frac{V_1}{V_{1,max}} = \frac{V_1}{\frac{4nV_{dc}}{\pi}} \tag{3.5}$$

and the (3.3) can be generalized in:

$$\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_n) = n \cdot m_I$$
$$\cos(3\theta_1) + \cos(3\theta_2) + \cdots + \cos(3\theta_n) = 0$$
$$\cos(5\theta_1) + \cos(5\theta_2) + \cdots + \cos(5\theta_n) = 0 \tag{3.6}$$
$$\cdots$$
$$\cos((2n-1)\theta_1) + \cos((2n-1)\theta_2) + \cdots + \cos((2n-1)\theta_n) = 0.$$

It is worth to note that in a three-phase system, it is not necessary to eliminate triplen harmonics (3rd, 9th, …) because they are automatically eliminated being in phase with each other.

Adding additional voltage levels, allows to have additional free switching angles available to perform harmonic elimination and therefore to achieve lower THD. Fig. 3.11 shows the output voltage waveform that can be obtained applying the basic SHE technique to a 7-level inverter such as the multi-cell modified cascade topology of Fig. 3.8, where θ_1, θ_2, θ_3 represents the turn-on angles of the switches S1-S2-S3.
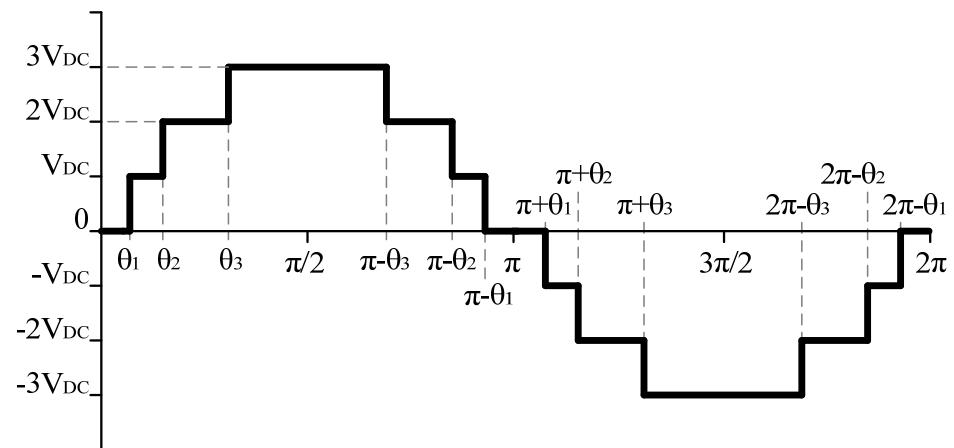
Fig. 3.11 Output voltage waveform for a 7-level inverter with SHE technique

3.9 Electronics components

In the following paragraphs some of the components used in power inverters and in particular capacitors, diodes, and MOSFETs. There will be taken into account the main parameters and the sources of power losses that affect the global efficiency of the inverter.

MOSFET is the devices usually used as switch in low and medium power converter, because they offer several advantages toward bipolar devices. In low frequency application, MOSFET losses are due especially to internal on-resistance, the minimization of which is limited by the design and material and by a trade-off with the breakdown voltage.

In the last decade, new configurations has allowed to significantly reduce a specific on-resistance in silicon MOSFETs. However, as silicon devices approach their theoretical limits, wide band gap semiconductors, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), provide attractive characteristics that allow to dramatically improve performance of power semiconductors. Some of these technologies and materials, which allow to reduce devices losses, will be analysed.

3.9.1 Capacitors

Capacitors allow to store energy, decoupling subsystems, filtering signals, etc., and are therefore essential components of power electronics systems. They are often the weak point and occupy a considerable percentage of the total volume of a converter. The choice of a capacitor reflects a number of constraints related to the waveform and the amplitude of the applied voltage. It is important to take into account the stresses, e.g. voltage magnitude and temperature, that a capacitor has to handle to avoid malfunctioning.

The losses can be classified in:

- ohmic, due to the armatures and connections and that depend on temperature and frequency;

- dielectric, due the conduction in the dielectric, e.g. leakage current, or polarization phenomena; these losses lead to a drift of the capacity.

The electric equivalent model of a real capacitor is shown in Fig. 3.12. It is composed of an ideal capacitor, in series with an inductance ESL (Equivalent Series Inductance) and a resistance ESR (Equivalent Series Resistance) that takes in account the ohmic losses, whereas the resistance in parallel with the capacitor represents the dielectric losses. The ESL is usually significant only at very high frequencies, whereas the ESR is higher at low frequencies and increases also with temperature.

The ESR value depends on the construction method of the capacitor and the insulating material used, and decreases with increasing capacity and working voltage rating.

The power dissipated in a capacitor can be approximated as:

$$P = I_{RMS}{}^2 \cdot ESR. \tag{3.7}$$
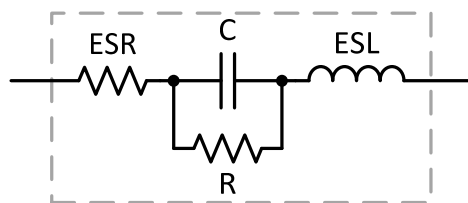
Fig. 3.12 Equivalent electric model of a capacitor

3.9.2 Diodes

The diode is the simplest semiconductor device, made by a P-N junction. It is used in power applications to rectify alternating current, and to provide a unidirectional current paths. The main parameters in power applications are:

- forward voltage (V_F), the voltage drop across the diode when it is forward biased; V_F is a function of temperature and the forward diode current I_F;

- breakdown voltage (V_B), the maximum voltage drop that the diode support in reverse bias before avalanche take place;

- reverse recovery time (t_{RR}), the time required to sweep out the charge Q_{RR} accumulated in forward bias due to excess of minority carriers at the edge of the depletion region, when the diode switch from conducting to blocking state. In this period of time, the diode may conducts in the reverse direction with a reverse recovery current I_{RR}.

The power dissipation in a diode is the sum of three major contribution: conduction (on-state) loss, off-state loss, and switching loss. The conduction loss depends on the forward voltage drop (V_F) and current (I_F), and can be calculated as:

$$P_{on} = \frac{1}{T_{SW}} \int_0^{T_{SW}} v_F(t) \cdot i_F(t) \tag{3.8}$$

For a square waveform it can be approximated to:

$$P_{on} \cong V_F \cdot I_F \cdot T_{ON} \cdot f_{SW}, \tag{3.9}$$

where T_{ON} is the fraction of one period in which the diode is forward biased, and f_{SW} is the switching frequency.

The off-state losses, which are usually negligible, depend on the reverse saturation current I_R and can be approximated to:

$$P_{off} \cong V_R \cdot I_R \cdot T_{OFF} \cdot f_{SW}. \tag{3.10}$$

Switching power losses have two components: loss due to reverse recovery and loss due to forward recovery which can be generally neglected

because much smaller than reverse recovery losses. Therefore switching losses can be calculated as the product of switching energy loss in reverse recovery and operating frequency:

$$P_{sw} = E_{RR} \cdot f_{SW} \qquad (3.11)$$

These losses can reach very high values when operating at high frequency but are not usually relevant at fundamental frequency. Considering a typical switching application, the (3.11) can be approximated with the following equation, that can be solved by knowing the reverse recovery charge Q_{RR} or the maximum reverse recovery current I_{RRM}:

$$P_{sw} \cong Q_{RR} \cdot V_R \cdot f_{SW} \cong \frac{t_{RR} \cdot I_{RRM}}{2} \cdot V_R \cdot f_{SW} \qquad (3.12)$$

Schottky rectifiers are the preferred choice for low voltage switching applications, particularly at high switching frequency. The two key advantages of Schottky diodes respect the conventional P-N diode are the lower forward voltage drop, and the virtual absence of reverse recovery charge. These two fundamental characteristics allow to reduce significantly the conduction and switching losses.

Being an unipolar device (only majority carrier are involved), there is no reverse recovery charge due to minority carrier; the very low switching losses derives only from the small displacement charge of capacitive nature.

However, Schottky diodes have also lower blocking voltage, and higher leakage current that prevent their use in some applications. The maximum voltage rating of commercial Schottky diodes is about 150 V – 200 V, and this has limited their use in power applications. Nevertheless, the use of materials such as Silicon Carbide (SiC) allows to achieve very high breakdown voltage (1200 V or more) while maintain the other advantage of the Schottky design.

3.9.3   Power MOSFETs

Power MOSFETs are the most frequently used switching devices due to their fast switching speed and low gate drive power.

MOSFETs are unipolar devices and therefore current is carried out only by majority carriers, avoiding the minority carrier storage effects of bipolar devices and allowing to reach very high switching speed, limited only by internal parasitic capacitances that must be charged and discharged. Moreover, while bipolar transistors require a large base current, MOSFETs have an high input impedance that allows to drive the gate with very low energy. They can also be easily paralleled thanks to the positive temperature coefficient of the internal resistance that allows to balance currents: the device with the most current heat up, increasing the resistance and reducing the current that therefore will flow to the cooler device, avoiding thermal runaway.

Power MOSFETs usually use a vertical structure made of several cells; the basic schematic of a VDMOS (Vertical Double Diffused MOSFET) cell is shown in Fig. 3.13a. For N-channel MOSFETs, a N- epitaxial layer (drift region) is grown on a N+ substrate (drain), and two diffused layers are produced on it: a P well for the channel, and N+ for the source. The gate, separated by an oxide, is over two adjacent cells. This construction, with Drain and Source terminals on opposite sides, allows to sustain higher current and voltage.

Examining the structure it is possible to notice a parasitic bipolar NPN transistor with the base formed by the P channel. In order to avoid the accidental turn-on of the parasitic transistor, base (P-body) and emitter (N+ source) are short-circuited at the source metallization. This create a parasitic P-N diode between source (anode) and drain (cathode) that limit the reverse voltage that the MOSFET can withstand. Also, a parasitic JFET appears in the region between the two P-body and limits the current flow when the depletion region of the two adjacent P-N junctions extend into the drift region.

The internal on-state resistance $R_{DS(on)}$ is one of the main source of a power losses in MOSFET. It includes several contributions (Fig. 3.13b): source resistance (R_S), channel resistance (R_{CH}), charge accumulation layer resistance (R_A), parasitic JFET resistance (R_J), epitaxial/drift region resistance (R_{EPI}), substrate resistance (R_{SUB}), and resistances of wire bond, metallizations, leadframes, and contact resistances between metallizations and silicon (R_W).

The resistance of the source and channel regions is relevant in low voltage power MOSFET, whereas in higher voltage devices $R_{DS(on)}$ is dominated by the resistance of the epitaxial layer and JFET region due to the higher resistivity in these layers. R_W can be significant in low voltage devices but is generally negligible in high voltage devices.

R_{CH} can be decreased by reducing channel length, or increasing the cells density, especially in low voltage device. In high voltage devices cell density is not so relevant because R_{CH} contribute to $R_{DS(on)}$ is small and moreover the distance between two cells must be enough to avoid the effect of parasitic JFET. An increased doping of P well help to reduce the channel length at the cost of higher threshold voltages.
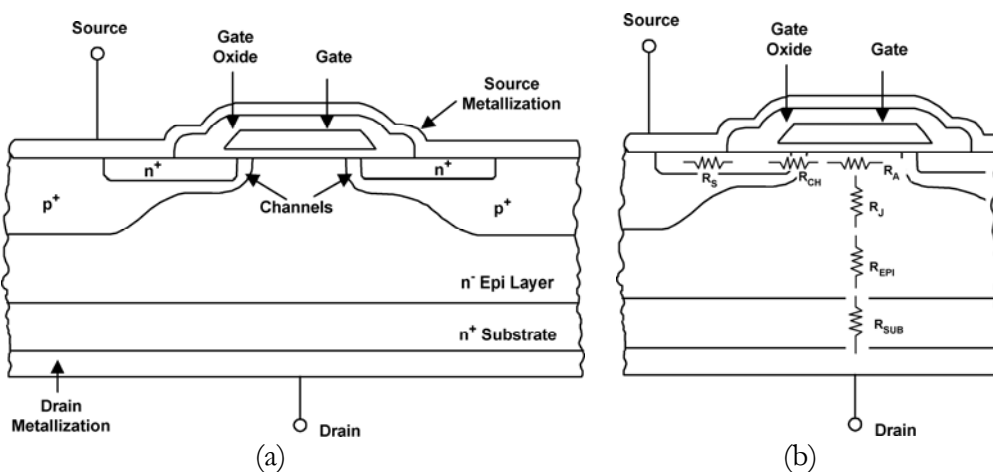
Fig. 3.13 Section of a VDMOS cell (a), and contribution of the different layers to the on-state resistance (b).

The ability of the power MOSFET to handle high reverse voltages is given by the breakdown voltage of the body-drift diode; when the diode breaks down high currents flow between source and drain with no bias applied to the gate, and the avalanche multiplication process could destroy the device.

As breakdown voltage is strongly dependent on the thickness and the doping of the low doped N- epitaxial region, there is a trade-off between $R_{DS(on)}$ and breakdown voltage. A thicker and lightly doped epitaxial layer allows to support higher breakdown voltage but results in a higher on-resistance. The silicon resistance per unit area in the drift zone has been found to be $R = 8.2 \times 10^{-9} \, V_{DSS}^{2.5}$ [40].

The switching performances of a MOSFET are determined by the time necessary to reach voltage values across input (Ciss), output (Coss) and reverse transfer (Crss) capacitances. Also the gate resistance and the parasitic inductances affect the switching performance.

3.9.3.1 MOSFETs power losses

The power loss in a MOSFET is the sum of the power loss in the on-state, and during turn-on and turn-off. Gate losses and off-state losses can normally be neglected.

The conduction losses depend on the internal on-state resistance $R_{DS(on)}$:

$$P_{con} = \frac{1}{T_{SW}} \int_0^{T_{SW}} R_{DS(on)} \cdot i_D^2(t) \, dt = R_{DS(on)} \cdot I_{Drms}^2 \qquad (3.13)$$

where I_D is the source-drain current and T_{SW} is the switching period. At low frequencies these losses are the main contribute to the total power loss, and therefore the choice of components with low $R_{DS(on)}$ is crucial to minimize the losses.

During the switching transitions both voltage and current are not null and this yields to power loss; the switching losses can be calculated from the general expression:

$$P_{sw} = E_{sw} \cdot f_{sw} = f_{sw} \int_0^{T_{SW}} v_{DS}(t) \cdot i_D(t) \, dt \qquad (3.14)$$

The switching losses can be approximated with the following equation by using a triangular approximation for the product of voltage and current. Moreover, there are losses associated to the charge stored in the C_{OSS} of the MOSFET. The total switching power loss can therefore be roughly approximated with:

$$P_{sw} = \frac{V_{DS} \cdot I_D}{2} \left(t_{on} + t_{off} \right) \cdot f_{sw} + C_{oss} \cdot V_{DS}^2 \cdot f_{SW} \qquad (3.15)$$

It is possible to minimize these losses by reducing the switching times that depend on the parasitic capacitance of the device and the voltage and current used to drive the MOSFET gate.

The intrinsic body diode of the MOSFET is a relevant source of losses because it is usually very slow. To maintain high the efficiency at high

switching frequency can be necessary to bypass the body diode with an external circuitry.

The losses associated with the gate driver circuit that charges and discharges the MOSFET gate with a charge Q_G are:

$$P = Q_G \cdot V_{GS} \cdot f_{SW}. \tag{3.16}$$

3.9.3.2 Power MOSFET thermal model

When the charge carriers, accelerated by the electric field, move through the device, their interactions with atomic lattice releases heat that affects the electronic transport properties of the material. Electrons can scatter with each other, with phonons (quantized lattice vibrations), with material interfaces, imperfections and impurities. The heating is due to electron–phonon scattering through the Joule heating mechanism. Other scattering mechanisms do not affect the energy, e.g. the electron–electron interaction redistributes the energy among the electron population, and electron-impurity scattering only affects the momentum [41].

In a traditional semiconductor device, the heating rate per volume can be expressed with the following simplified model [42]:

$$H = \boldsymbol{J} \cdot \boldsymbol{E} + (R - G)(E_G + 3k_B T). \tag{3.17}$$

The first term, which is the dot product of the local electric field E and the current density J, represents the Joule heating and is the power loss in a conductor caused by the electrical resistance. The second term represents the heating due to non-radiative recombination of carriers; R and G are respectively the recombination and generation of electron-hole couples, E_G is the energy band gap, k_B the Boltzmann constant and T the lattice temperature.

Joule heating is the main source of heat generation in MOSFETs as they are majority carrier devices and there is a limited carrier recombination. Instead, in bipolar devices (e.g. P-N diode, bipolar transistor) recombination heat generation cannot be neglected due to minority carrier injection [43].

Equation (3.17) may include higher order terms accounting for a non-constant temperature distribution and variations of the band edges [42].

This model however does not take into account microscopic thermal non-equilibrium due to different energy of vibrational modes. In silicon, electrons with energies below 50-60 meV scatter mainly with acoustic phonons, whereas those with higher energy scatter with the optical modes. High-energy optical phonons have low group velocities and thus do not contribute significantly in heat transport. They instead transfer their energy to the faster acoustic phonons, which diffuse heat. However, the energy transfer between phonons is slower than that from electrons to optical phonons; optical phonons are not able to transfer their energy to acoustic phonons fast enough and this can lead to thermal non-equilibrium. Under high fields, the optical phonons build up over time, causing a higher rate of interaction with electrons, which leads to more scattering events that affect electron transport and reduce the drain current [41], [44].

The classic formulation of the Joule heating does not give a microscopic picture of the heating, and not differentiate the electron energy exchange with the various phonon modes. Therefore electron-lattice scattering and the phonon simulation models have been introduced. These models shown significant differences respect the Joule heating model on short time and nanometers scales but they are almost equivalent under steady-state equilibrium conditions [44].

Equation (3.17) suggests that the peak of heat generation in MOSFETs is where the product of the field and current density is largest. The region where this happen can be different among the various devices structures because current conduction mechanisms and field distribution are different. The main location of heat generation in MOSFETs is usually in the channel region close to drain, which is the region with the highest electric field.

In VDMOS the heat generation has a peak below the gate, in the low doping drift region near the source side, due to the high current density. In other structure, e.g. super-junction (cf. paragraph 3.9.4.1), the heat-generation distribution is different; the current density is more uniform along the structure and the maximum heat generation takes place basically at the bottom of the drift region where the electric field is maximum [45].

Devices have a maximum "junction" (i.e. the area near the channel where the heat generation is maximum) temperature ($T_{J(max)}$), and their electrical characteristics are function of the junction temperature. Self-heating causes a temperature rise that affects the performance and reliability of the devices; therefore a device must always work within its maximum specifications. A steady-state thermal model of a device and its electrical analogue are shown in Fig. 3.14. The heat generated at the junction flows through the substrate and the device package to the heat sink. The temperature increase above the ambient temperature is proportional to this heat flow and the thermal resistance $R_{\theta,J-A}$ between the junction and the ambient.

$$R_{\theta,J-A} = \frac{T_J - T_A}{P}. \tag{3.18}$$

$R_{\theta,J-A}$ is the sum of thermal resistances along the thermal path: $R_{\theta,J-C}$ (junction to case), $R_{\theta,C-A}$ (case to ambient), $R_{\theta,C-H}$ (case to heat-sink), $R_{\theta,H-A}$ (heat-sink to air). The total $R_{\theta,J-A}$ is given by the (3.19), or merely the (3.20) when no heat-sink is used.

$$R_{\theta,J-A} = R_{\theta,J-C} + \frac{R_{\theta,C-A}\left(R_{\theta,C-H} + R_{\theta,H-A}\right)}{R_{\theta,C-A} + R_{\theta,C-H} + R_{\theta,H-A}}, \tag{3.19}$$

$$R_{\theta,J-A} = R_{\theta,J-C} + R_{\theta,C-A}. \tag{3.20}$$

The $R_{\theta,C-A}$ can be neglected when its value is considerably higher than $R_{\theta,H-A}$, and the (3.19) becomes:

$$R_{\theta,J-A} = R_{\theta,J-C} + R_{\theta,C-H} + R_{\theta,H-A}. \tag{3.21}$$
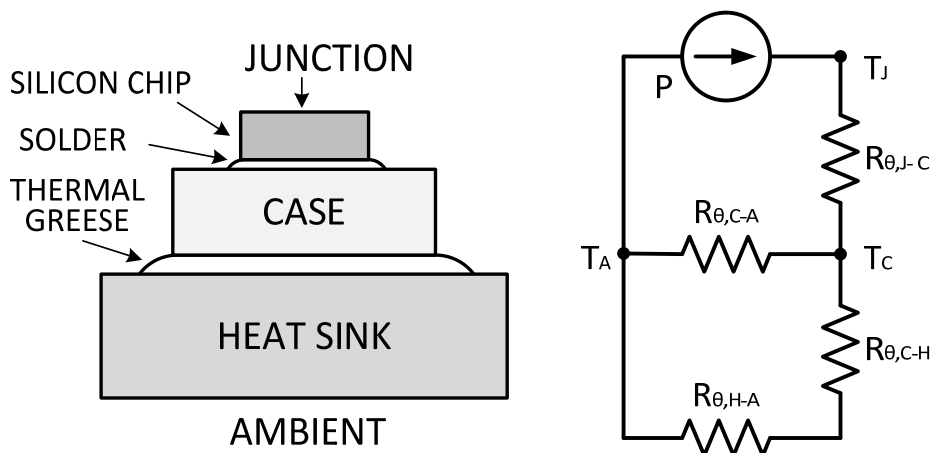
Fig. 3.14 Steady-state thermal model of a device and electrical equivalent circuit

$R_{\theta J-C}$ is the internal thermal resistance and is constituted by the thermal resistance of the semiconductor, the metal and the contact between them. The thermal resistance across a layer of thickness *d* and area *A* is equal to *d/(k·A)*, where *k* is the thermal conductivity of the material ($k \approx 170$ W·m⁻¹K⁻¹ in silicon, and 240 W·m⁻¹K⁻¹ in aluminium) and is a function of the temperature. The thermal resistances relative to the package usually dominates heat conduction in modern transistors.

3.9.4 Technologies and materials to reduce losses

Silicon industry has growth tremendously over the years, and significant developments have been achieved allowing to improve performance and characteristics of the devices. In many applications, above all those of power electronics, the developments of new technologies or materials is fundamental to overcome the physical limits of silicon.

As seen in the previous paragraph, the reduction of specific on-resistance in power MOSFET is limited by material and breakdown voltage, and requires a thick and lowly doped epitaxial layer. In the last few years, technologies, e.g. super-junction, have allowed to overcome the silicon limits and significantly increase efficiency of low and medium voltage power devices. A further step in conversion efficiency will be achieved by using semiconductors with large prohibited energy gap, above all Silicon Carbide (SiC) and Gallium Nitride (GaN).

Fig. 3.15 shows the 2015 technology positioning forecast of the advanced power devices for different uses and market segment, considering material properties, cost, and availability [46]. SiC will be the predominant material for high voltage applications, whereas GaN will be used mainly for low voltage applications, but devices with higher voltage rating are expected in future. Super-junction silicon MOSFET dominates the medium voltage applications, whereas silicon IGBT use is restricted in the low-end market.

3.9.4.1   *Trench and Super-junction MOSFETs*

In planar low voltage power MOSFETs $R_{DS(on)}$ is set primarily by the channel resistance, the access resistance, and the presence of parasitic JFET that limits the current when cells are too close and does not allow to increase the cells density. Trench power MOSFETs (Fig. 3.16a) have a vertical gate buried inside the structure; this allow to create a vertical channel that avoids any access resistance and remove the JFET. Therefore this technology reduce $R_{DS(on)}$ and allows higher cell density.

For a high voltage power MOSFET, the on-resistance is tied to the capability to sustaining high reverse voltage. In fact, in conventional power MOSFETs, the voltage blocking capability is achieved through the combination of light doping and a thick epitaxial region, resulting in very high resistances in the drain region. The on-resistance increases exponentially with the light doping and the thick drift layer that are required to achieve high breakdown voltage. The resistance in the drift region represents the major contribution to on-resistance of high-voltage MOSFETs and can reach 95% of the total device resistance [47].

A relatively new technology called super-junction (SJ) allows to greatly reduce the epitaxial zone resistance compared to the conventional VDMOS, while maintaining same level of breakdown voltage [48], [49]. The SJ concept, shown in Fig. 3.16b, is based on two key principles: a heavily doped current path, and a junction charge-balance principle. The current path is more heavily doped than conventional power MOSFET, and this allows to reduce the on-state resistance. However, without the p-columns the highly doped n-region would yield to a much lower blocking voltage capability. The p-columns constitute a charge-compensation structure that spreads the electrical field and helps electrons through the drift region. During the off-state, the columns create a lateral depleted region that spreads into the drift zone and compensates the vertical depletion charge, keeping the blocking voltage capability. There is a tridimensional distribution of the charges and the resistivity in the drift layer is no longer tied to $V_{DSS}^{2.5}$.

This technology allows to reduce the $R_{DS(on)}$ of high voltage MOSFETs by a factor of five, making possible to broke the silicon limit line which

previously has been a barrier to performance improvements in power MOSFETs. The reduction of area specific resistance, and the consequent reduction of the chip size has also positive effects on the device parasitic capacitances, and therefore yields to a reduction of the switching losses.

The SJ concepts have been successfully implemented in commercial devices such as the CoolMOS (Infineon) and the MDmesh (ST-Microelectronics); the latest generation of SJ devices has further reduced the area specific $R_{DS(on)}$ below $1 \ \Omega \cdot mm^2$ [47]. Fig. 3.17 shows the intrinsic resistance versus the blocking voltage for a conventional MOSFET and various generation of SJ CoolMOS devices.
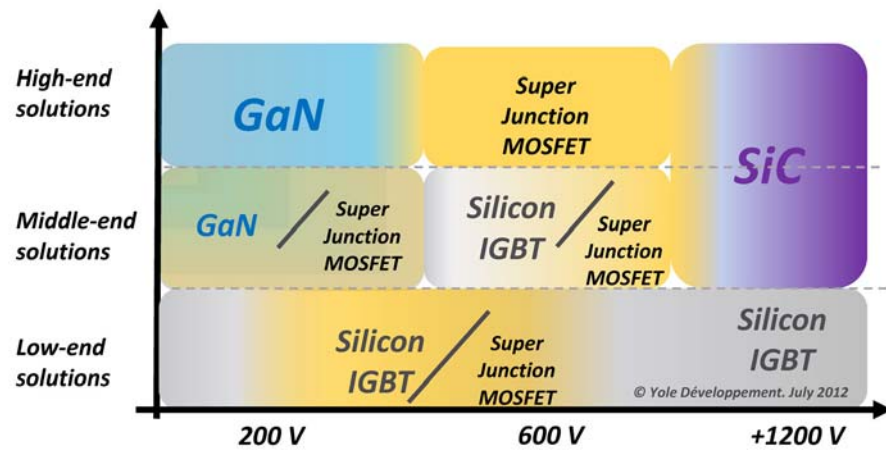
Fig. 3.15 2015 Technology positioning forecast [46]

(a)   (b)
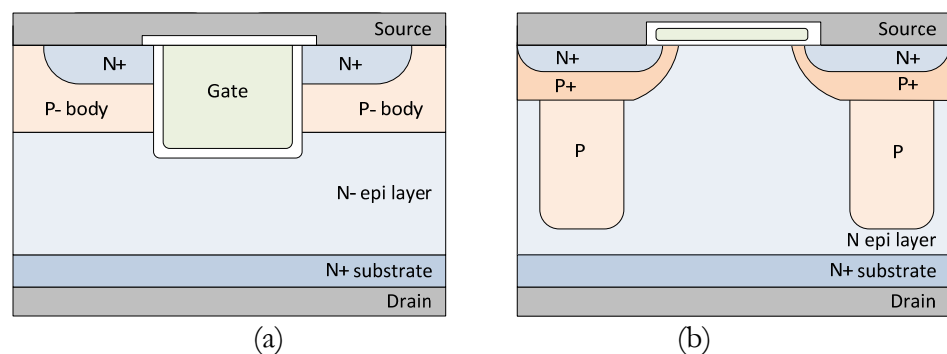
Fig. 3.16 Schematic structure of a Trench MOSFET (a), and Super-junction MOSFET (b)
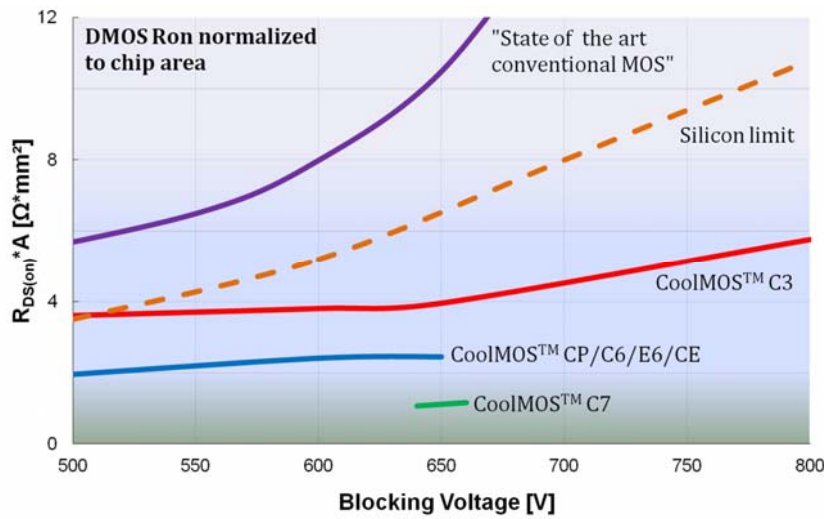
Fig. 3.17 Area specific $R_{DS(on)}$ versus blocking voltage capabilities of conventional MOSFET and CoolMOS generations [47]

3.9.4.2 Silicon Carbide and Gallium Nitride

Silicon Carbide (SiC) and Gallium Nitride (GaN) are wide bandgap materials with high thermal conductivity and current density that make them promising for the realization of power devices.

Silicon carbide was one of the first semiconductors discovered (1824), but only recently, thanks to progress in manufacturing techniques, devices based on it were made available on the market, initially in the form of Schottky diodes, and more recently as JFET and MOSFET. These devices allow to overcome the physical limitation of silicon, improving the overall performance of the system and expanding fields of applications.

SiC is available in various structures; the three most common polytypes are: 3C-SiC, 6H-SiC and 4H-SiC [40] with different electric characteristics. Table 3.7 reports the main properties for semiconductor devices performance. The main advantages of SiC versus silicon are:

- Large energy band-gap (E_g), which allows the devices to operate at high temperature, and in optical applications for low wavelength emitters/receivers.

- Large breakdown electric field (E_c), which allows the realization of devices with higher voltage rating then silicon and with thin drift layer and therefore lower on-resistance.

- High thermal conductivity (λ_{th}), which allows to transfer the heat much more effectively and therefore reduces the dissipation requirement.

- High saturation speed of the carriers (v_{sat}), which allows to operate at very high frequencies.

SiC allows to realize devices with better characteristics in a fraction of the space required for an equivalent silicon device. A SiC MOSFET allows to achieve all the advantages typical of the MOSFET compared to a bipolar device but with lower on-resistance and higher voltage rating (>1200 V). For the diodes, the use of SiC to realize Schottky rectifiers allows to overcome their problem of low breakdown voltage while maintain the advantages of the Schottky design.

The major limit of this material is the high production cost of the wafers, that are only available with low diameter and have an higher defect density, and therefore lower yields, compared to silicon.

Gallium Nitride devices are an alternative to silicon for low and medium voltage applications (200 V – 600 V range), but devices with higher blocking are expected to be available in future [50]. GaN offers advantage similar to SiC in many aspects, but the lack of substrates of sufficient size and quality has prevented its success on the mass market. Bulk GaN substrates are excessively high-priced, requiring the use hetero-epitaxial films on other substrates (SiC, sapphire) which are also expensive. However, recent developments have allowed GaN devices to be built on silicon substrates overcoming the problems of lattice and thermal expansion coefficients mismatch. This has allowed to reduce costs but worsening some of the benefit of the material, e.g. the thermal conductivity is limited by the silicon substrate. Also, the lack of good quality substrates prevent its use in vertical devices. The basic GaN-on-Si device structure is a HEMT (High Electron Mobility Transistor).

At the moment, SiC is more commercially mature than GaN and have conquered a not negligible market, whereas GaN devices are used in very few

applications. However GaN power devices have the potential to provide great reduction of both conduction and switching losses with costs much lower than SiC [51]. The Fig. 3.18 shows a comparison of specific on-resistance vs breakdown voltage for various devices technologies and materials.

Table 3.7 Comparison of the main physical properties for components performances for Silicon, SiC polytypes and GaN

	Si	3C-SiC	6H-SiC	4H-SiC	GaN
E_g (eV) forbidden bandwidth	1.12	2.2	3.02	3.26	3.39
E_c (MV/cm) breakdown electric field	0.28	1.5	2.2	2.2	5
v_{sat} ($\times 10^7$ cm/s) carriers saturation speed	1	2.5	2	2.2	2
λ_{th} (W/cm.K) thermal conductivity	1.5	4.9	4.9	4.9	1.5 [1]

[1] Typical value for GaN-on-Si; bulk GaN could reach 4 W/cm.K
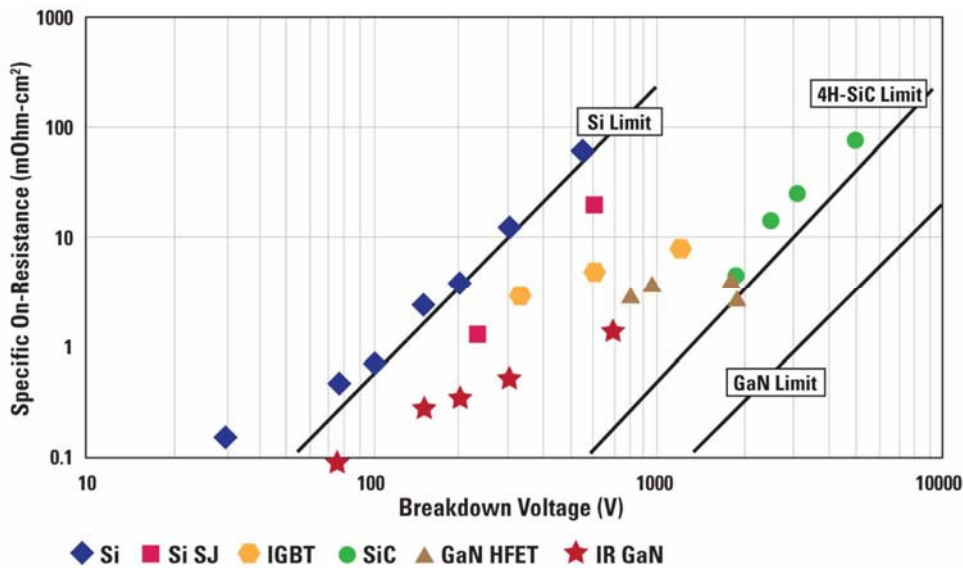
Fig. 3.18 Specific on-resistance vs breakdown voltage for different devices technologies and materials

4 Power Measurements

The precise measurement of the power dissipated by a semiconductor device is of great importance for assessing system performance and reliability, and to evaluate the overall efficiency of a power electronics systems. Efficiency measurement can be difficult when the device is highly efficient and the power losses are extremely low. Measurement errors can be introduced due to high frequency components in the waveforms. In this chapter is presented a calorimetric method based on a micro-machined dual-sensor heat-flux measurement device that allows the estimation of the power dissipated by a semiconductor device. The system uses a thermoelectric heat pump to keep the switching device at room temperature in order to minimise the heat exchanged with the ambient and improve the precision of the measurement.

4.1 Introduction

The measurement of power losses with high accuracy is important to evaluate the performance of electronic systems, to establish the overall power loss or conversion efficiency, and to optimize the design of a circuit. The increasing efficiency and operating frequencies of semiconductor devices brings up the problem of the precise measurement of the power dissipated by these devices. Efficiency measurements on high performance systems become increasingly difficult as the converter efficiency rises.

Power loss measurement techniques include electrical methods and calorimetric methods. The electrical measurement of the power loss is based on the product of voltage and current. The electrical method is easy to perform and achievable with good precision for DC and low-frequency AC devices by using analog electronic equipment. However the instruments at the base of this method are limited by the bandwidth and the dynamic frequency response,

therefore these methods are not suitable for high frequency and highly distorted signals.

On the other hand, conversion circuits will operate at higher and higher frequencies. Transistors in materials like SiC or GaN, are considered among the best alternatives to increase inverter efficiency thanks to their low conduction and switching losses. These devices can switch at very high frequencies to save further costs by getting smaller dimension and easy filtering.

For high-frequency switching devices, the electrical method is often subject to large errors due to the distorted signals, and the accuracy of digital instruments is also affected by the probes delays, phase shifts between sampling channels of digitizer, sampling errors and non-linearities of A/D converter [52]. Other errors are associated with the noise introduced by signal with high di/dt and dv/dt.

Determining the power loss though the measurement of the input and output power can lead to additional errors associated to the subtraction of two comparable values. The error in the measurement of the power loss in a power converter is the sum of the errors in the measurements of input and the output power. As the efficiency rises, the error increases; even a low error in the measurement of current and voltage can produce an high error in the calculation of the power loss [52].

As the total power losses are dissipated as heat, it is possible to calculate the power dissipated by a device by measuring its heat produced. It is therefore possible to archive measurements with acceptable precision, without the use of expensive digital instruments.

The calorimetric method allows a measurement of the power loss which the device dissipates as heat. This method allows to measure the power losses under normal operating conditions independently from electrical quantities of the device under test (DUT). The measurement is effective for very fast signals, is not affected by phase shifts between voltage and current, and is almost immune to electromagnetic RFI/EMI disturbances.

The method presented here is based on a heat-flux measurement sensor, made with two micro-machined temperature sensors, coupled with a readout

circuit, that allows the characterization of the losses in a power semiconductor device. The micro-device could be in principle integrated into the device package to allow the continuous monitoring of the dissipated power.

4.2 Calorimetric methods

The calorimetric method allows to measure the power loss which a DUT dissipates as heat. It has been previously proposed as an accurate method to measure the power loss in high efficient converters, where the measurement with digital instruments can lead to non-accurate results due to high frequency components in the input/output waveform.

Various kind of calorimetric apparatus have been developed, and an overview is given in [52]–[54]. These methods are widely used for the measurement of the power dissipated by large machines and magnetic components. Errors are possible due to the non-perfect thermal isolation from the ambient, and moreover the measurements are limited to steady states and are time-consuming.

4.2.1 Calorimetric methods based on heat flux sensor

Among the numerous calorimeters presented in literature, a simple apparatus for total loss measurement is the calorimeter based on a heat-flux sensor [55], [56]. The heat-flux sensor is embedded into a pedestal on which the DUT is mounted and there is a cooled base plate that serves as the heat exchanger (Fig. 4.1). The heat passing through the sensor generates a temperature difference between the two sides of the sensor which is proportional to the heat flux through the sensor itself, and therefore to the power dissipated by the device. The system is designed such that almost all the heat generated by the DUT passes through the heat flux sensor. To minimize heat loss by convection the apparatus is enclosed in a evacuated aluminium chamber, and the surfaces are polished to minimize the radiation heat loss. This set-up can archive accuracies within 5% [55].
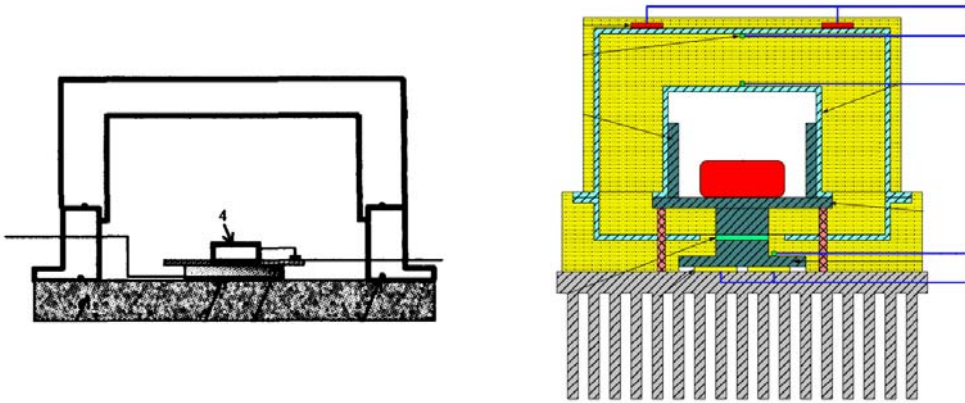
Fig. 4.1 Typical calorimetric apparatus based on a heat-flux sensor [55], [56]

4.3 Heat-Flux sensors

The heat-flux is the heat transfer per unit area (W/m^2). Different kinds of heat-flux sensors have been developed and most of the methods for measuring heat flux are based on measurements of the temperature on the surfaces of a material [57].

Energy transfer by conduction, which involves heat transfer by electrons and phonons, is related to the temperature distribution by Fourier's law, which states that the heat flux is equal to the product of the thermal conductivity k and the negative temperature gradient:

$$\vec{q}'' = -k\,\vec{\nabla}T. \tag{4.1}$$

Considering a heat flux that flows perpendicular to the surface of a layer of thickness δ and thermal conductivity k (Fig. 4.2), in steady-state one-dimensional condition, the heat transfer by conduction is linear [57] and the (4.1) become:

$$q'' = k\frac{(T1-T2)}{\delta}, \tag{4.2}$$

where T_1 and T_2 are the temperatures at each side of the layer. Therefore it is possible to estimate the heat flux that flows the sensor measuring the temperature difference between the two sides of the substrate.
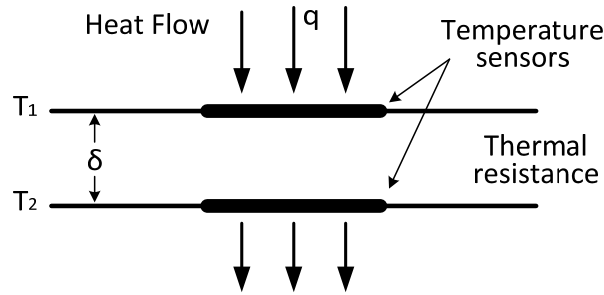
Fig. 4.2 Heat-flux sensor working principle

The temperature difference can be measured in many ways, e.g. thermocouples and RTDs (Resistance Temperature Detectors). Thermocouples generate an output voltage that corresponds to the temperature difference between two junctions; they can be put in series to achieve a larger output signal and increase the sensitivity. By using metal RTDs, two individual temperature readings are required; they allow to know the individual temperatures rather than the difference and the time response of the sensor can be analytically enhanced [57]. As the thickness of the sensor δ and thermal conductivity k are not known with sufficient accuracy, it is usually necessary a calibration procedure to determine the heat flux.

4.4 Experimental calorimetric setup based on Heat flux sensor

The proposed apparatus, which is shown in Fig. 4.3, uses a thermoelectric module (Peltier) to absorb the heat generated by the DUT, e.g. a power MOSFET, and keep the device package at the same temperature of the surrounding air, minimizing the heat exchanged with the environment. When the DUT is in thermal equilibrium with air, there is virtually no heat exchange (cf. paragraph 3.9.3.2).

The heat-flux sensor is positioned between the DUT and the thermoelectric module, so the heat generated by the device is forced to flow

through the flux sensor to the Peltier element. Two heat spreader made of copper were used to distribute the heat uniformly.

4.4.1 The Heat-flux sensor

A heat-flux sensor has been realized to allow the measurement of the heat flux generated by the power semiconductor device; the sensor is based on two stacked RTDs that measure temperature difference across a substrate.

We used two stacked temperature sensors separated by a layer of alumina (aluminium oxide) that has been chosen because it has a good thermal conductivity and it is an electrical insulator. By changing material and thickness of the thermal resistive layer between the two RTDs, it is possible to control the sensitivity of the sensor. One advantage of that implementation of the sensor, over that based on thermocouples, is that it allows to know individual temperatures rather than the temperature difference [57].

The two resistive temperature sensors have been realized with micro-fabrication techniques at the DIMES Technology Centre, TU DELFT. Each sensor is realized on a p-type Silicon wafer with the design shown in Fig. 4.4. A thin layer of silicon nitride has been used for isolation and the capping layer; the metal which implements the thermo-resistance is a 1.4-μm-thick aluminium film. The overall dimension of a sensor is $6 \times 3 \times 0.5$ mm, and it has four contacts that make possible the use of the 4-wire resistance measurement technique. The RTDs have a resistance of 3 ± 0.1 Ω at 25 °C and the resistance vs. temperature curve is displayed in Fig. 4.5. In Fig. 4.6 we reported the dynamic response of the sensors cooling-down the thermo-resistance by applying a current that varies from 250mA to 10mA; the time constant is about 4 μs.
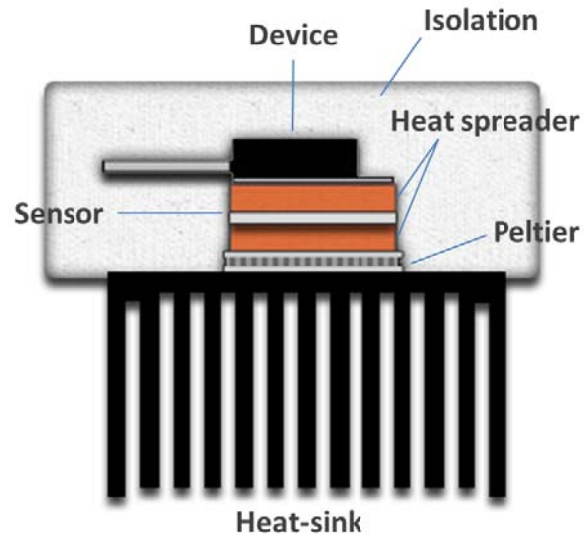
Fig. 4.3 The proposed calorimetric apparatus

(a)   (b)
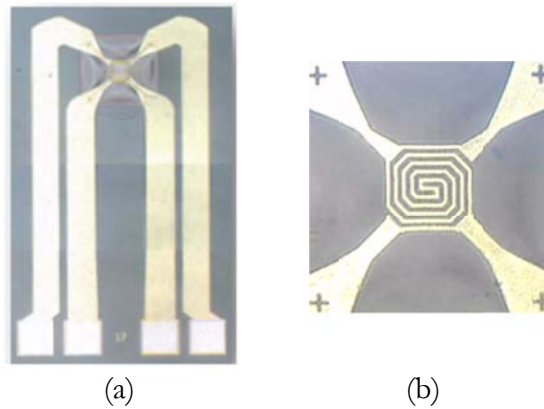
Fig. 4.4 Picture of a micro-fabricated RTD sensor: a) entire sensor, b) detail of the coil
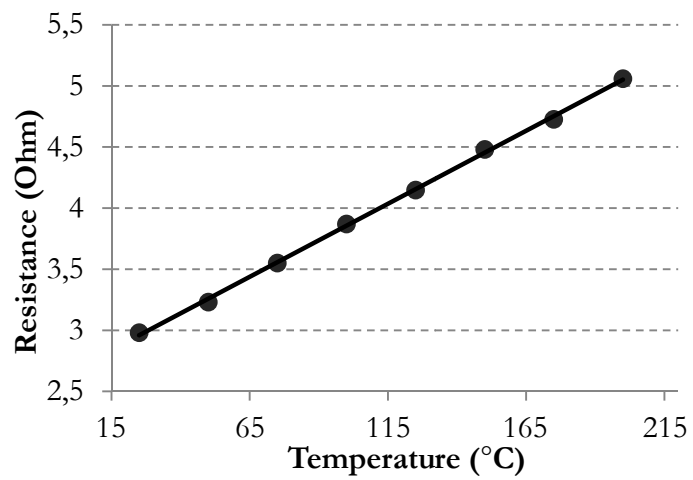
Fig. 4.5 Resistance vs. Temperature curves of a micro-fabricated RTD sensor
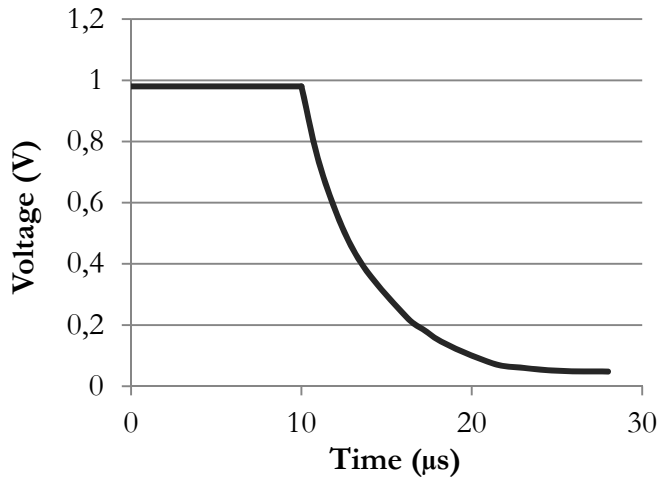
Fig. 4.6 Dynamic response of a micro-fabricated RTD sensor

4.4.2 Working principle of the apparatus

By using the thermoelectric module, it is possible to absorb the heat generated by the device and regulate the temperature of its package, keeping its mean value at the same value of air temperature, minimizing therefore the heat transfer by convection in the air. Furthermore, to minimize the heat leakage, the apparatus has been isolated from the ambient using polystyrene layers, whereas small diameter wires have been used to minimize the heat loss through the leads. In fact, part of the heat is lost by conduction through the leads of the device or the sensor's wires. The heat loss through the wires increases with their diameter and length [56].

The losses are determined in two steps: an initial calibration test and the main test. In the first step, we measured the heat flux produced by the device in DC operation, when the power dissipated by the device can be measured with higher precision. Later the power lost is computed for arbitrary electrical signals through an interpolation on the basis of the calibration data.

To acquire the sensor's signals we realized a board (Fig. 4.7) with a microcontroller, an analog conditioning circuit, and a 24-bit analog to digital converter to acquire the temperatures of the two RTD sensors. Other analog and digital temperature sensors are used to monitor the package and ambient temperature. The microcontroller reads the measurement, communicates via USB with a PC software expressly developed, and implements a digital PID

control to adjust the bias of the Peltier cell and archive the required temperature regulation of the DUT. When the temperature of the DUT package matches the ambient temperature, it is possible to take the measurement $\Delta T = T_1 - T_2$ from the sensors positioned between the DUT and the thermoelectric module. This difference is proportional to the heat-flux and the dissipated power.

Fig. 4.8 shows some images of the realized apparatus, the sensor and the PC readout software.
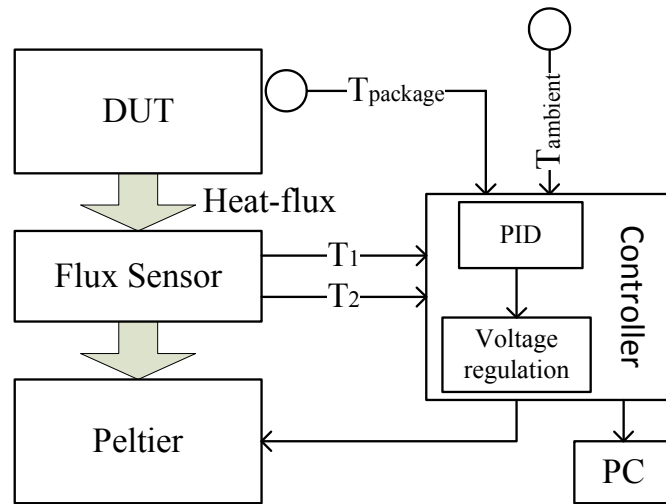
Fig. 4.7 Schematic of the proposed calorimetric apparatus and control system

4.4.3 Measurement and Results

Finite element thermal simulations were performed to theoretically study the temperature profile along the thermal path with heat sources of different values. We used the model of heat transfer in solid with the structure in Fig. 4.9. It is composed of two silicon substrates (163 $W \cdot m^{-1} \cdot K^{-1}$, 0.5 mm thick) which represent the sensors; they are separated by alumina layers (Al_2O_3 alpha, 1 mm thick), and two blocks of copper (400 $W \cdot m^{-1} \cdot K^{-1}$, 2 mm thick) are used at the extremities of the structure. The simulations use a boundary heat source to impose the heat generated by the DUT, and the temperature at the bottom surface is fixed at 25°C. All the surfaces are thermally insulated, and we used a thin thermal resistive layer (0.3 $W \cdot m^{-1} \cdot K^{-1}$, 15 μm thick) between the alumina and silicon layers. Fig. 4.10 shows the temperature difference between the two

sensors surfaces as measured by our sensors and as obtained by the performed thermal simulations.

The apparatus has been characterized by performing numerous calibration measurements in DC and with arbitrary electric signals. In Fig. 4.11 we reported a calibration curve that relate the power dissipated by a MOSFET in DC operation (calculated as $V_{DS} \times I_D$) and the temperature difference $\varDelta T$ measured between the two RTD sensors. The linear fit of the data-set is $\varDelta T = 29.14 \times P$, with a coefficient of determination $R^2 = 0.99948$ and a standard error of 0.3080 °C. The sensitivity of the sensor is therefore *29.14 °C/W;* it is possible to obtain different sensitivities by changing the thermal resistive layer of the sensor.

After the DC calibration, we analysed the heat dissipation of the MOSFET in switching operation, driving its gate with square wave at various frequencies and connecting different loads to its drain.

The chart in Fig. 4.12 shows the power loss measured by our circuit and that measured by a digital oscilloscope (*LeCroy Wavepro 7100* equipped with an *AP015* current probe) at increasing frequencies and with a fixed load. It is possible to observe that the two measurements are in good agreement at low frequencies while they tend to diverge as the frequency increases. This is evidently due to the underestimation of the losses measured through the oscilloscope at higher frequency.

In Fig. 4.13 we show a comparison of the power measured with the two methods with the MOSFET driven at the frequency of 100 Hz. We varied the load conditions for the switching device, and detected the temperature difference $\varDelta T$ between the two sensors, from which the produced heat could be calculated by means of the relative calibration curve. At each point, in addition, the dissipated power was measured by means of the same digital oscilloscope.

(a)

(b)

(c)

(d)
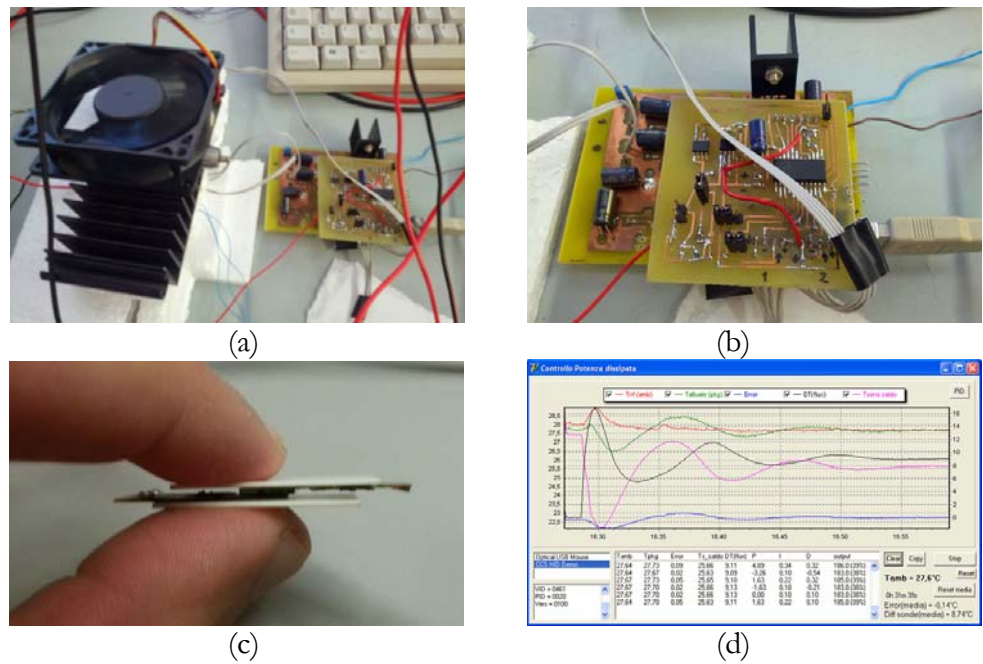
Fig. 4.8 Images of the realized calorimetric apparatus: a) complete apparatus, b) acquisition board, c) heat-flux sensor, c) software for data acquisition
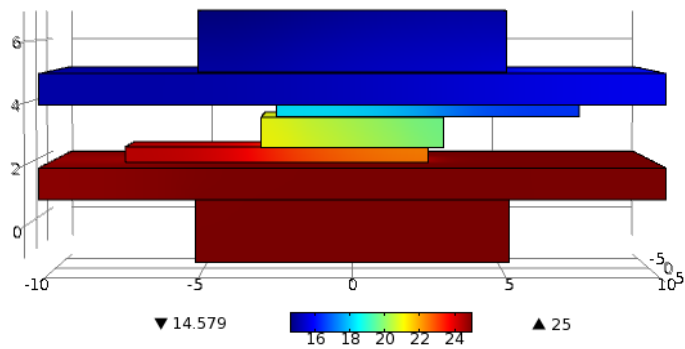
Fig. 4.9 Geometry and temperature distribution of the structure simulated with an heat source of 1 W
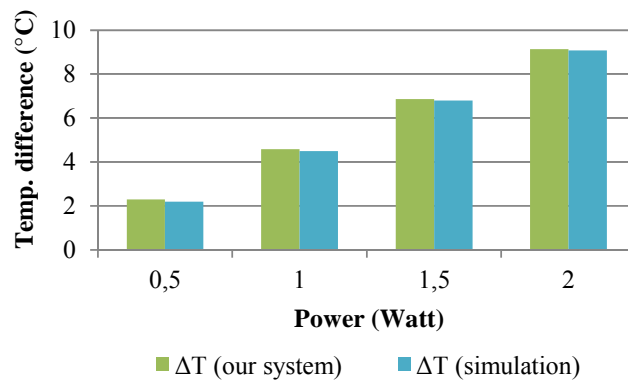
Fig. 4.10 Temperature difference between two sensors surface as measured by our system and by thermal simulation
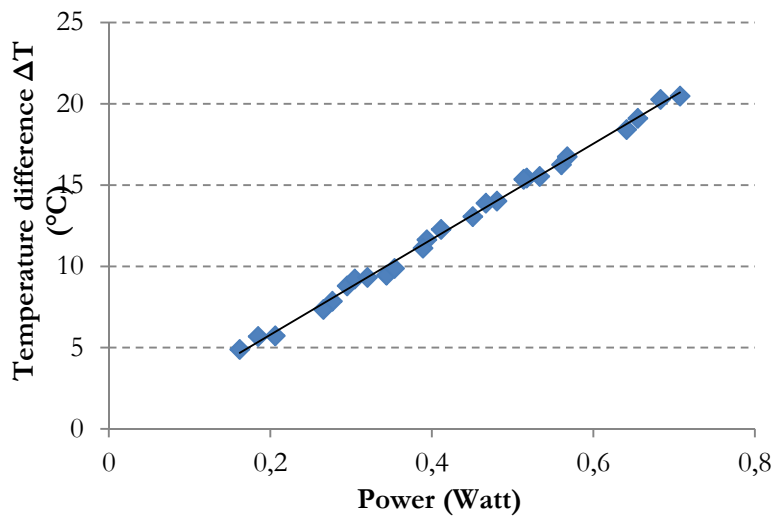
Fig. 4.11 A DC calibration curve of the apparatus
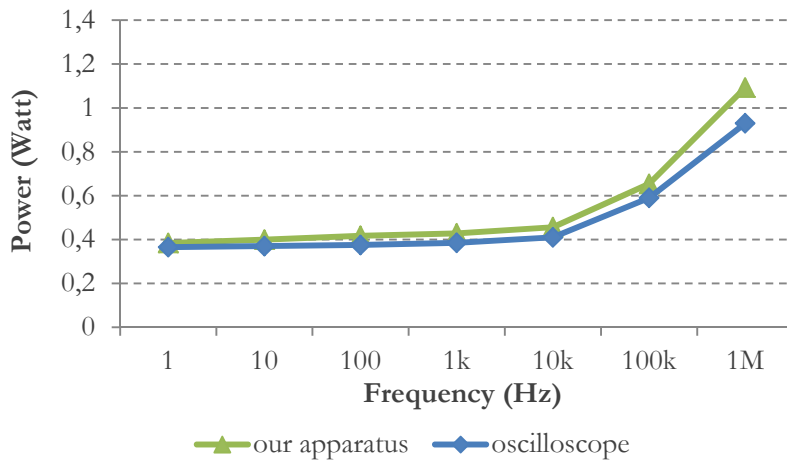
Fig. 4.12 Comparison between the dissipated power estimated by our system and the power measured by a digital oscilloscope with variable frequency and fixed load
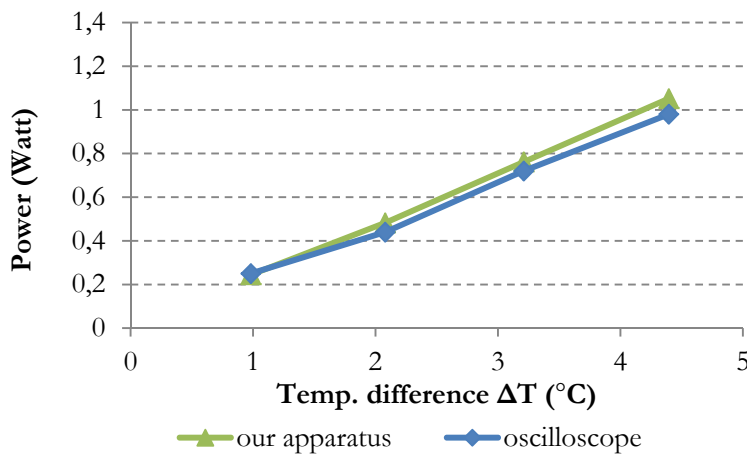
Fig. 4.13 Comparison between the power estimated by our system and the power measured by a digital oscilloscope. The switching frequency is 100Hz while the load is varied

4.4.4 Conclusions

A calorimetric apparatus for the measurement of the power dissipated by a switching device has been realized for performing calorimetric measurement of the power loss of a power device. The set-up consists a of heat-flux sensor, a thermoelectric module with heat-sink and a microcontroller-based readout circuit. The heat flux sensor is based on two expressly-made micro-machined RTDs sensor and a thermoelectric module is used to absorbs the heat and to keep the device at the same temperature of air in order to minimise the heat exchanged and thus the heat leakage.

The apparatus was used to measure losses of devices operating in dynamic repetitive conditions. A calibration procedure is necessary to establish the relation between the measured flux and the dissipated power.

Also finite element thermal simulations were performed to evaluate the temperature profile of the apparatus and they showed good accordance with our prototype.

Inversely from by other calorimetric methods, this set-up is simpler because it does not require the use of a closed chamber and has a simpler isolation. The apparatus could also be adapted to make in-circuit measurements with the final aim to build a sensor integrated within the power device case or mounted between the device and the heat-sink to get a real-time estimation of a system efficiency.

5 Multilevel inverter in detail

This chapter focus its attention on the multi-cell modified cascade multilevel inverter that will be used in the subsequent simulations and for the prototype. The SHE control technique has been applied to calculate the optimal switching angles that minimize the lower order harmonics and reduce the THD. The solutions for various number of levels are reported, and an algorithm to determine the optimal angles, given the number of levels and the desired output voltage, is provided. Finally a "swapping" control technique, which allow to achieve evenly utilization of the sources, has been discussed.

5.1 Introduction

An overview of multilevel inverters and their advantages over traditional inverters, which include higher efficiency and reliability, have already been discussed in chapter 3. Photovoltaic sources are particularly suited for these category of inverters as they can be easily partitioned to form the voltage level required for the DC-sources.

The use of PV sources for these topologies, however, might reduce the global efficiency of the system because periodically a given set of PV modules (or string) is "open", i.e. not connected to a load, and therefore does not produce useful energy. A way to recover efficiency consists in including storage elements (e.g. capacitors, rechargeable batteries) that operate as the load of the open PV modules in the time slots during which the string is not put in series with the other strings. Such components store the energy produced by the PV modules when they are disconnected from the rest of the system and release it when the load is reconnected. The storage elements might also compensate for small discontinuities in the operation of the photovoltaic modules, or provide

significant robustness for voltage drops or load swings at the AC utility grid interface [26], [27].

The importance of the storage elements will be shown clearly in the next chapter. The next paragraphs present the multilevel inverter and the control technique utilized in this thesis work.

5.2 Characteristics of the realized multilevel inverter

The complete system realized includes DC-sources, storage elements, a multilevel inverter based on the Multi-cell Modified Cascade H-bridge topology, and control logics (Fig. 5.1). Simulations and an "intelligent" prototype of the system will be shown in the next two chapters. The simulation of the complete system gives useful information in terms of efficiency, distribution of power dissipation and effects of the variation of parameters such as temperature and parasitics of the components. The prototype allows to evaluate the actual performance of the inverter and verify that they are in accordance with the simulations.

In the schematic shown in Fig. 5.1, it is easy to note the differences with the generic topology shown in Fig. 3.8: N-MOSFETs are used as switching devices and the switches of the DC-blocks are positioned in the return path of the current so that the source terminal of the MOSFET is clamped to the negative terminal of the DC-source. To make the system modular, each DC-block is independent and has its own controller, powered by the associated DC-source. Since the ground reference level of the controller is the same of the source terminal of the MOSFET, it is easy the control the gate-source voltage. Therefore this configuration simplifies the control of the MOSFET turn-on and does not need level shifters or other complex driving circuits required for the "high-side" configuration in which the MOSFET has a floating source.

These variation does not modify the working principles of the inverter that has been illustrated in paragraph 3.7.
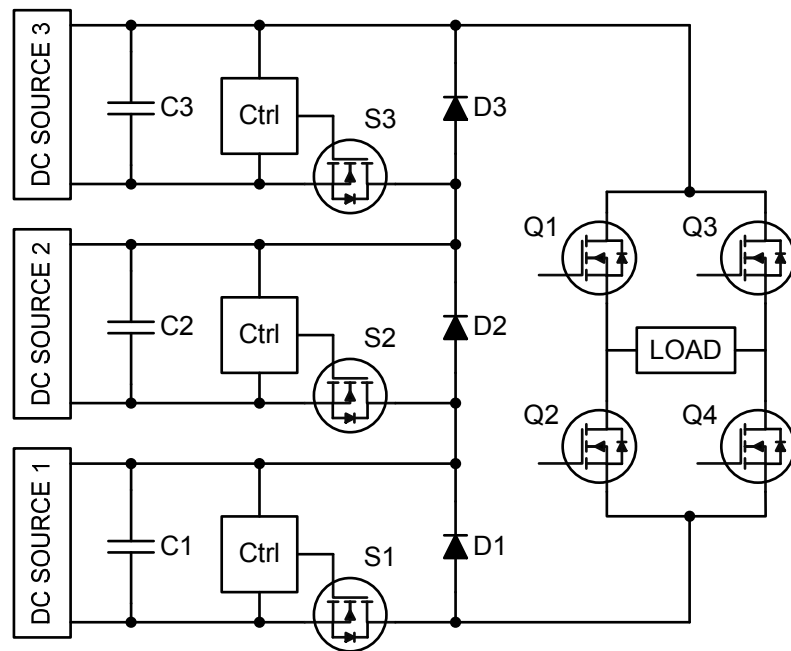
Fig. 5.1 Schematic diagram of the realized 7-level Multi-cell Modified Cascade H-bridge Inverter, with storage elements and control logics

5.3   Utilized modulation technique

The efficiency, power loss in the switches, and the harmonic distortion of the output waveform depend on the modulation strategy used to control the inverter [58]. The SHE technique (3.8.1) is particularly suitable for multilevel inverter as it allows to reduce the harmonic distortion by minimizing the lower order harmonics while keeping low the switching frequency of the switches.

In fact, a suitable way to reduce the power losses in the switches is to reduce the switching frequency. However this yields to harmonic components of the output waveform very close to the fundamental one. The lower order harmonics can be more problematic compared to the higher order ones, because they are difficult to filter due to their proximity to the fundamental one. Therefore the use of the SHE technique to eliminate the low order spectrum components allows to operate at low switching frequency and to reduce the power consumption.

Utilizing the SHE technique, the output waveform of a multilevel inverter, is obtained by switching on and off the devices such that the output waveform approximates the sinusoid with the minimum harmonic distortion.

The Total Harmonic Distortion (THD) is a parameter that measures the harmonic distortion present in a waveform. The voltage THD can be calculated as the square root of the sum of the squares of the harmonics voltages divided by the fundamental one:

$$THD = \frac{\sqrt[2]{V_2^2 + V_3^2 + \cdots + V_n^2}}{V_1}. \tag{5.1}$$

5.3.1 Calculation of the switching angles

By using the SHE technique, the switching angles are obtained through the solution of the set of nonlinear transcendent equation reported in (3.3). The solution of that set of equations allows to minimize the 3rd, 5th, 7th, … *(2n+1)*[th] harmonics, where *n* is the number of DC-sources available and *2n+1* is the number of levels of the inverter.

The solution can be obtained by means of numeric iterative methods, e.g. Newton-Raphson. Various methods have been implemented to seek out the solutions; the method described here uses the function *fsolve*, included in Optimization toolbox of MATLAB, that allows to obtain the solution of a nonlinear system of equations in the form *F(x) = 0*. The choice of the initial guess x_0 is important for the convergence of the algorithm and therefore a MATLAB routine that uses the function *fsolve* has been developed to search for the solution starting from random initial guesses. Since for each number of levels there may be many possible solutions, the routine chooses the one that has the lowest THD, i.e. the optimal solution.

An approach useful to speed up the convergence or to search the solution in real-time using digital controllers, is to transform the set of transcendental equations in a system of polynomial equations by using Chebyshev polynomials of the first kind.

$$\begin{aligned} T_0(x) &= 1 \\ T_1(x) &= x \\ T_{n+1}(x) &= 2xT_n(x) - T_{n-1}(x). \end{aligned} \tag{5.2}$$

where the polynomials can be defined as:

$$T_n(\cos(\vartheta)) = \cos(n\vartheta) \quad n = 0, 1, 2, 3, \dots \tag{5.3}$$

As an example, the (3.3) for a 5-level inverter become

$$4x_1{}^3 - 3x_1 + 4x_2{}^3 - 3x_2 = 0$$
$$16x_1{}^5 - 20x_1{}^3 + 5x_1 + 16x_2{}^5 - 20x_2{}^3 + 5x_2 = 0, \tag{5.4}$$

and, after a solution has been found, it is easy to find the switching angles as

$$\theta_i = \mathrm{acos}(x_i), \qquad i = 1 \dots n. \tag{5.5}$$

Table 5.1 reports the optimal switching angles obtained applying the described technique for different numbers of levels.

Fig. 5.2 and Fig. 5.3 show how the THD and the spectrum of the output voltage waveform change as the number of level increases. It is possible to observe that, as the number of level increases, the THD of the output voltage waveform decreases.

Table 5.1 Optimal switching angles obtained with the SHE technique for different number of levels

Num. of levels	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6
3	30°					
5	12°	48°				
7	11,67°	26,94°	56,06°			
9	0,86°	24,86°	35,14°	60,86°		
11	5,73°	21,41°	35,10°	55,89°	87,13°	
13	7,27°	14,94°	29,44°	40,85°	59,58°	87,52°
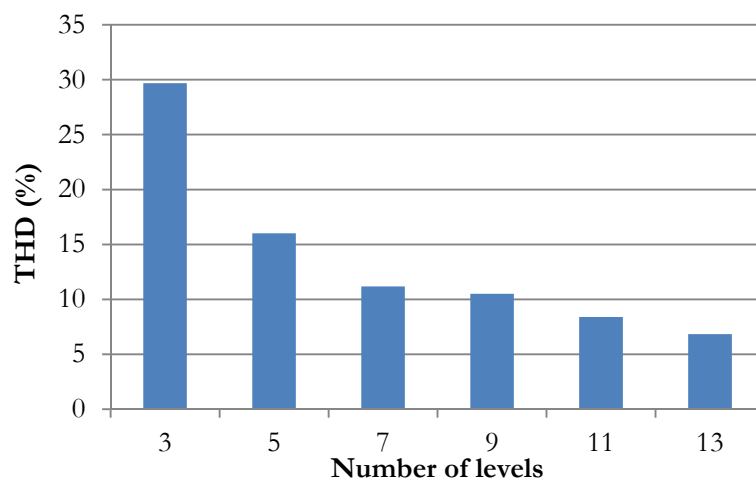
Fig. 5.2 THD of the output waveform at increasing number of levels, calculated on the first 40 harmonics

5.3.2   *Amplitude modulation of the output waveform*

As described in 3.8.1 the SHE can be used to minimize *n* low order harmonics, or a degree of freedom can be used to control the amplitude of the voltage of the output waveform though the modulation index.

For example, in an eleven levels inverter, there are five degrees of freedom, therefore four of them can be used to minimize the four lower order harmonics, whereas the last one can be used to adjust the amplitude output voltage by regulating the main component.

The (3.6) can be solved, as described in the previous paragraph, by iterative methods. As there are many possible solutions for every value of the modulation index, a MATLAB routine has been developed. The script calculates, starting from random initial guesses, a number of possible solutions and select, for every m_I, the solution that provides the lowest harmonic distortion. The routine executes, for a given number of levels, the following cycle for every m_I:

- constructs the SHE set of equations for the desired number of levels and the m_I value;
- finds the valid solutions of the set of equations starting from a predefined number of random initial guesses;
- excludes incorrect solutions (e.g. angles > 90°);
- selects, among the valid results, the solution with:
  - the minimum THD, or
  - the minimum value of the harmonics to be cancelled.

It is worth to note that the optimal solution can be different if it is selected by considering the minimum THD or the minimum value of the chosen harmonics.

Fig. 5.4 shows the optimal switching angles (selected with the minimum THD criterion) and the relative THD as a function of m_I, for various number of levels, whereas the output voltage vs modulation index for a seven levels inverter is shown in Fig. 5.5:
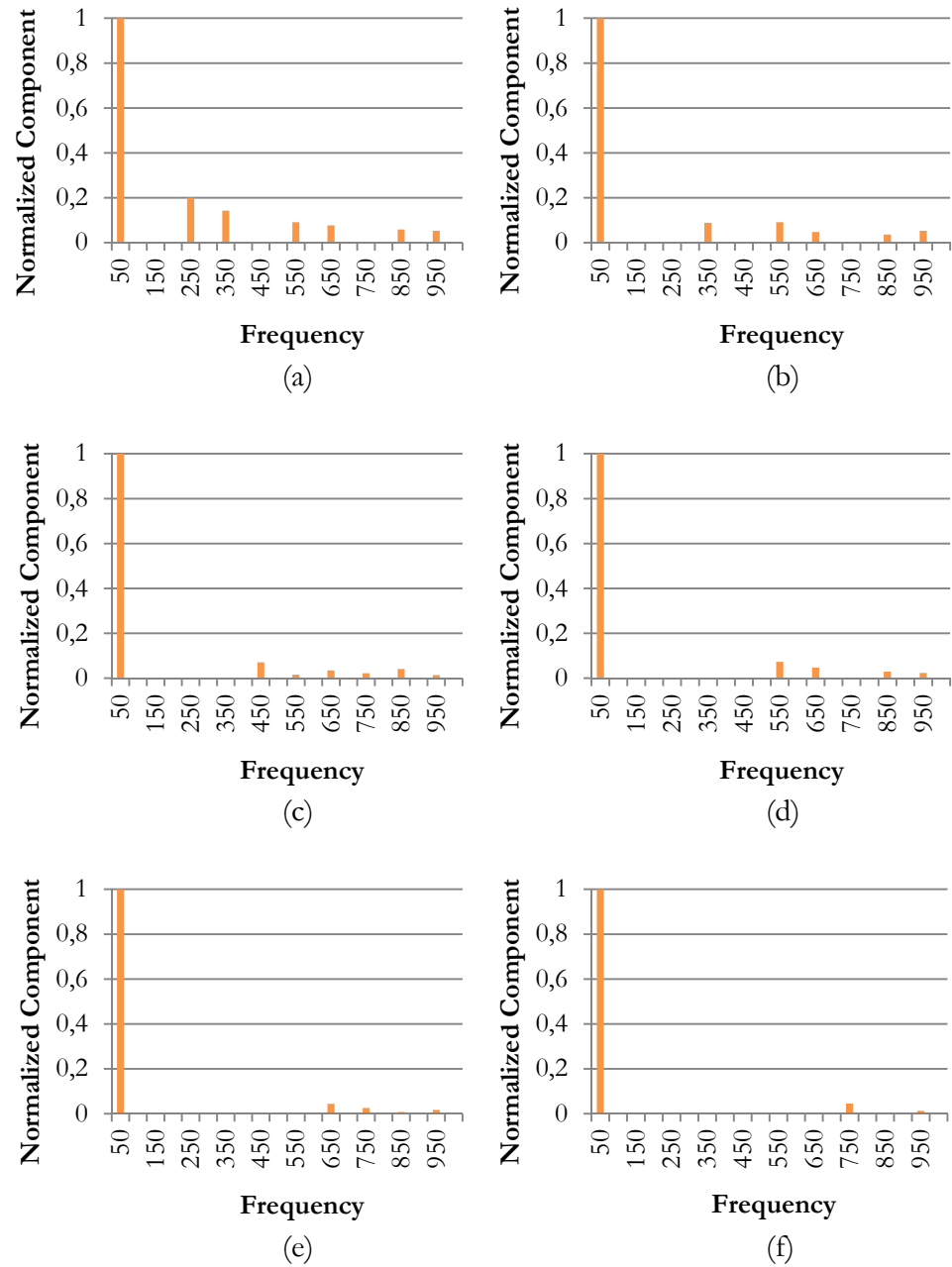
Fig. 5.3 Fourier components of the output voltage: a) 3-levels, b) 5-levels,
c) 7-levels, d) 9-levels, e) 11-levels, f) 13-levels
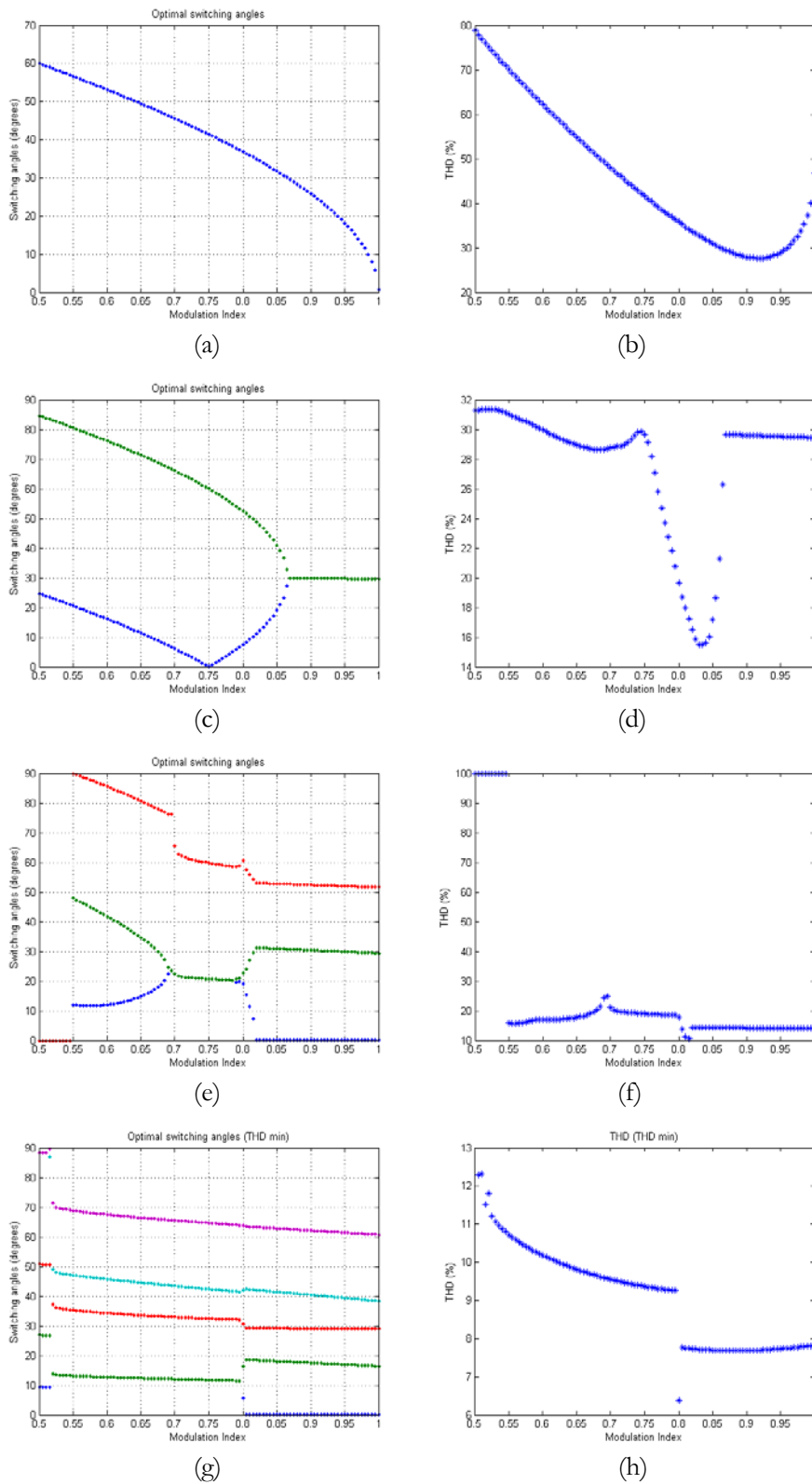
Fig. 5.4 Optimal switching angles and the relative THD versus the modulation index: a) 3-levels angles, b) 3-levels THD, c) 5-levels angles, d) 5-levels THD, e) 7-levels angles, f) 7-levels THD, g) 11-levels angles, h) 11-levels THD
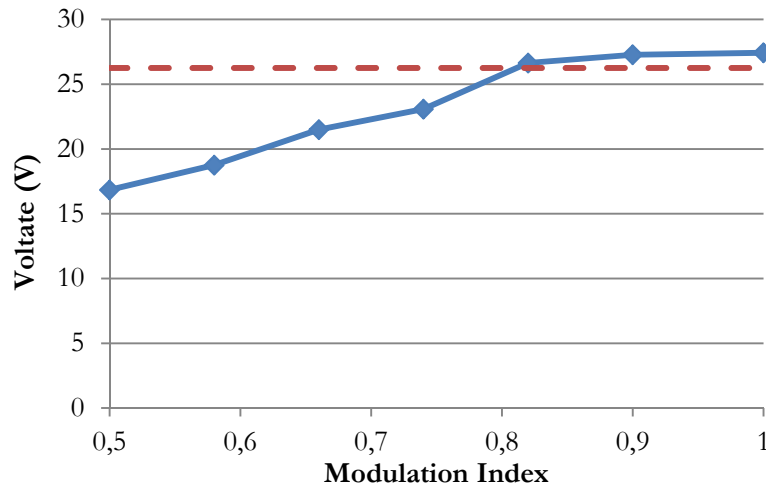
Fig. 5.5 Output voltage vs modulation index for a seven levels inverter with 12 V DC-sources; the dashed line is the output voltage obtained by annulling the 3rd, 5th, 7th harmonics without the regulation the fundamental

5.3.3 Duty cycle swapping

The SHE technique allow to determine the optimal switching angles of each DC-block and produce waveforms such as those in Fig. 3.11. However, the straight application of those patterns leads to an unbalanced use of the DC-blocks, which will therefore unevenly contribute to energising the load. In fact, e.g. in a seven levels inverter, the source corresponding to the third level ($3V_{DC}$), whose DC-block switches at θ_3, will supply on average much less power than the sources associated with the 1st and 2nd levels, whose DC-blocks switches at θ_1 and θ_2 and therefore stay ON for a longer time. This may result in non-uniform voltages at the capacitor or battery terminals, an event that can in turn increase the total harmonic distortion of the output voltage waveform.

The duty cycle "swapping" is a technique based on the variation of the switching angles sequence that can be utilized, in addition to the SHE, to prevent the uneven usage of the DC blocks [33].

This technique consists in rotating the duty cycle of each DC block, e.g. every cycle, so that all the energy sources are evenly used over a number of cycles. Fig. 5.6 shows the waveforms produced by each DC-block and the overall output waveforms of the Modified Cascade MLI with the swapping technique applied.

This technique has been used for this thesis, both on the simulations and on the prototype. Moreover, for the prototype a variation of this technique has also been developed. It consists in swapping the control signals based on the state of charge (SOC) of the storage elements, e.g. batteries. With this variant the system checks continuously for the voltage of each DC-blocks and override the swapping by forcing the DC-block with the lowest voltage to apply the control signal with the lowest duty cycle and therefore to provide less power. This is particularly useful when the batteries have different SOC and allows to restore a uniform SOC among the various sources.
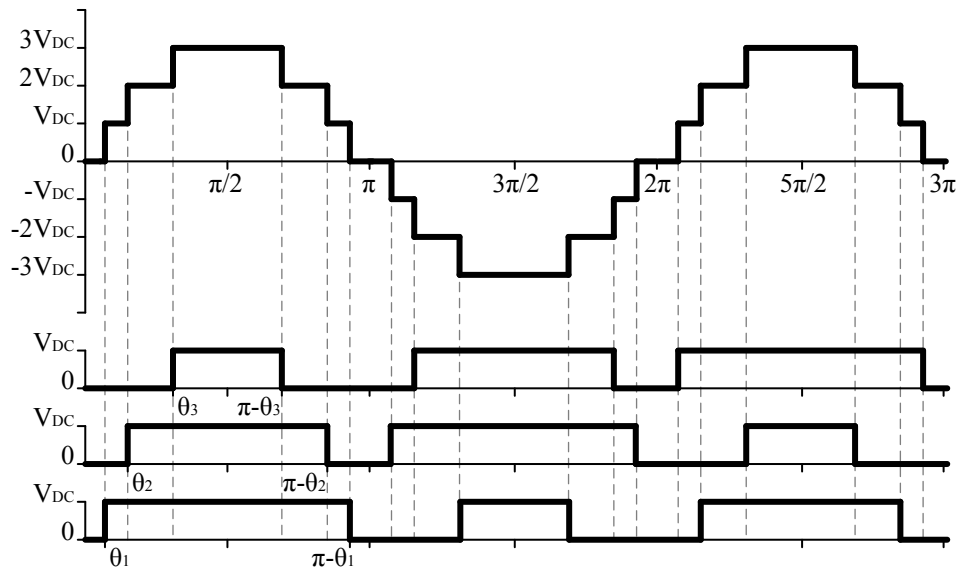
Fig. 5.6 Output voltage of the inverter, and output waveforms of each DC block for a 7-level inverter with SHE and swapping technique applied

6 SPICE model of the complete photovoltaic system

In this chapter a SPICE simulation model of a complete photovoltaic system is presented, including a detailed model of photovoltaic cells, a modified cascaded multilevel inverter, and energy storage elements. The simulation of the system as a whole allows evaluating readily the effects on its performances of the variation of the component parameters, as well as of the external load, the solar irradiation, and the cell temperature. The global conversion efficiency and the total harmonic distortion of the output waveform are in particular analysed. The role and sizing criteria of a storage element, such as a capacitor, placed at the PV module output, are also analysed for various operating conditions.

6.1 Introduction

This chapter reports about the build-up and use of a SPICE model of a complete PV system including a detailed model of PV cells, storage elements, and a multilevel inverter circuit (Fig. 6.1). The PV cells are grouped in series to form PV modules or strings. The model of the converter, that includes the nonlinearities of the switches, allows the complete characterization of the system dynamics.

The all-in-one simulation approach yields useful information in terms of efficiency, distribution of power dissipation and effects of the variation of the operating point with respect to the maximum power point, otherwise not obtainable through a separate simulation of the subsystems.

In order to show the advantages of studying the entire system in a single simulation, a simple PV system was considered. The inverter structure used in

this study is the Multi-cell Modified Cascade H-bridge (paragraphs 3.7, 5.2) in conjunction with the SHE modulation technique (paragraphs 3.8.1, 5.3).

The tool used for the simulations is Cadence PSpice [59], a de-facto industry-standard SPICE-based simulator, which supports a wide range of simulation models and includes advanced simulation technologies that allow to improve reliability and speeds on larger systems.

The next paragraph describes the inverter circuit and its elements, and the fundamental SPICE model of the PV cell that has been used to build up the PV string model. Then the simulation results are described, showing the advantages of an all-in-one model approach compared to other more common approaches, where e.g. ideal DC sources are used instead of the PV modules. Comments are also provided on the system efficiency and general criteria for a correct set of the storage elements and switches.
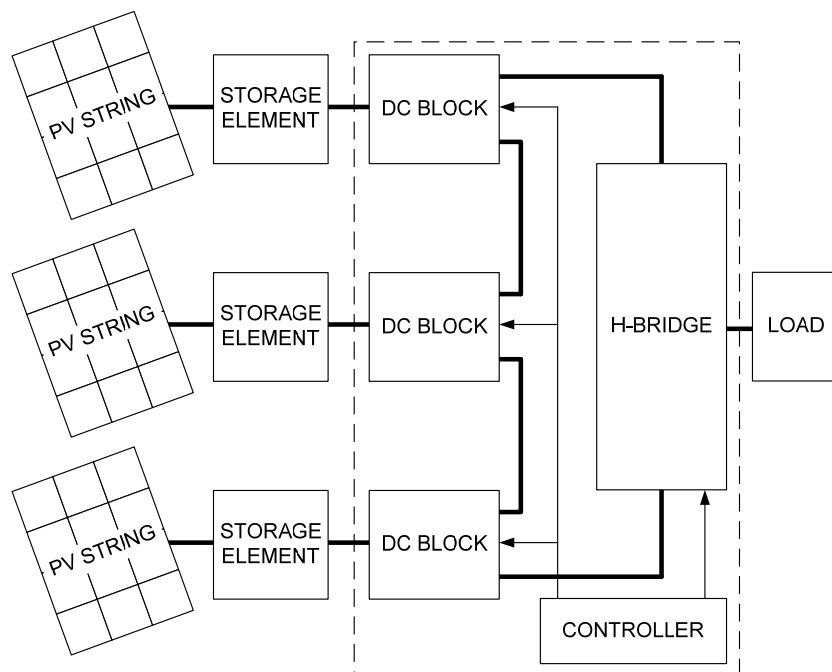
Fig. 6.1 Schematic diagram of the simulated system. Each PV string is connected to a storage element and to a DC block. The DC blocks are connected in series to build the output waveform.

6.2   Description and characteristics of the model

The structure used in the simulation is a seven levels Multi-cell Modified Cascade H-bridge inverter connected to a resistive load, whose SPICE schematic is shown in Fig. 6.2.

The circuit consists of three identical DC-blocks each including a PV string, a storage element (C1, C2, C3), a controlled switch (S1, S2, S3) and a diode (D1, D2, D3). The three blocks are connected in series to generate a positive waveform with four different voltage levels (0, V_{DC}, $2 \cdot V_{DC}$, $3 \cdot V_{DC}$). The necessary driving signals are generated by the DRV blocks (drivers).

The H-bridge connected after the DC blocks allows to generate positive and negative polarity in the output waveform. The MOSFETs are driven so that Q1-Q4 or Q2-Q3 are turned ON for a half cycle, allowing to invert the input waveform.

The three main element of the inverter (DC-blocks, PV sources and storage elements) will be analysed in the following paragraphs.
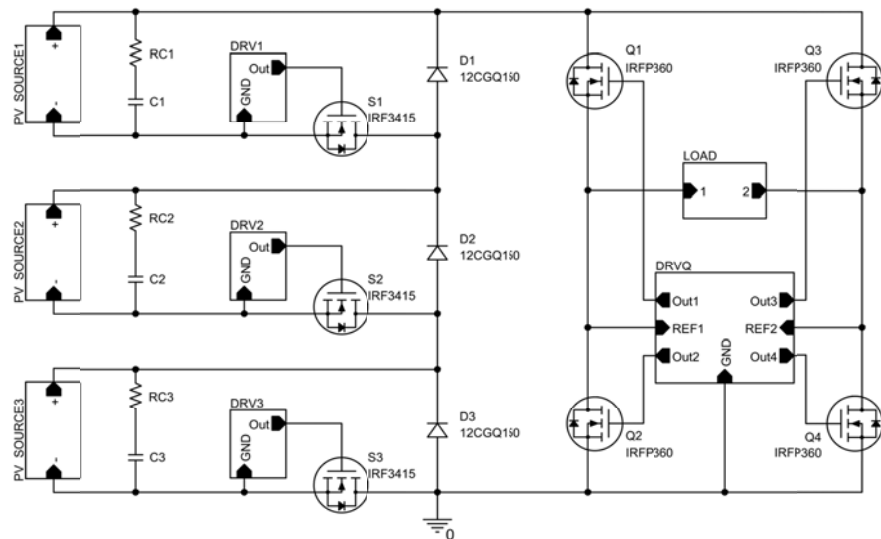
Fig. 6.2 SPICE implementation of 7-level inverter with multi-cell modified cascade H-bridge topology

6.2.1 DC-blocks

6.2.1.1 Switching devices

The switches used in the circuit are MOSFET and, for the simulations, models of commercial devices have been used. The S1-S2-S3 switches are *IRF3415* N-MOSFETs [60]. These switches are positioned in the return path of the current, allowing an easier control of the turn-on without the need of a level shifter, because the source terminal is clamped to the negative terminal of the DC-source. The D1-D2-D3 diodes are IRF *12CGQ150* Schottky rectifiers [61] with maximum reverse voltage of 150 V and low forward voltage drop. The H-bridge switches are *IRFP360* [62], with a higher Drain-Source breakdown voltage than *IRF3415*. These devices can be easily replaced with others with better characteristics to analyse the behaviour of the system.

Many simulation have been made also with other devices; for example *IRF3415* have been replaced with *IRFPS3815* [63], whereas the MOSFETs of the H-Bridge *IRFP360* have been replaced with *IPW65R045C7* [64], a super-junction MOSFET that can provides a much higher efficiency (cf. paragraph 3.9.4.1). The main difference between the two pairs of devices regards the drain-source ON resistances ($R_{DS(on)}$) which is very low in the second couple of devices used in the simulation. In the Table 6.1 are reported the main specifications of the two couples of devices.

6.2.1.2 Control signals and modulation technique

With a 7-level inverter it is possible to eliminate the 3rd, 5th, and 7th harmonics by determining the conduction angles θ_1, θ_2, θ_3 that solve the SHE equations set derived from (3.3):

$$\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) = 0$$
$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_n) = 0 \qquad (6.1)$$
$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_n) = 0.$$

By solving the above set of equation as shown in 5.3.1, one obtains the conduction angles reported in Table 6.2. From these, assuming a sine wave at 50 Hz, the corresponding conduction delays and pulse duration can be calculated. The periodic swapping of the control signals among the three DC

sources has been utilized to balance their average usage as described in 5.3.3. The DRV blocks are used to generate the gate signal of the S1-S2-S3 switches based on the pre-determined conduction angles; their circuitry includes a periodic signal generator, logic gates and resistors to limit the input current at the gate terminal of the MOSFETs. The driving signals for the S1-S2-S3 switches caught at the gate terminal of the MOSFETs are shown in Fig. 6.3.

Finally, the DRVQ block generates the switching signals for the H-bridge MOSFETs.

Table 6.1 Key specification of the MOSFET used in the simulations

Parameters (max. values)	DC-block MOSFETs		H-Bridge MOSFETs	
	IRF3415	IRFPS3815	IRFP360	IPW65R045C7
V_{DS} (V)	150	150	400	700
$R_{DS(on)}$ (mΩ)	42	15	200	45
I_D (A) @ 25 °C	43	105	23	212
Q_g (nC)	200	260	210	93

Table 6.2 Conduction angles, delay and pulse duration for the 7-level inverter

	Conduction Angles	Conduction Delay @ 50 Hz	Pulse Duration @ 50 Hz
θ_1	11.7°	0.65 ms	8.70 ms
θ_2	26.9°	1.49 ms	7.02 ms
θ_3	56.1°	3.11 ms	3.78 ms
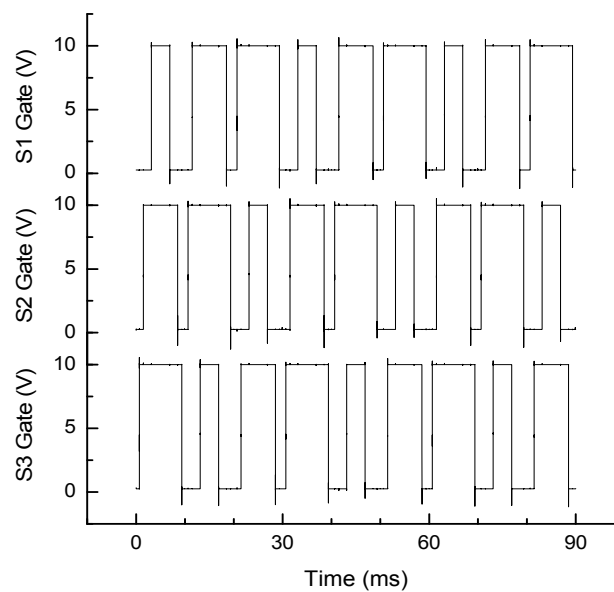
Fig. 6.3 Driving signals for the S1-S2-S3 switches of the inverter, caught at the gate terminal of the MOSFETs

6.2.2   Model of PV modules

The common approach in SPICE-based studies of multilevel inverters provides for the use of standard DC sources as power generators [22], [31], [65]. To gain accuracy in the results, in the PV system considered in this study, shown in Fig. 6.1, three PV strings replace the DC sources of Fig. 3b. These strings are made of the series of 220 PV cells each. The model used for the single cell is the double diode exponential model introduced in paragraph 2.5. The model (2.11) is non-linear and implicit and for this reason an iterative method fitting the I-V solar cell characteristic should be used to find the appropriate coefficients of the analytical expression. Here, the Levenberg-Marquardt method is used [66], which guarantees a rapid convergence to solution. This method searches for a solution on the first partial derivative in a given set of key points of the I-V curve and then refines them to get the best approximation of the whole curve. The iterative solution is identified by the Newton-Raphson method.

Once the extraction algorithm has identified the solution, the next step is the implementation of the simulation circuit in the SPICE environment. Our model uses voltage-controlled current generators (VCCG) instead of diodes, because VCCGs allow to implement more effectively the analytical equations of the model for a more efficient computation [67].

The first simulations are performed in standard test conditions. This allows comparing the simulation results with the actual electrical parameters of cells, obtainable from the datasheets. In this work *MOTECH IM156-158* [68] polycrystalline silicon cells have been considered. Through the extraction algorithm, the following values of the characteristic parameters have been identified in Standard Test Condition (25 °C, 1000 W/m^2, AM1.5): $I_{01} = 2.58 \times 10^{-10}$ A, $I_{02} = 6.46 \times 10^{-6}$ A, $I_{ph} = 8.17$ A, $R_s = 3.84$ mΩ, $R_{sh} = 3.99$ Ω.

6.2.2.1   Effect of irradiance and temperature

To allow the model to simulate the real behaviour of a solar cell under variable atmospheric conditions, the dependence of temperature and irradiance is introduced by using the (2.12) with STC reference values and a current temperature coefficient of 3.26 mA/°C.

For the two dark saturation currents the temperature dependence is introduced with the following equations obtained through an exponential interpolation of the I_{01} and I_{02} values extracted at different temperatures:

$$I_{01} = 4.1 \times 10^{-12} \cdot e^{0.1658 \cdot T},$$ (6.2)

$$I_{02} = 2.8 \times 10^{-7} \cdot e^{0.1256 \cdot T}.$$ (6.3)

The simulation results are compared with experimental measurements for different values of the irradiance in Fig. 6.4. A comparison between experimental data and simulations is shown in Fig. 6.5 at variable temperature and fixed irradiance of 1000 W/m^2.
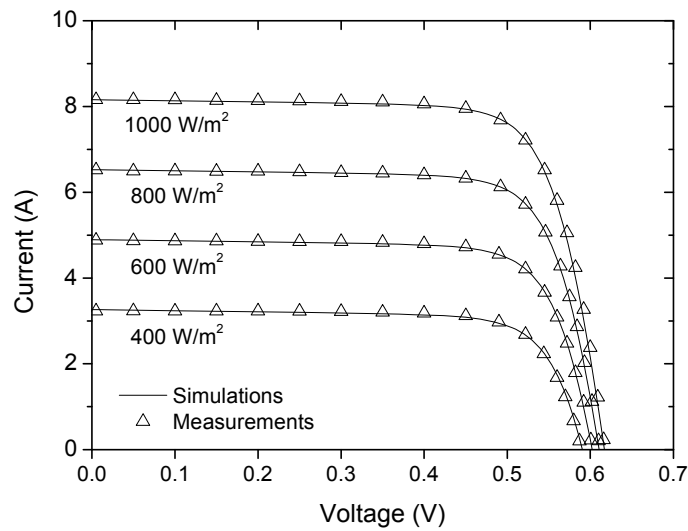
Fig. 6.4 Cell experimental and modeled I-V characteristics at variable irradiance for a temperature of 25 °C.
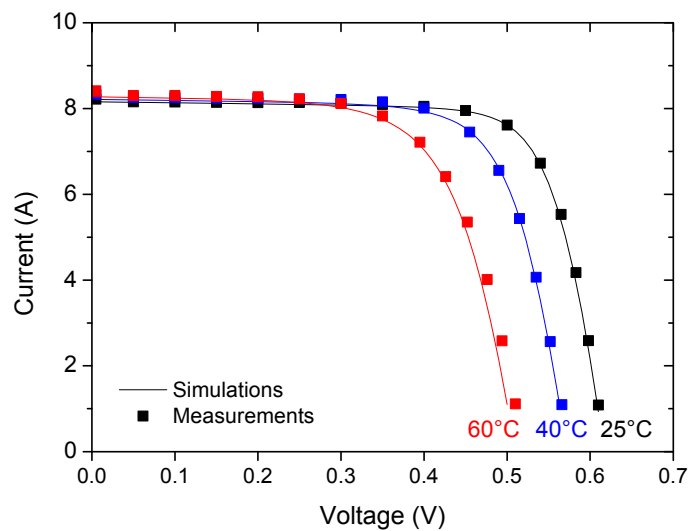
Fig. 6.5 Comparison between experimental data and simulations at the temperature of 25 °C, 40 °C, and 60 °C for an irradiance of 1000 W/m^2.

6.2.2.2 *PV strings*

The photovoltaic module, or string, has been simulated by placing in series the models of several solar cells. It has been initially assumed that the cells in the series have the same characteristics, however it is easy to generalize the analysis and consider the case where cells differ each other due to tolerances or to different irradiance levels.

Considering the same characteristics and operative conditions for all the cells in a string, it is possible to generalize the (2.11) for N_S cells connected in series:

$$I = I_{ph} - I_{01}\left(e^{\frac{V+N_S I R_S}{N_S n V_T}} - 1\right) - I_{02}\left(e^{\frac{V+N_S I R_S}{N_S m V_T}} - 1\right) - \frac{V+N_S I R_S}{N_S R_{sh}}, \qquad (6.4)$$

The SPICE model of a PV string is shown in Fig. 6.6. The current and power vs. voltage characteristics of one PV string considered in this study are shown in Fig. 6.7, whereas in Table 6.3 are reported the string main specifications: short circuit current, open circuit voltage and the values of current, voltage and power at the maximum power point (MPP) for different values of the temperature. As the temperature increases, the maximum power generated by a PV string decreases considerably.
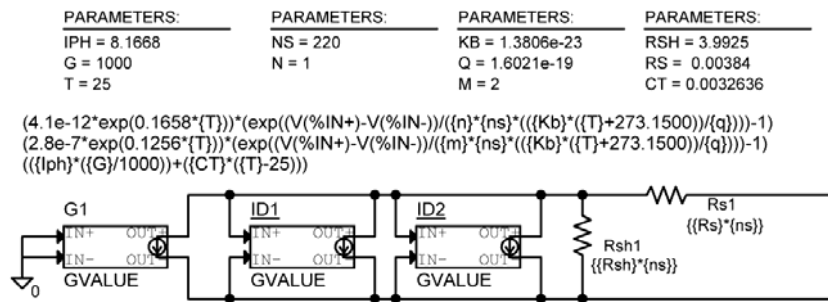
Fig. 6.6 SPICE model of the PV string

Table 6.3 Parameters of the PV String SPICE Model

Parameter	Values at 25 °C	Values at 40 °C	Values at 60 °C
I_{SC}	8.16 A	8.21 A	8.27 A
V_{OC}	135.74 V	127.10 V	112.13 V
I_{MPP}	7.52 A	7.44 A	7.23 A
V_{MPP}	111.43 V	102.01 V	85.92 V
P_{MPP}	838.61 W	759.27 W	621.10 W
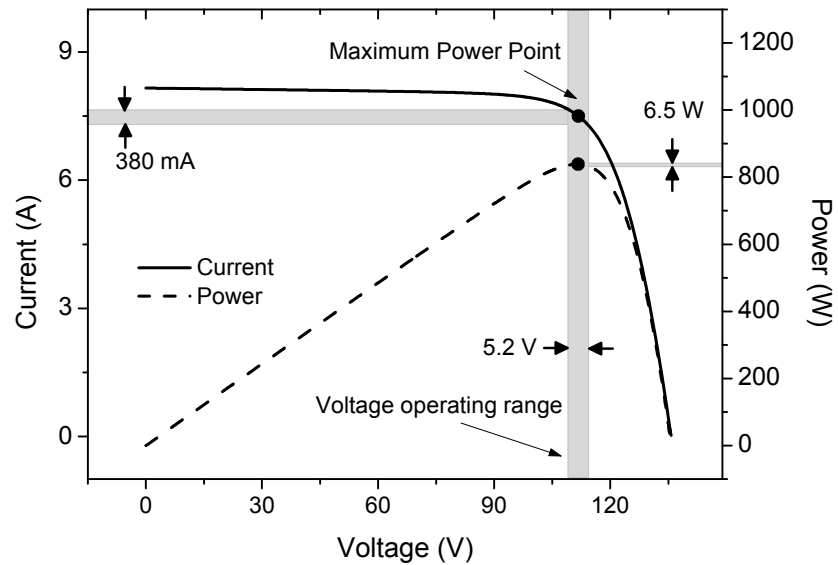
Fig. 6.7 I-V and P-V characteristics of the string SPICE model at the nominal irradiance of 1000 W/m², and at a temperature of 25 °C. The string operating range during a complete switching cycle (30 ms, cf. Fig. 6.9) is also shown for a load of 23.5 Ω and a storage capacitance of 10 mF (grey bands)

6.2.3 Storage elements

One drawback of the application of the multilevel approach to PV systems is that periodically one, two, or all the modules are not connected to the load because the switch of the corresponding block is OFF, reducing therefore the global energy conversion efficiency of the system, from sunlight to the load. However, the use of storage elements can help keeping the conversion efficiency high. In the simulation, capacitors are used as storage elements (C1-C2-C3), and their value has been varied to assess their effect on the system general behaviour. A 100 mΩ resistor in series (RC1-RC2-RC3) schematizes the parasitic resistance of the capacitor and is moreover essential for the convergence of the simulation. This value can be easily changed to reflect the actual ESR (Equivalent Series Resistance) of the capacitors (paragraph 3.9.1).

6.3   Simulation results

The simulation results are analysed in terms of the THD and the overall system efficiency, calculated as the ratio between the power delivered to the load and the power theoretically available at the PV elements output if they were operated at their maximum power point. The results are summarised in Fig. 6.8, assuming an irradiance of 1000 W/m^2 and a temperature of 25 °C (STC); the AC load is varied in the range from 17 to 30 Ω, with 23.5 Ω the load optimising the conversion efficiency.

6.3.1   Effect of storage capacitors

The presence of a storage capacitor is fundamental for the correct operation of the PV generators and the inverter. In fact, for C = 10 mF or above, the circuit efficiency shows its maximum at the optimal AC load. For C = 1 mF or lower, not only the maximum efficiency is not achieved, but for very low capacitances the efficiency is dramatically reduced. This can be explained with the help of Fig. 6.9, showing the time evolution of the operating point of a string for various storage capacitor sizes, in a time interval of 60 ms, corresponding to two full swapping cycles for the DC block, at an irradiance of 1000 W/m^2, at a temperature of 25 °C and for a load of 23.5 Ω. It can be seen that for C = 10 mF the string steadily operates in the proximity of the MPP. The voltage ripple at the string terminals is only 5.2 V (about 4.5% variation), while the current ripple is 380 mA, i.e. about 5% variation. The maximum variation of the power extracted from the string during one cycle is about 0.7%. This working range is highlighted in Fig. 6.7 (grey bars).

Too low a value of the capacitance is unable to store the energy that could be extracted from a PV string in the time slots during which it is not connected to the load. In particular, the fluctuation of the charge stored inside the capacitor results in the impossibility for the PV modules to operate steadily nearby its maximum power point and produces a reduction of the overall system efficiency.

The positive effect of the storage element on the efficiency saturates for C > 10 mF. However, larger storage elements help the strings to operate close

to their MPP also in case of temporary changes of external parameters, e.g. due to load fluctuations.

The use of capacitors of 1 mF or smaller has also a deep negative effect on the quality of the output waveform. With C = 0.1 mF and a load of 23.5 Ω, the THD is over 22%, whereas it is about 9.7% for C > 10 mF. In Fig. 6.10 it is possible to observe how the spectrum of the output voltage changes for two value of storage capacitors. With C = 0.1 mF there is a not negligible third harmonic appearing despite the SHE technique is applied. In fact, the voltage waveform on the load results strongly distorted, as can be seen in Fig. 6.11.
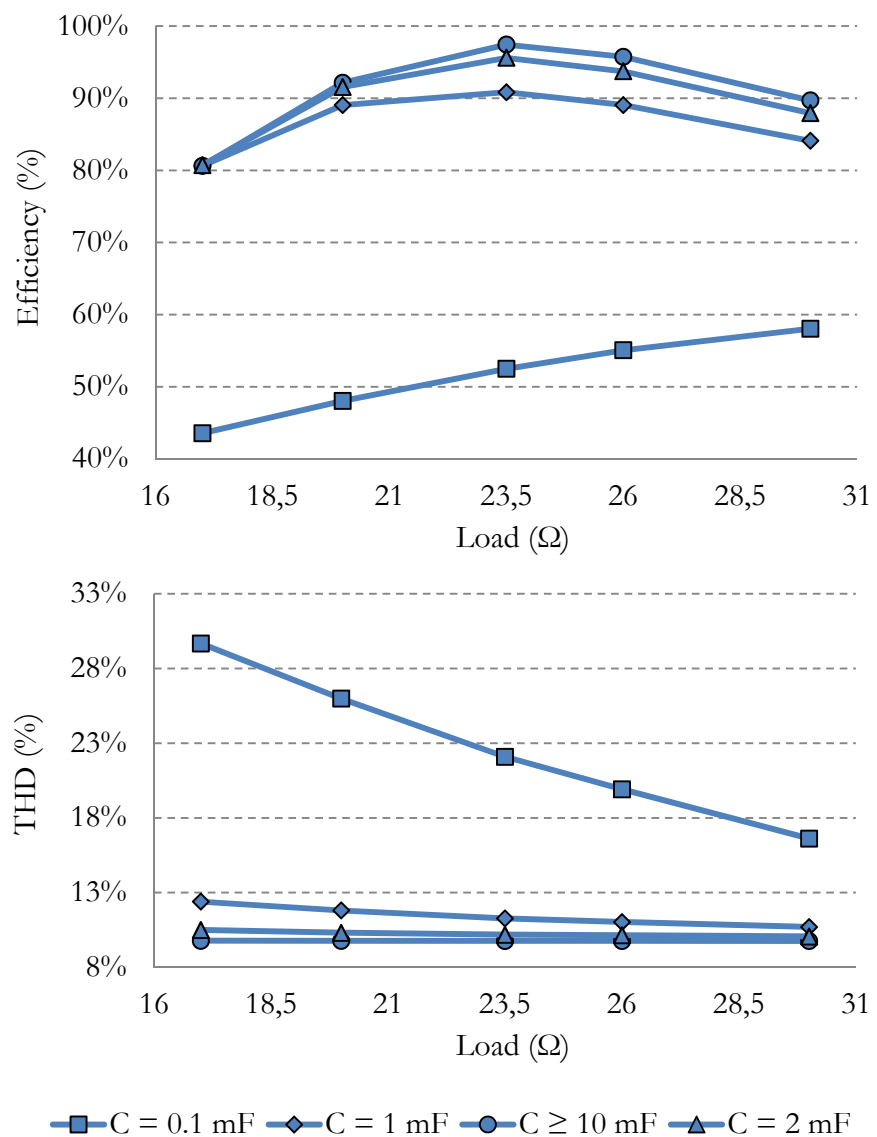
Fig. 6.8 Efficiency of the system and THD of the output waveform vs. load with different sizes of storage capacitors under a nominal solar irradiance of 1000 W/m² and at a temperature of 25°C
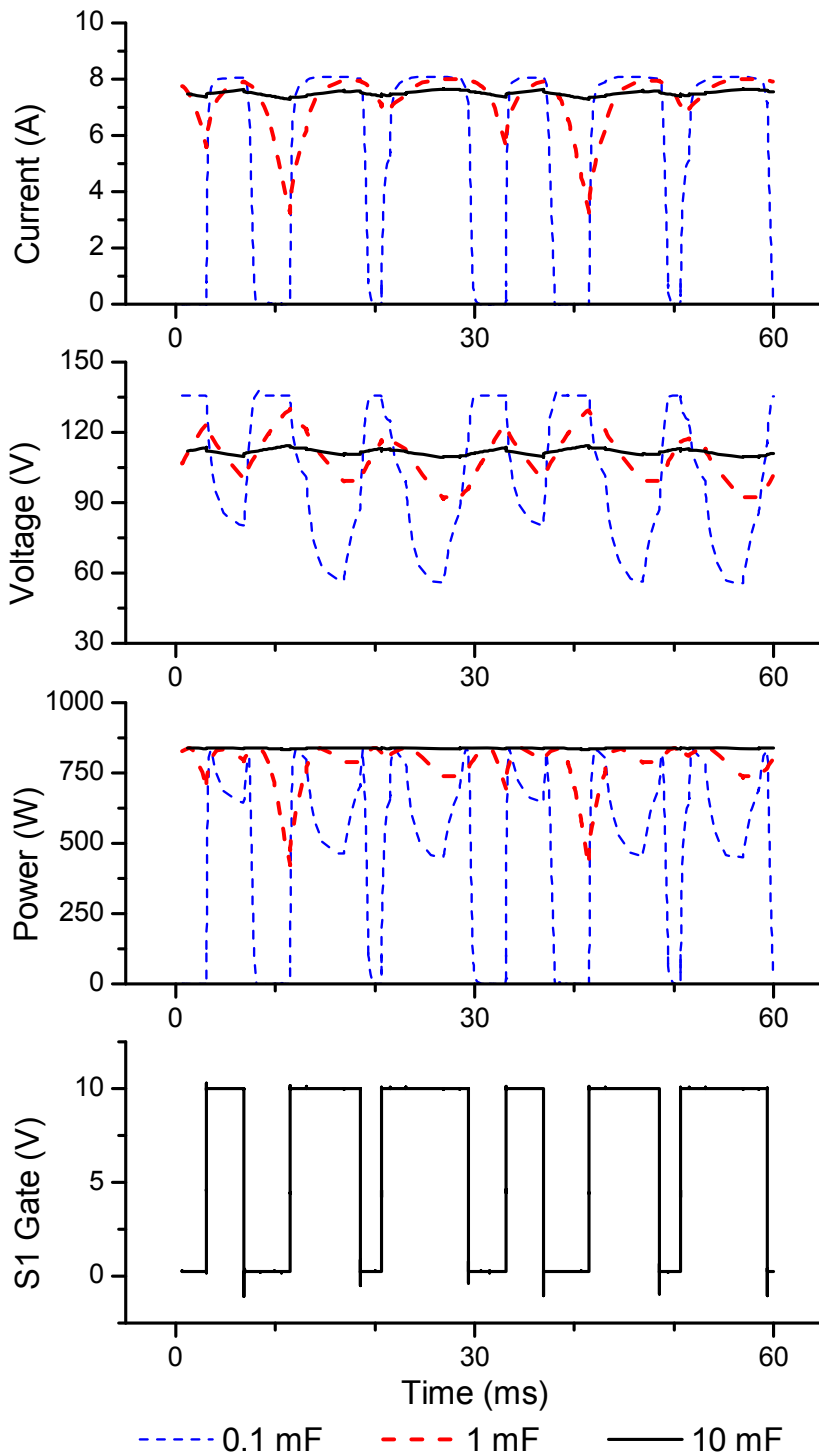
Fig. 6.9 Current, voltage and power at the PV string 1, and control signal of switch S1. The load is 23.5 Ω, while different values of the storage capacitor have been considered: a) 0.1 mF – b) 1 mF – c) 10 mF
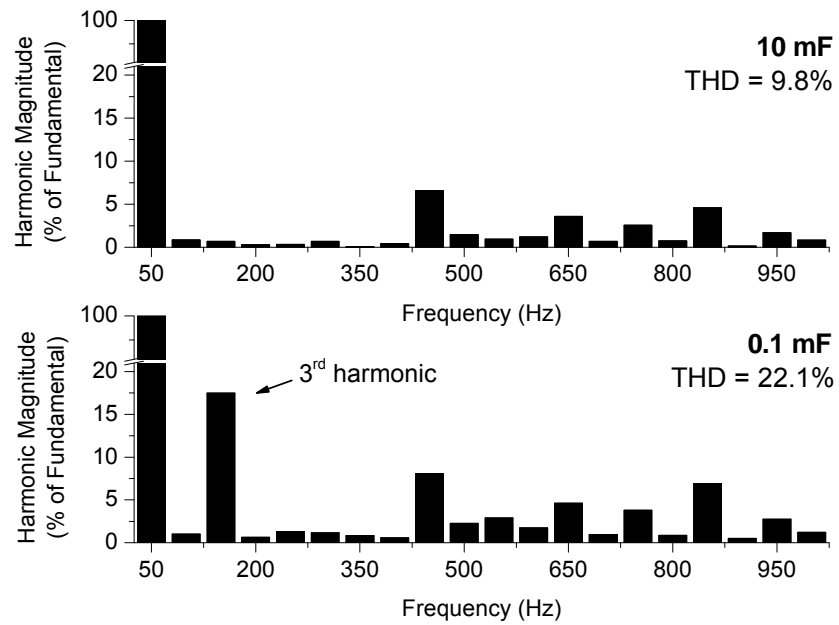
Fig. 6.10 Fourier components of the output voltage approximating the 50 Hz sine wave, obtained for two capacitance values (10 mF and 0.1 mF), with a load of 23.5 Ω, an irradiance of 1000 W/m^2, and a temperature of 25 °C
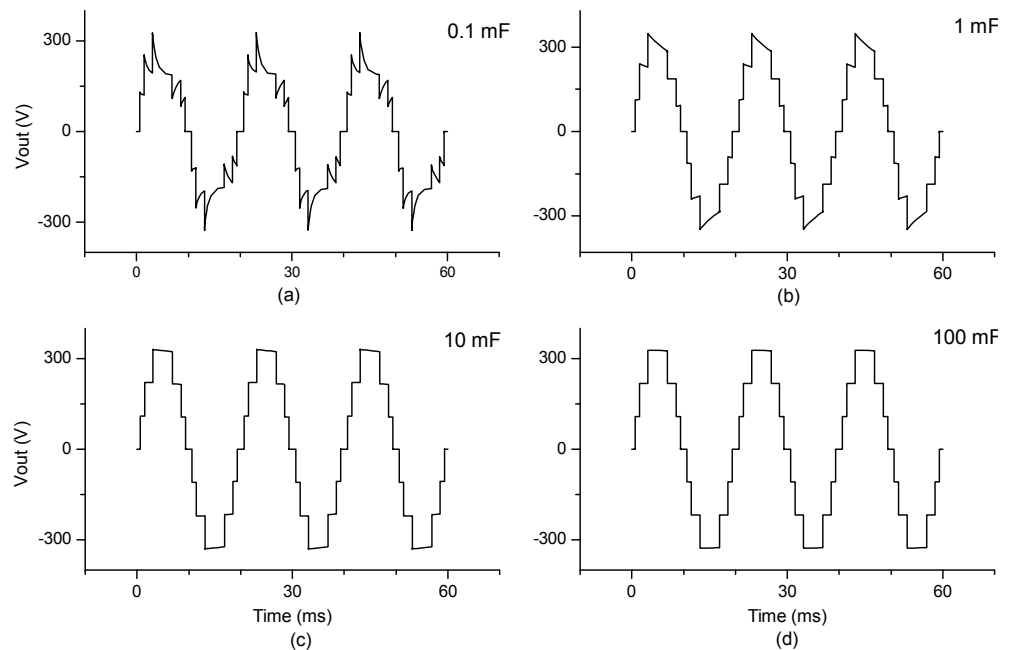
Fig. 6.11 Output voltage waveform with a load of 23.5 Ω, and different values of the storage capacitors: a) 0.1 mF – b) 1 mF – c) 10 mF – d) 100 mF. The irradiance is 1.000 W/m^2 and the temperature is 25°C

Fig. 6.12 shows the variation of current, voltage and power over time at the PV string 1 when the AC load suddenly changes from 23.5 Ω to 17 Ω, for three different values of the storage capacitor (1 mF, 10 mF, 100 mF), at an irradiance of 1000 W/m² and at a temperature of 25 °C. Once the value of the load changes, the working point of the PV strings also changes with a time constant depending on the capacitor size. A value of 100 mF or higher can be useful to achieve a slower variation of the maximum power operating point of the PV strings in case of temporary changes of the optimal load.
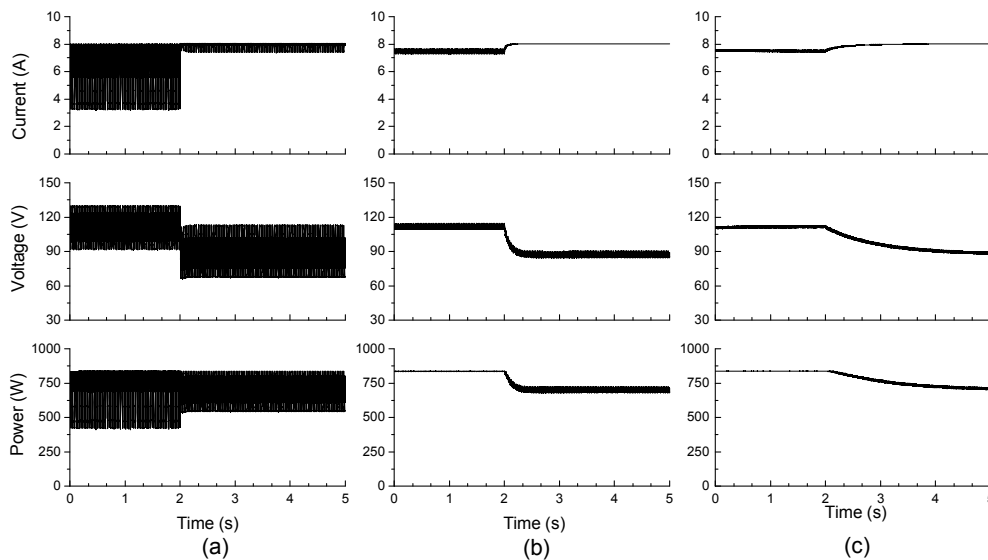
Fig. 6.12 Dynamic behaviour of the system when the load changes from 23.5 Ω to 17 Ω for different values of the storage capacitor: a) 1 mF – b) 10 mF – c) 100 mF. Current, Voltage and Power at the PV string 1 are considered. The load change takes place at t = 2 s.

Finally, the model has been tested at different temperatures. Fig. 6.13 shows how the overall system efficiency depends on temperature for two different values of capacitors (1 mF, 10 mF). As expected, the maximum power generated by the PV strings decreases with increasing temperatures. When the temperature increases from 25 °C to 40 °C, the voltage at the maximum power point drops from 111.4 V to 102 V (Table 6.3), and the AC load that maximises the system efficiency moves to about 22 Ω. The variation of the temperature does not produce any noticeable effect on the THD.
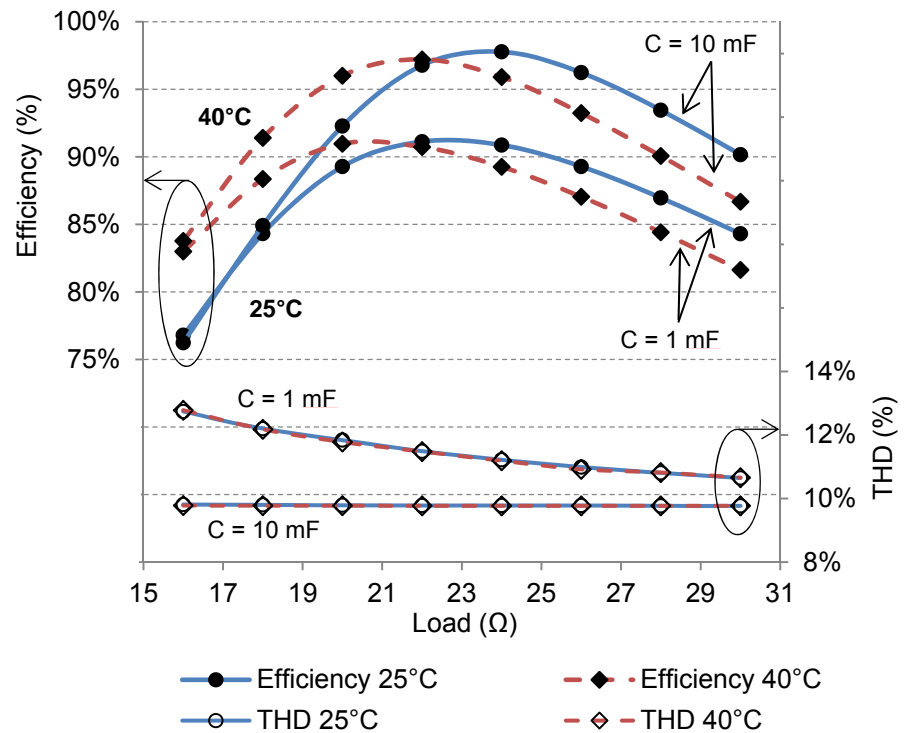
Fig. 6.13 Efficiency of the system and THD with a load varying from 16 to 30 Ω and different sizes of storage capacitors, under a nominal solar irradiance of 1000 W/m² and temperatures of 25 °C and 40 °C

6.3.2 Power loss and efficiency analysis

Fig. 6.14 shows the inverter efficiency, the system efficiency, and the distribution of power losses among the inverter components for different values of the storage capacitors when *IRF3415* and *IRFP360* MOSFETs are used for the DC-blocks and the H-bridge. With these switching devices, an optimal resistive load of 23.5 Ω, and a 10 mF storage capacitor, at an irradiance of 1 kW/m² and a temperature of 25 °C, the efficiency of the overall system is 97.4%. Thanks to the simulation of the complete system, it is possible to calculate that in this condition the strings are delivering nearly 100% of their rated power. About 22% of the 2.6% overall losses are dissipated in the switch-diode blocks (16% of the losses are due to S1-S2-S3 switches and 6% to the D1-D2-D3 diodes). The RC1-RC2-RC3 resistors associated with the capacitor are responsible for a 17% of the power lost in the inverter, whereas the power

majority (61%) is dissipated on the Q1-Q2-Q3-Q4 switches that constitute the H-bridge.

The average power consumption of each MOSFET in the H-bridge is 9.41 W. This loss is due to the drain-source on-state resistance $R_{DS(on)}$ of the device, which can be as high as 0.2 Ω. The switching losses are negligible because in this topology the devices are switched at 50 Hz. A reduction of the losses could be obtained by using power switching devices of newer generation, e.g. super-junction MOSFETs or devices made of Silicon-carbide (SiC) or Gallium-nitride (GaN), showing high blocking voltages with, at the same time, lower internal resistances.

As an example, the *IRF3415* has been replaced with *IRFPS3815*, whereas the *IRFP360* MOSFETs of the H-Bridge have been replaced with the more efficient *IPW65R045C7* super-junction MOSFET. The main difference between the two pairs of devices regards the $R_{DS(on)}$ which is very low in the second couple of devices used in the simulation. The main specifications of the two MOSFET couples have been already provided in Table 6.1.

The low internal resistivity of the MOSFET allows to obtain a considerable increase in the efficiency of the inverter and hence of the complete system. Fig. 6.15 shows a comparison of the efficiency of the system obtained by using the two distinct couples of MOSFETs for different values of the storage capacitors and load. It is possible to observe an increase of the efficiency of 1.5 %, reaching a peak of 98.8% with a 10 mF storage capacitors.

Fig. 6.16 shows the power dissipated by the system divided in:

- PQx: power dissipated in the MOSFETs of the H-Bridge;
- PSx: power dissipated in the MOSFETs of the DC-blocks;
- PDx: power dissipated in the diodes of the DC-blocks;
- PRCx: power dissipated by ESR of the storage capacitors.

The new MOSFETs allow to achieve very low power losses; in particular the power dissipated in the H-bridge are reduced by four times. It is easy to observe that the power dissipated in the capacitor is a substantial percentage of the total power loss in the system, especially with high output power and when the high efficiency MOSFET are used.
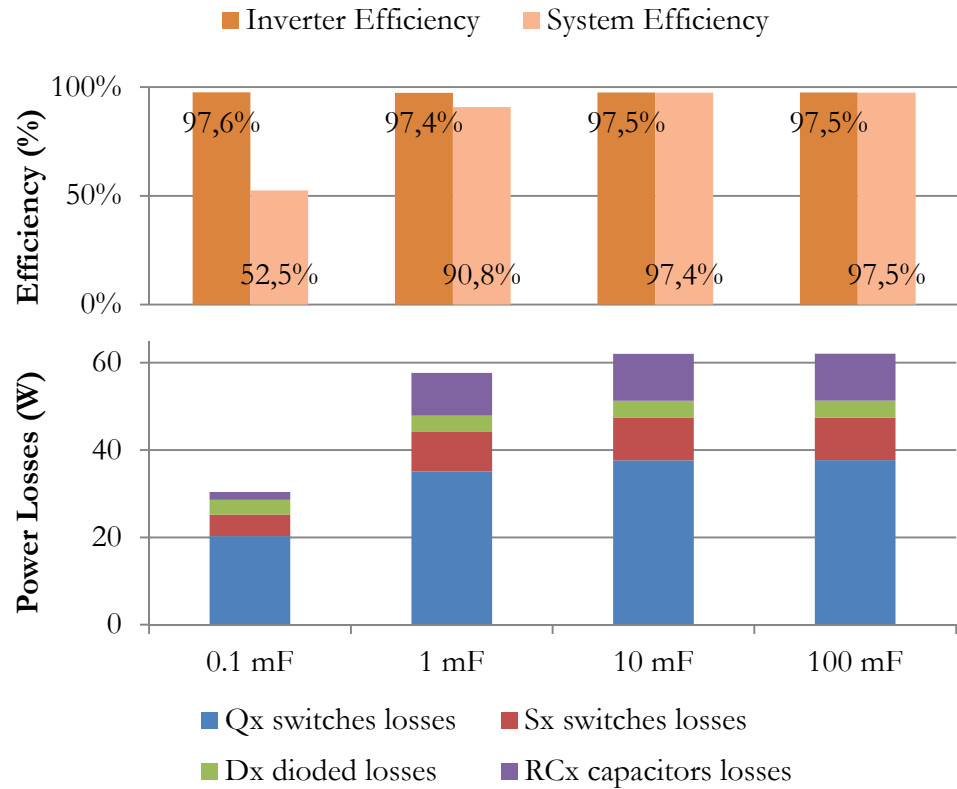
Fig. 6.14 Inverter efficiency, system efficiency, and distribution of power losses among the inverter components for different values of the storage capacitors
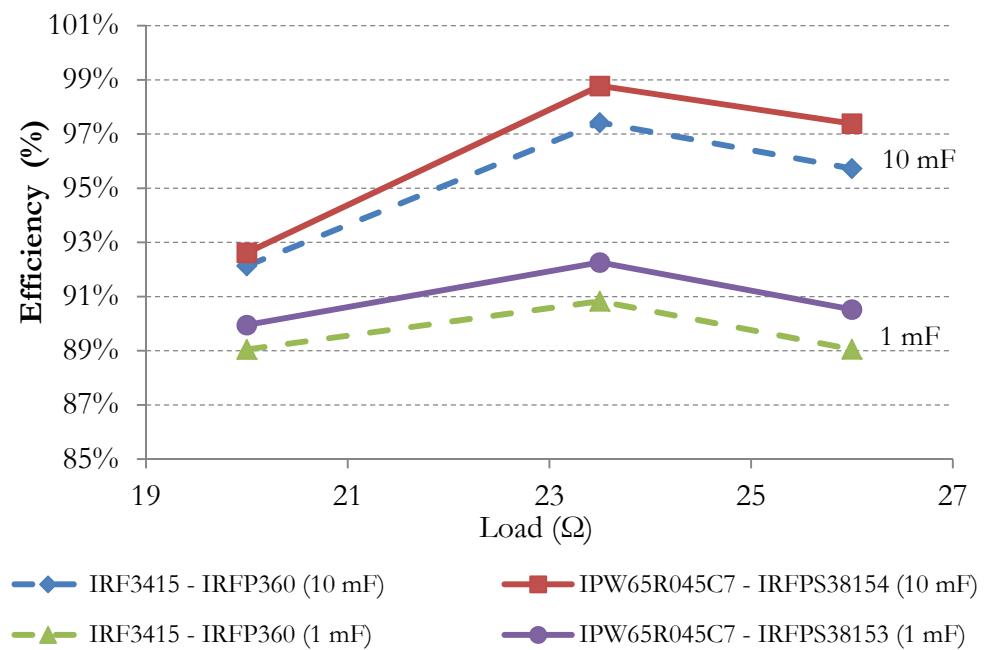
Fig. 6.15 System efficiency of the two couples of MOSFETs for two different values of the storage capacitors and load
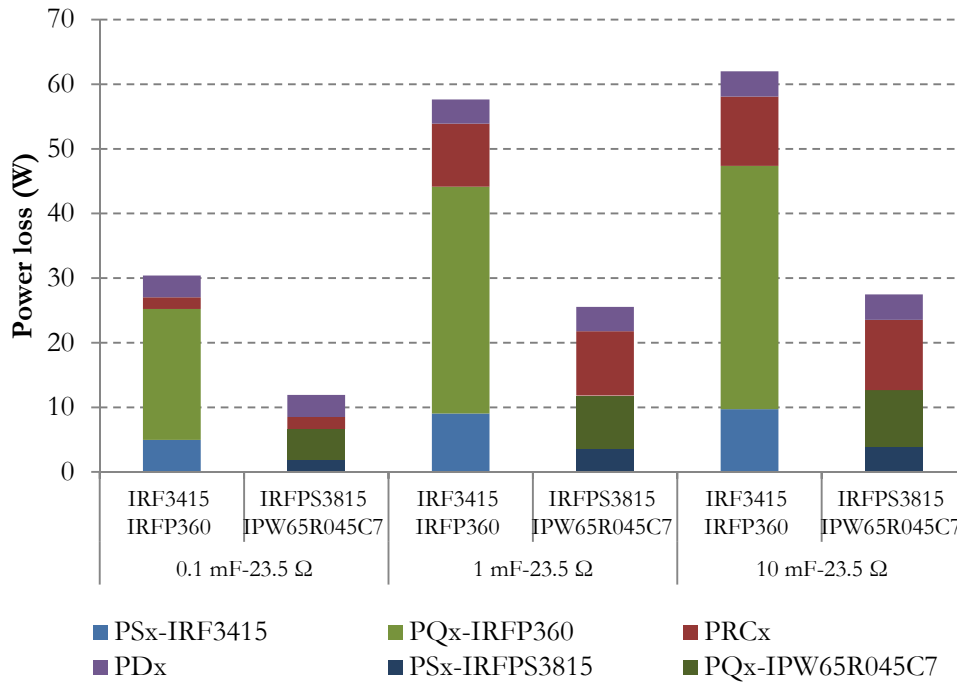
Fig. 6.16 Distribution of power losses among the inverter components for the two couples of MOSFETs and different values of the storage capacitors

6.3.3 Advantages of a complete simulation

The use of PV cells as the DC sources of the inverter allows to obtain more realistic results compared to those provided by ideal DC voltage sources.

In fact, the simulation of the complete PV system allows to gain a deeper insight into the circuit performances, especially when the cells are biased far from their MPP. As an example, Fig. 6.17 shows a comparison between the efficiency of the PV system as obtained by using as DC-sources the PV strings (dotted line), and that obtained with the more common choice of a DC voltage generator (continuous line) [65], [69]. Note that the DC voltage generator parameters (internal voltage V_B and internal series resistance R_S) have been calculated by linearizing the PV module I-V characteristic around its MPP, providing $V_B = 223$ V and $R_S = 14.8$ Ω. It is possible to observe that by using the DC voltage generator the efficiency is overestimated, especially for small capacitances and for loads that are far from the value corresponding to the MPP.
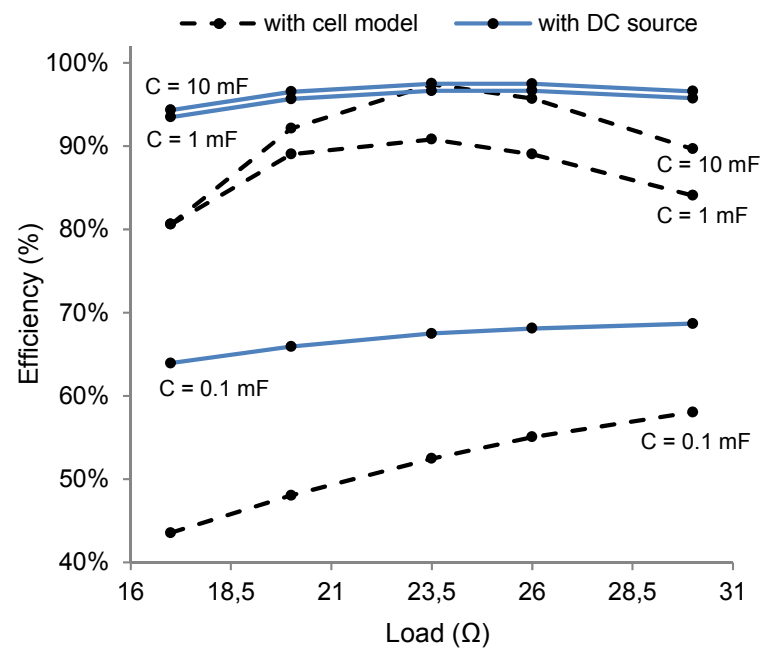
Fig. 6.17 Comparison of the system efficiencies obtained using either PV strings modelled with the double-diode cell model (broken line), or DC voltage generators (continuous line), for different values of the load and storage capacitors. The irradiance is 1 kW/m² and the temperature is 25°C

7 Prototype of the inverter

A prototype of the MLI, based on the architecture described in the previous chapters, has been built and tested with the objective to assess the performance of the inverter and to verify the correct application of the SHE technique. The prototype uses a distributed architecture, with a control circuit associated with each source, that allows to achieve high flexibility and robustness. Experimental measurements have been carried out for different values of voltage sources and loads.

7.1 Introduction, design and characteristics

The prototype is based on the Multi-cell Modified Cascaded topology described in 5.2. It is possible to identify three sections in the inverter. With each source there is an associated DC-block, similar to that already described in the previous chapters, with its own microcontroller which generates the signals used to control the MOSFET. A control board manage the entire system by controlling the DC-blocks and the H-Bridge.

The inverter is composed of three main elements:

- DC-blocks: constituted by a MOSFET, a diode and the relative control circuits; these blocks allow to connects periodically the source with the remaining parts of the circuit. They also integrate a capacitor to store the energy that the source provides when the MOSFET is OFF and therefore the source disconnected from the load. The circuits use a microcontroller to control the MOSFET and monitor voltage and current at the DC-source.

- Master: it is essentially a microcontroller that generates the control signals for the H-bridge, and controls the entire system

by determining the control strategy and by synchronizing the connected DC-blocks generating a clock signal distributed to all the elements;

- H-Bridge: invert the signal obtained by the sum of the outputs of the DC-blocks, producing an alternate waveform that approximate the sinusoidal signal.

This architecture, with distributed intelligence, allows to achieve several advantages:

- each DC-Block is independent and can work independently form the Master and the other blocks;
- it is possible to easily monitor the parameters, e.g. voltage and current, of each source;
- the master controls the system and determines the switching angles and the swapping technique to use, so it is only necessary to modify its code to adjust the control strategy;
- robustness: if the DC-blocks or their relative sources are damaged the system will automatically adapt and continue to work with a reduced number of levels if the load tolerates the output voltage; it is also easy to add redundant blocks to the system.
- the DC-blocks are connected together through simple and standard Ethernet cables, used to transmit the logic signal across the system.
- it is easy to add and remove new sources and produce an output waveform with the desired number of levels.

The system can handle up to 16 sources, and therefore can produce an output waveform with 33 levels. Moreover, the DC-block can be added and removed without shutting down the system.

As DC-blocks are independent and generate the control signal for their MOSFET internally they have to be synchronized to avoid phase shift between

the various levels. The master generates a synchronization signal and send it to all the DC-block to keep the timing consistent.

The communication between the various elements take place through a standard serial bus based on the CAN (Controller Area Network) protocol which has high reliability and noise immunity.

Finally, as each DC-block uses a different source and has a different reference voltage in the system, it is necessary to isolate and translate all the signals that are exchanged between the various boards existing in the system. Every board integrates therefore digital isolators to solve this problematic.

The Fig. 7.1 shows a schematic diagram of the complete system.

The microcontroller software that handle the system has been developed with the C programming language (CCS PICC), whereas the PCB (Printed circuit board) of the each block of the system has been projected with CadSoft EAGLE PCB Design Software. The microcontrollers have been programmed with the use of a programming and debugging software and hardware provided by Microchip Technology Inc. (PicKit2 and PicKit3 and their respective tools).
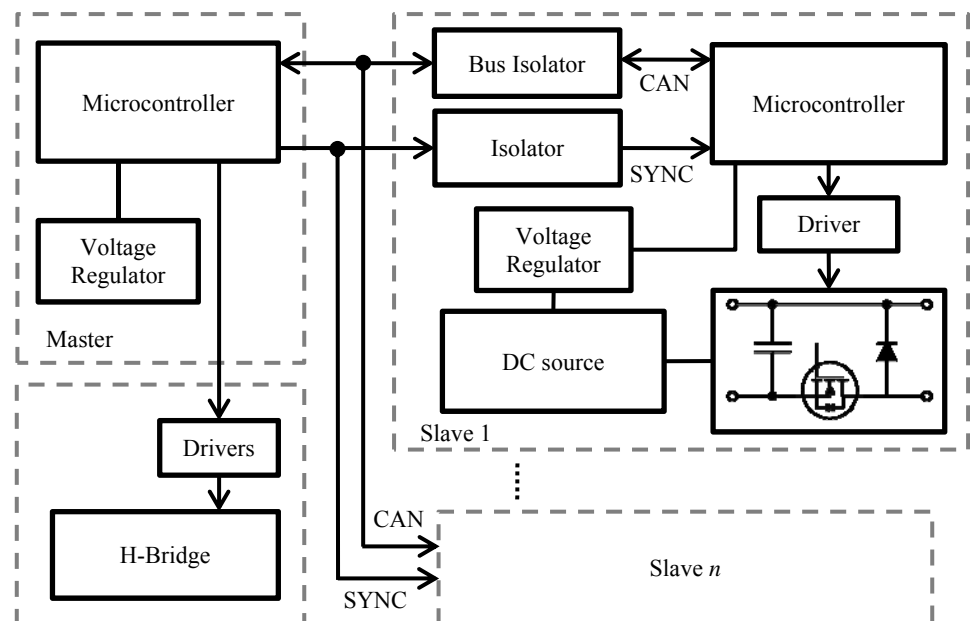
Fig. 7.1 Schematic diagram of the realized inverter

7.2   Elements of multi-level invert

7.2.1   Microcontrollers

A microcontroller (MCU) is small computational unit, designed for embedded applications, that includes on a single integrated circuit a processor core, memory, peripherals, and programmable inputs/outputs. By integrating memory and peripherals it is possible to reduce size and costs compared to a design with separated components.

The CPU (Central Processor Unit) is the "heart" of a microcontroller; it decodes and executes the instruction and controls the peripherals. The memory is usually divided in Program memory (Flash or OTP ROM) used to store the program instructions and RAM (Random Access Memory) used for data created during the execution of the program.

A MCU also includes I/O (Input/Output) lines which allow to communicate with other devices and external peripherals. Usually it also includes analog and digital peripherals and auxiliary components. Some example are timers, comparators, ADC (Analog-to-Digital Converter), DAC (Digital-to-Analog Converter), PWM (Pulse Width Modulation) signal generators, and communication busses like UART, I2C, SPI, CAN, USB, Ethernet.

Most MCUs include internal oscillators to generate the clock for the CPU and the peripherals. Microcontrollers provide also fast response to internal and external events through the interrupt functionality: when an event occur an interrupt signals the processor to suspend current activity and execute an interrupt service routine (ISR) that perform the required processing. An interrupt can for example signal a timer overflow, the change of status of a pin, the completing of an operation, the reception of data, and also wake up the MCU when it is in low power sleep state.

Microcontrollers are easy to use and available in a great variety of models with different dimension and computing capacity. Some microcontrollers can operate a very low frequency and with extremely low power consumption as low as microwatts, or even nanowatts when in idle. Other microcontrollers

have superior performance and dedicated features and can be employed in performance-critical design to act as digital signal processor (DSP).

7.2.1.1 Microcontroller PIC18F25K80

The microcontroller PIC18F25K80 [70] has been chosen to control the various element of the system. This microcontroller is part of the PIC18F66K80 family, a new generation of microcontrollers, produced by Microchip Technology Inc., which integrates a full CAN controller thus allow to avoid the use of external additional controllers.

The PIC18F25K80 is a 28-pin MCU that provides support for the CAN protocol with high efficiency and low costs. Besides the CAN module, this PIC incorporates a range of serial communication peripherals, including two USARTs and a module capable to handle SPI and I2C bus.

It has 32 Kbytes of on-chip Flash Program Memory, 1024 Bytes of Data EEPROM and 3.6 Kbytes of SRAM. Other features include: 8 channels 12-bit ADC; 4 programmable 16 bit timers; a comparator and voltage reference module; on-chip 3.3 V Regulator. A 16 MHz high precision internal oscillator can provide the clock for the CPU and the peripherals, and an integrated PLL (Phase-locked loop) allows to increase further the working frequency up to 64 MHz.

7.2.2 Communication bus

The components of the inverter communicate each other through a serial bus to exchange information useful to monitor the sources and generate the control signals. Among the various serial protocols available, the CAN (Controller Area Network) has been chosen for its speed, reliability, and noise immunity. Other protocols like RS-232 and I2C have been analysed and tested with the prototype, but they have been discarded as they don't provide the same performance and reliability of the CAN. The main advantages of the CAN bus are:

- Strict response times: allows to connect a large number of devices while maintaining stringent time constraints.

- Simplicity and flexibility of the wiring: the bus can be implemented on a twisted-pair network cables; moreover the nodes do not have an address, and they could be added or removed without having to reorganize the system.

- Immunity to interference: the interface chip can continue to communicate even in extreme conditions.

- reliability: hardware managed error detection and retransmission.

- Confinement of errors: each node is able to detect its own malfunction and to exclude itself from the bus.

7.2.2.1 CAN (Controller Area Network)

The CAN bus is a serial digital bus introduced by Bosh in '80 to allow devices to communicate with each other within a vehicle [71]. It has been introduced for automotive applications, but then its usage widespread also in other markets like automation and medical equipment.

It is a message-based protocol with a multi-master architecture; each node is able to send and receive messages, but not simultaneously. Bit rates can reach 1 Mbit/s for network lengths below 40 m.

A message (or "frame") contains an ID (identifier), up to eight data byte, and a CRC field (Cyclic redundancy check); it is transmitted serially to all the all nodes with a non-return-to-zero (NRZ) encoding. The bus has two states: recessive (logical 1) and dominant (logical 0); when the bus is idle the state is at the recessive level. If a node transmits a dominant bit and another one transmits a recessive bit then the dominant bit prevail.

The ID identify univocally the message in the network and can have a length of 11 bits or 29 bits (extended frame format). The ID also represents the priority of the message for the bus arbitration: if two nodes begin sending messages at the same time, only the message with the more dominant ID, i.e. the message with more dominant bits, remains on the bus and is received by all nodes. Therefore messages with the lower value of ID are transmitted with the higher priority.

The transfer layer of the protocol receives messages from the physical layer and transmits those messages to the object layer; besides bit timing and synchronization, it is responsible for message framing, acknowledgement, arbitration, error detection, and fault confinement.

The physical layer (ISO 11898-2) defines the electrical aspects but not the mechanical aspects (connectors, cables, pin-outs). The electrical implementation is a multi-dropped balanced line configuration with a resistor termination (120 Ω) at each end of the bus. The balanced pair signals can be carried in twisted pair wires and shielded cables to reduce interferences.

The signals necessary are CAN-Low (CAN-), CAN-High (CAN+), and the supply pins (ground and power). A dominant state is asserted by switching the CAN- to ground and CAN+ to the bus voltage thereby forming a current path through the termination resistors, which are therefore an essential component, and not required only to limit wave reflection. In a recessive state the signal lines and resistors remain in a high impedances state and the voltages on both the lines pull towards ½ rail voltage.

There is no clock signal; each node has its own clock and synchronization is done by dividing each bit into segments (synchronization, propagation, phase 1, and phase 2), the timing of which can be adjusted according to network requirement. The sample point falls between phase segment 1 and phase segment 2.

Even if the used microcontroller integrates the CAN controller, it is not connected directly to the bus, but through a transceiver which convert signal levels from the physical bus to a level correct for the CAN controller.

7.2.2.2 CAN transceiver

The Master and each DC-block integrates a transceiver. The model of transceiver used in the system is the ADM3054 by Analog Devices, Inc. [72]. It is a 5 kV rms signal isolated controller area network (CAN) physical layer transceiver that employs iCoupler technology [73] to combine a 3-channel isolator and a CAN transceiver into a single package.

The device implements the isolation on the logic side of the interface. Therefore, it has two main sections: a digital isolation section and a transceiver

section (Fig. 7.2). Two channel of the isolator are used for the CAN signals to isolate the microcontroller, i.e. the CAN controller, and the physical layer bus. The third channel is a logic signal, related to the status of the supply voltage on the bus side, that can be used to detect loss of power on the bus side.

The ADM3054 is capable of running at data rates of up to 1 Mbps, and has several protection mechanisms like current limiting, thermal shutdown, and protection on the bus pins (CANH, CANL) against short circuits.

The iCoupler technology is an isolation barrier that uses chip scale transformer windings to couple magnetically the signals to the two sides of the barrier. Inputs are encoded into waveforms that excite the primary transformer winding, and the induced waveforms at the secondary winding are decoded into the original binary value. The isolation is therefore provided without the detrimental characteristics of the electro-optical conversions present in optocouplers, i.e. high power consumption, and large timing that constrain data rate. The integration of CAN controller and isolator provides clearly advantages reducing size and cost relative to optocoupler implementations. This solution delivers also performance benefits with higher timing accuracy, reduced power consumption, and lower supply voltages.
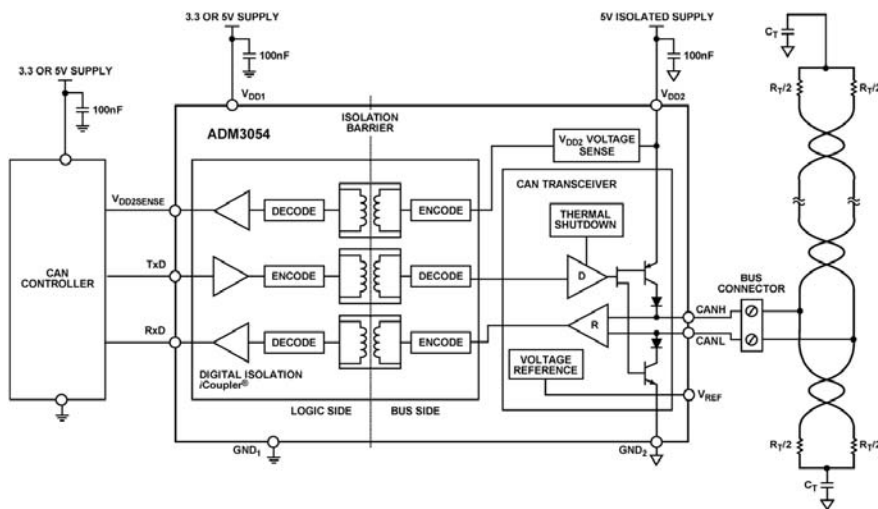
Fig. 7.2 Functional block diagram of ADM3054 transceiver and typical application circuit

7.2.3 Master Control board

The main control board, called "Master" has the function to control and supervise the complete system; it:

- determines the control strategy of the various elements of the inverter;

- synchronizes the DC-blocks generating a clock signal distributed to all the elements;

- communicates with the DC-blocks receiving the voltage and current measurement of each DC-sources, and sending to them the switching angles they have to generate.

- generates the control signals for the MOSFET of the H-bridge.

7.2.3.1 Hardware

The board, whose schematic is reported in Fig. 7.3, includes a PIC18F25K80 microcontroller (paragraph 7.2.1), a voltage regulator and an ADM3054 CAN transceiver (paragraph 7.2.2.2).
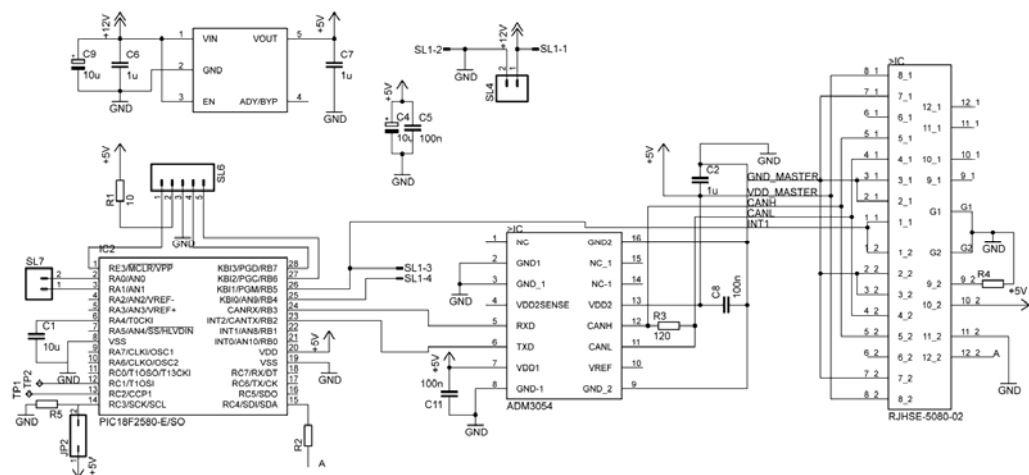
Fig. 7.3 Schematic of the master

The pins CANRX and CANTX of the microcontroller are utilized for the CAN communication bus and connected to the transceiver to interface with the physical layer of the bus.

The generic pins B4 and B5 are used to output the control signal of the H-bridge; one of the two signal is also used to synchronize the DC-blocks.

Two pins can be used to read generic analogic signals such as the output load voltage for control purpose, that are converted through the integrated 12-bit ADC (Analog-to-digital converter).

The supply voltage of the board is minimum 10 V, and a SPX3819M5-L 5-0 [74] voltage regulator is used to supply the various elements of the board. The SPX3819M5-L-5-0 is a low noise, high accuracy (1%) linear voltage regulator with a fixed output of 5 V.

The board also includes two RJ-45 connectors to connect the board with the other elements of the system and an ICSP (In Circuit Serial Programming) connector that allows to program and debug the code of the microcontroller without removing it from the board.

7.2.3.2   Software

The microcontroller has been programmed to generate the suitable control signals and to communicate with the DC-blocks. The code implements two distinct interrupt routines and a main routine that can be interrupted by the other two that have an higher priority.

The first interrupt routine generates the 50 Hz signal to control the H-bridge MOSFETs by alternating a high and low output value on the pins B4 and B5. The procedure is executed every 10 ms with the help of a timer integrated in the PIC.

The second interrupt routine reads the data sent by the DC-blocks on the CAN bus. It receives asynchronously the status of each DC-block (id, voltage and current of the source) and stores the data in a vector. This routine is executed every time the microcontroller receives data in the buffer.

After the initialization of the microcontroller, the main routine periodically checks the data stored in the vector, puts in order the data and sends to the DC-blocks the timing necessary to generate the correct control signal. These timing are stored in a look-up table and depends on the number of DC-blocks connected (levels of multilevel inverter) and the voltage level of each block. The master chooses the timing to send to each slave in order to

implement the swapping techniques described in 5.3.3. A jumper allows to select the swapping technique to use.

If a DC-block does not send any data to the master within a certain time interval (e.g. the DC-block is damaged or removed from the system), it is marked as disconnected and the master excludes it from the control strategy. If a DC-block is added in the system the master takes care to add its status to the vector.

7.2.4 DC-blocks

Each DC-block, also called "Slave" is connected with an independent DC-source. The main function of these blocks is to generate suitable waveforms that are then summed to obtain a final approximation of the sinusoidal waveform. A DC-block integrates a microcontroller, the functions of which are:

- to generate the control signal for the MOSFET, based on to the timing strategy decided by the Master;

- to monitor the DC-source by reading its voltage and current and to send the data to the Master;

7.2.4.1 Hardware

The board, the schematic of which is reported in Fig. 7.4, includes a storage capacitor, a diode, and a MOSFET controlled to connect and disconnect periodically the source to/from the remains part of the inverter, making possible to obtain different voltage level on the load.

The logic part of the board includes a PIC18F25K80 microcontroller (paragraph 7.2.1), a voltage regulator, an ADM3054 CAN transceiver (paragraph 7.2.2.2), an ADUM1280 isolator [75], and an INA283 current sensor [76].
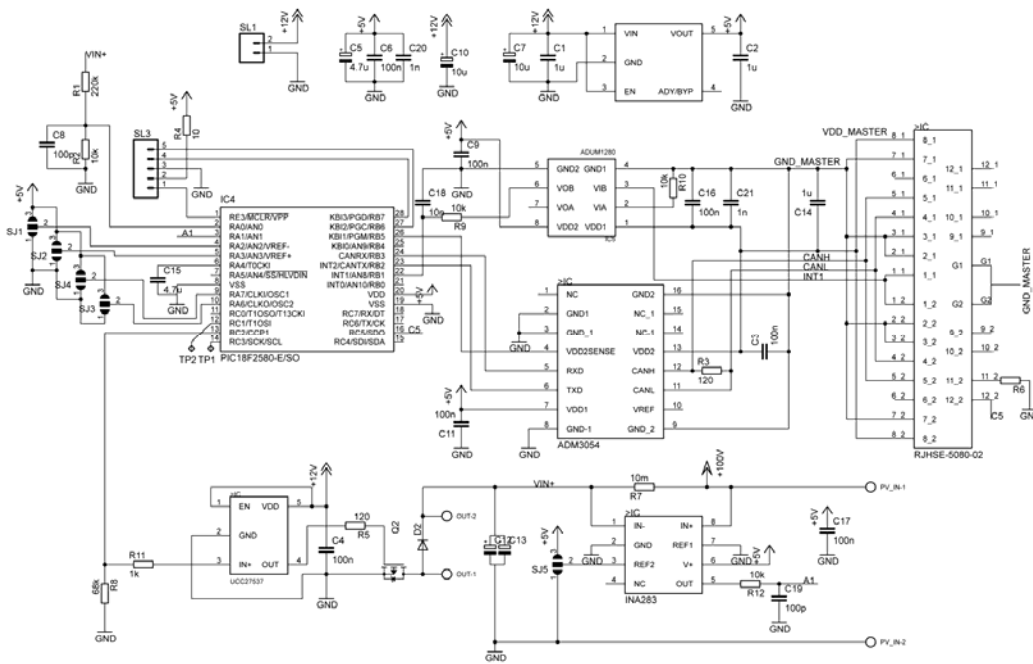
Fig. 7.4 Schematic of a single DC-block

As in the master board, the pins CANRX and CANTX of the microcontroller are connected to the ADM3054 transceiver that provides isolation and an interface to the CAN bus. The voltage regulator provides the 5 V necessary to supply the integrated circuits present on-board.

To avoid conflicts on the communication bus, every slave connected to the system must have an unique address. These boards have four pins that can be used to define an unique address; the four pins allow to set $2^4 = 16$ different combinations, and therefore to connect up to 16 DC-blocks on the system obtaining an output waveform with 33 levels.

Voltage and current of the associated DC-source are read by the 12-bit ADC integrated in the microcontroller. The voltage of the source is read across a voltage divided that allow to obtain a voltage value in the range of 0–5 V from an input voltage of 0–115 V, with a resolution of about 28 mV.

The current drawn by the source is read through a sensing resistor and an integrated differential amplifier INA283. The resistor (10 mΩ) is inserted between the positive input terminal of the source and the storage capacitor, allowing to monitor the current that flows out of the source. The amplifier has a fixed gain of 200 V/V and rises the voltage across the resistor up to 5 V

which is the input limit of the microcontroller, allowing to monitor current up to 2.5 A with a resolution of about 0.6 mA.

The master sends a synchronization signal to every slave; the microcontroller receives this signal on the pin INT1, a special pin that allows to trigger a software interrupt routine that handle the synchronization. Each slave has a different voltage reference and it is therefore necessary to isolate all the communication lines that connect the master and DC-blocks. The synchronization signal passes through the ADUM1280, an innovative digital insulator based on the Analog Devices iCoupler technology, that provides higher performance than optocouplers and other integrated couplers.

The MOSFET used in the board is a IPB038N12N3 [77] that can sustain up to 120 V and 120 A, with a very low $R_{DS(on)}$ (3.8 mΩ) which allow to maintain high the efficiency of the system as shown in 6.3.2. Being a power device and the microcontroller, which has a maximum output current of 25 mA per pin, is not able to drive its gate directly in a fast and efficient way. Therefore it is necessary to use a MOSFET driver able to charge and discharge the gate capacitance in the shortest possible time, ensuring fast switching times and therefore low power loss (paragraph 3.9.3.1). The driver used is a UCC27537 [78], which provides up to 2.5 A current source capacity and up to 5 A current sink capacity, with very low rising and falling times and propagation delays. A small resistor between the output of the driver and MOSFET has been used to limit the peak current and reduce voltage spike on the drain and EMI (Electromagnetic interference) disturbance.

The diode used is the MBRS3100T3G Schottky Rectifier [79] which ensure very low losses thanks to the small forward voltage and small capacitance.

7.2.4.2   Software

All the DC-blocks are identical and their microcontrollers have been programmed with the same code. The code implements three distinct interrupt routines and a main routine that can be interrupted by the other three that have an higher priority.

The main routine starts with the initialization of the microcontroller consisting in the configuration of the various integrated peripherals and in the determination of the address of the board by reading the four pins dedicated to this functionality. After the configuration, the microcontroller periodically uses the ADC to read the voltage and current of the associated source, and then sends the data over the CAN bus to the master.

The three interrupt routines are used to read the data sent by the master, and to generate the control signal of the MOSFET. The CAN interrupt routine is executed every time the microcontroller receives data in the buffer; the microcontroller reads the data sent by the master that contains the timing of the waveform that has to be generated.

The external interrupt routine is executed every time the signal on the pin INT1 (synchronization signal) makes a transition low-to-high; this routine resets all the timers and ensures that all the DC-blocks start the waveform generation at once. The timer interrupt routine is executed every 10 ms and generates the control signal on the pin C2 which is connected to the driver of the MOSFET; the timing of the generated signal is that provided by the last data reception on the CAN bus and sent by the master to implement the SHE and swapping technique.

7.2.5 H-Bridge

An H-Bridge circuit has been used to obtain an output voltage waveform with positive and negative polarity as described in the previous chapters. The board includes two Half-Bridge drivers and four MOSFETs; the schematic is reported in Fig. 7.5.

Two IR2106 [80] Half-Bridge drivers have been utilized to drive the two MOSFET couples that constitute the H-Bridge. These drivers are designed to be fully operative up to 600 V. The dead time control is not integrated in the driver, but the master generates the control signals with a small delay between the edges to ensure that the two MOSFET are never in conduction at the same time.
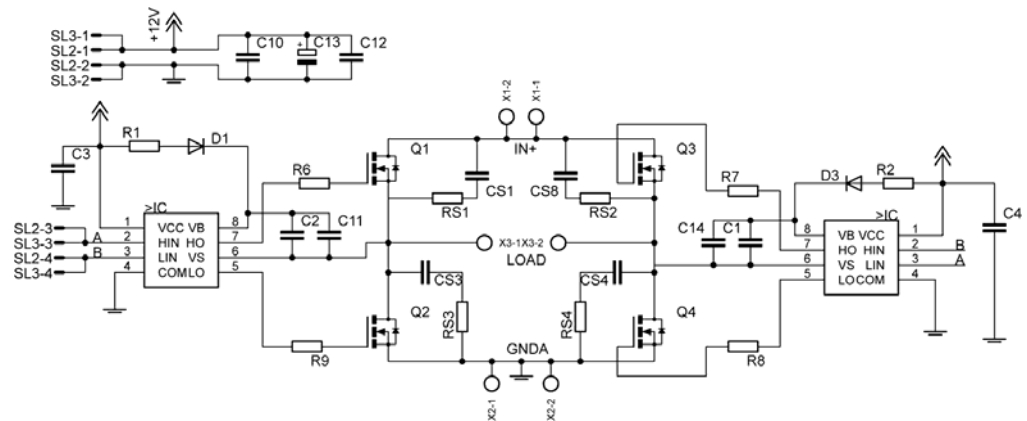
Fig. 7.5 Schematic of the H-bridge

The driver integrates a level shifter to drive the high-side MOSFET and a boot-strap configuration is used to provide the supply voltage to the high-side driver, whose reference is floating because depends on the status of the low-side switch. The bootstrap technique, which has the advantage of being simple and low cost, requires a diode and a capacitor that store the energy for the high-side driver. The capacitor is charged when the Vs voltage goes below the driver supply voltage V_{CC}, i.e. the low-side switch is turned on and the high-side switch is turned off. When the low-side switch is turned off and high-side switch is turned on, the capacitor provides the voltage above the floating V_S that allows the high-side switch to operate correctly, and the diode, which is now reverse biased, blocks the rail voltage.

Each driver has two logic inputs which are connected to the master control board. The two inputs are compatible with CMOS and TTL technology which allows to connect the microcontroller directly to the driver.

The MOSFETs used are STW88N65M5 [81], a state-of-art super-junction device which is able to sustain up to 710 V with a drain-source on-resistance below 25 mΩ.

The images of the realized boards are shown in Fig. 7.6.

7.3 Measurement and results

To verify the correct behaviour of the realized prototype, several tests have been done. The obtained experimental results are shown in the following.

GWInstek GPS-3303 voltage generators, which allow to regulate the output voltage up to 63V, have been used as DC-sources of the various DC-blocks. The results reported are relative to a 7-levels and a 11-levels versions of MLI prototype. Measurements are made with a *LeCroy Wavesurfer 434* and *AP015* current probe.

7.3.1 Tests on 7-levels inverter

Fig. 7.7 shown the control waveforms generated by the three DC-blocks of the 7-level MLI prototype, and the synchronization signal. The image allows to verify the correct behaviour of the various elements that constitute the prototype; all the signal are synchronized and generated with the correct timing to implement the SHE technique for 3 switching angles, so to minimize the 3rd, 5th, 7th harmonics. The duty cycle swapping technique, applied here every 70 ms, has been used to assure the even utilization of the DC-sources.

The Fig. 7.8 shows the voltage waveform at the load terminals and its harmonic spectrum for the realized prototype, with a resistive load of 100 Ω and DC-sources set at 12 V. Fig. 7.9 shows the output voltage and the spectrum when the three DC-sources are set to 63V.

It is possible to evaluate the contribution of the various harmonics to the output voltage waveform and calculate the THD by using the (5.1) applied at the first 20 harmonics:

$$THD = \frac{\sqrt[2]{V_2^2 + V_3^2 + \cdots + V_{20}^2}}{V_1} \approx 9.8\ \%.$$

The value of THD obtained is comparable with the SPICE simulation results (9.7%, cf. paragraph 6.3.1).
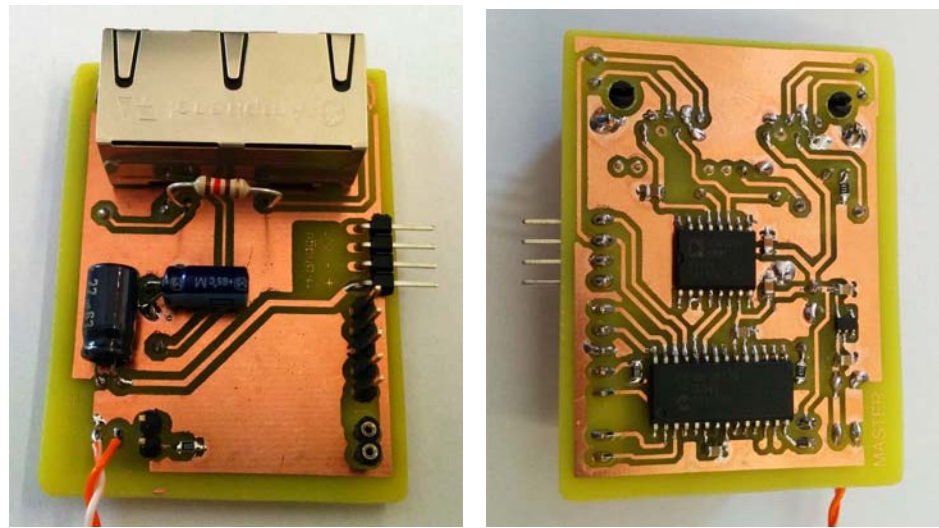
(a)
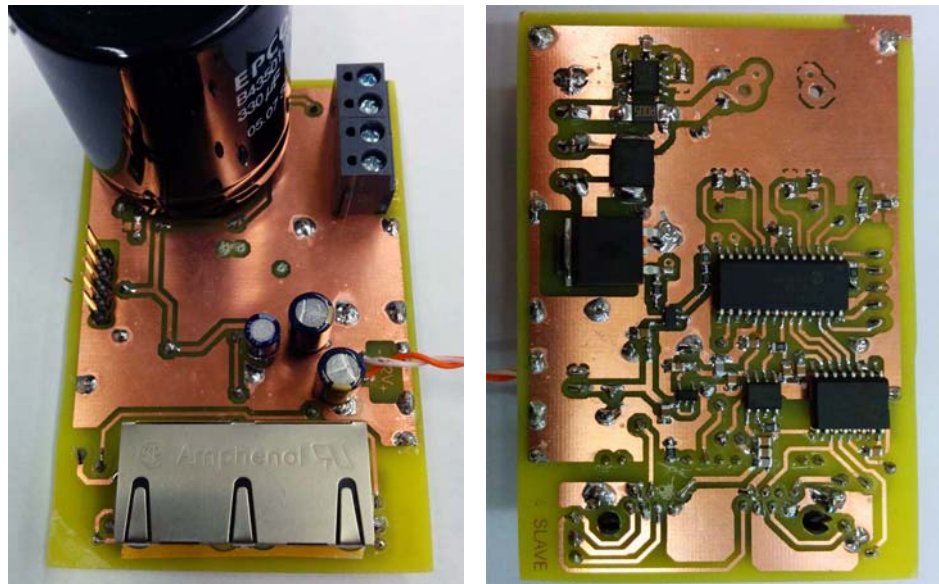
(b)
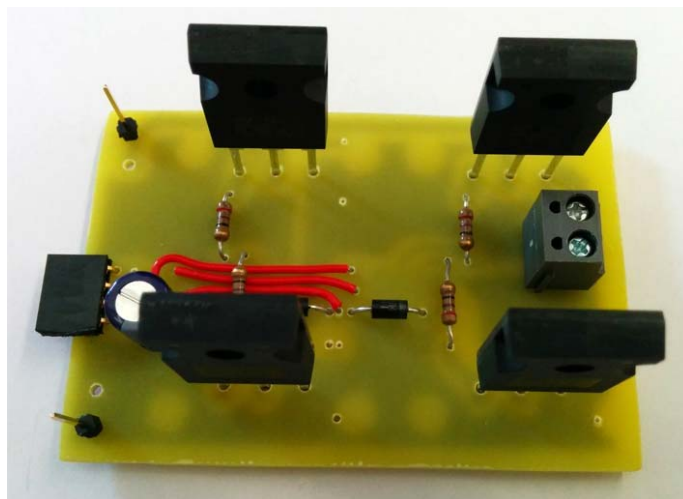
(c)

Fig. 7.6 Images of the realized boards: a) master, b) slave, c) H-bridge

Fig. 7.7 MOSFETs control waveforms of each DC-blocks (channel 1-2-3) and synchronization signal (channel 4) for the 7-level MLI prototype
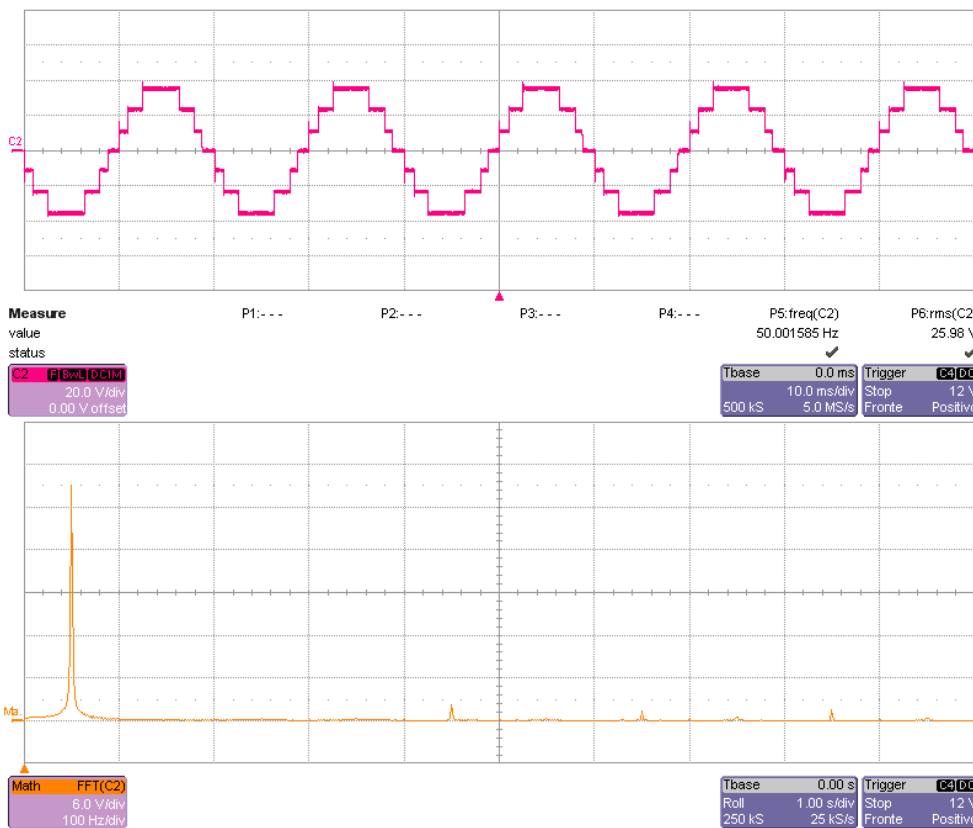
Fig. 7.8 Output voltage waveform and spectrum produced by the MLI prototype with 7 levels enabled, 12 V DC-sources, and a load of 100 Ω
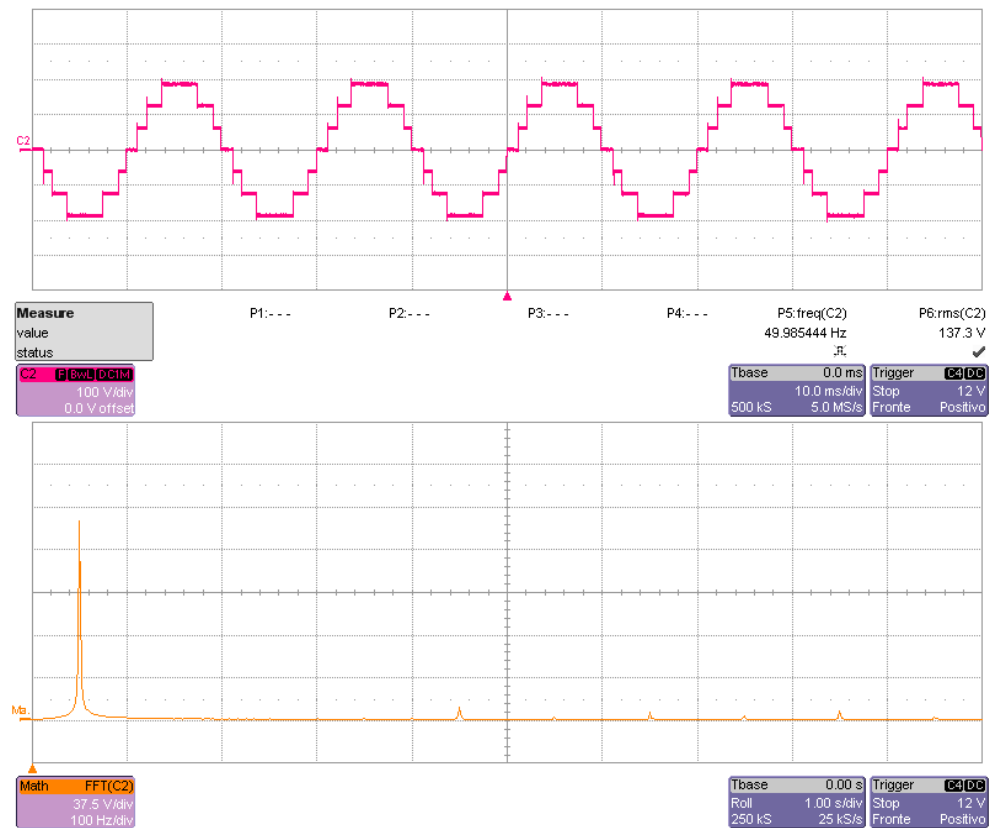
Fig. 7.9 Output waveform and spectrum produced by the MLI prototype with 7 levels enabled, 63 V DC-sources, and a load of 100 Ω

The efficiency of the inverter is above 97% in all the tested conditions, and reach a value over 99% with 12 V sources and a load of 100 Ω. These data do not take into account the consumption of the logic part of the DC-blocks (microcontroller, transceiver, isolator, driver) that amounts to about 50 mW for each slave, and 450mW for the master and H-bridge drivers. The power consumption of these parts has not been optimized, and consistent reduction of these losses are therefore possible.

As described in paragraph 5.3.3, a second duty cycle swapping technique has been implemented on the prototype to uniform the DC-source voltage. The DC-block connected with the source at higher voltage generates the control signal with the smaller switching angle and higher duty cycle, whereas the DC-block connected to the source with lower voltage value produces the control signal with the higher switching angle and lower pulse duration.

As an example, Fig. 7.10 shows how the control signals are modified when the DC-sources voltages change as reported in the relative legend.
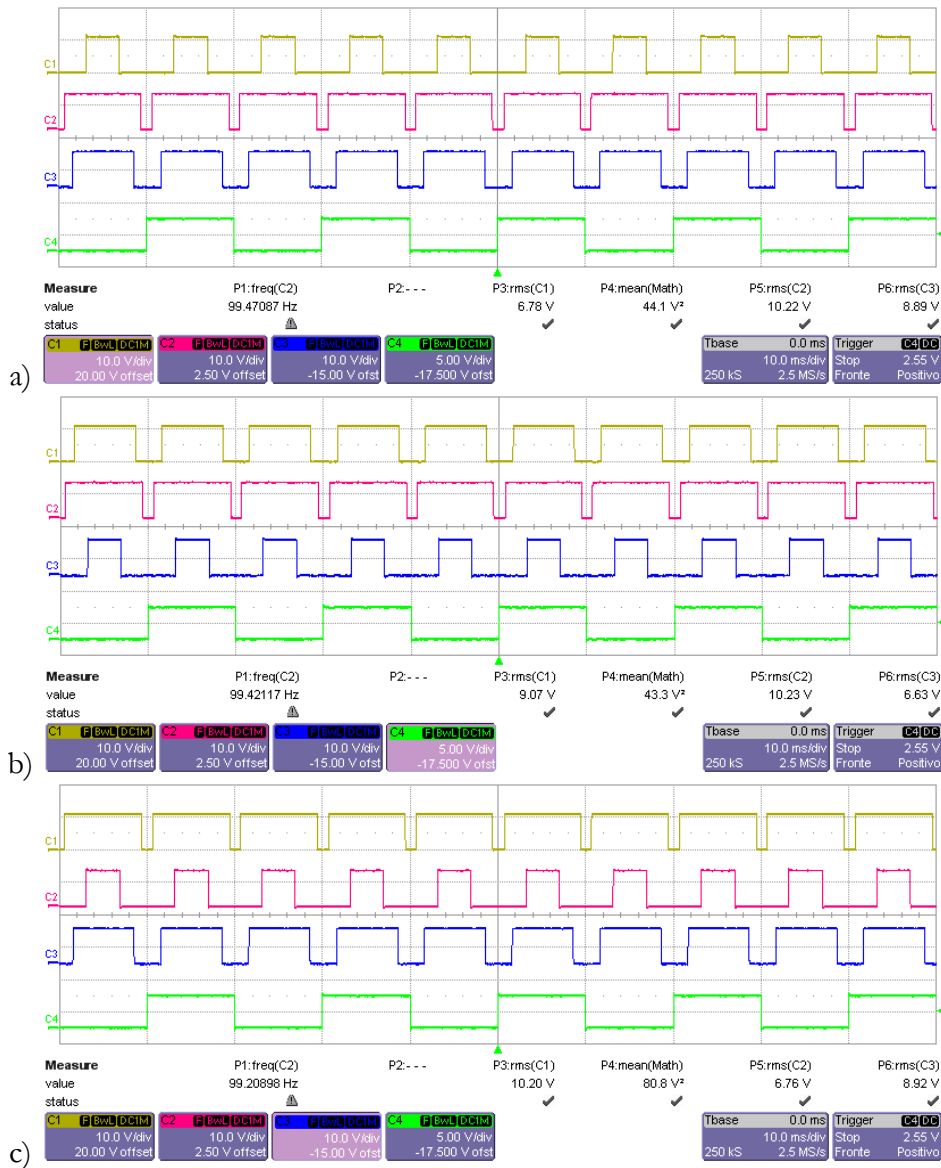
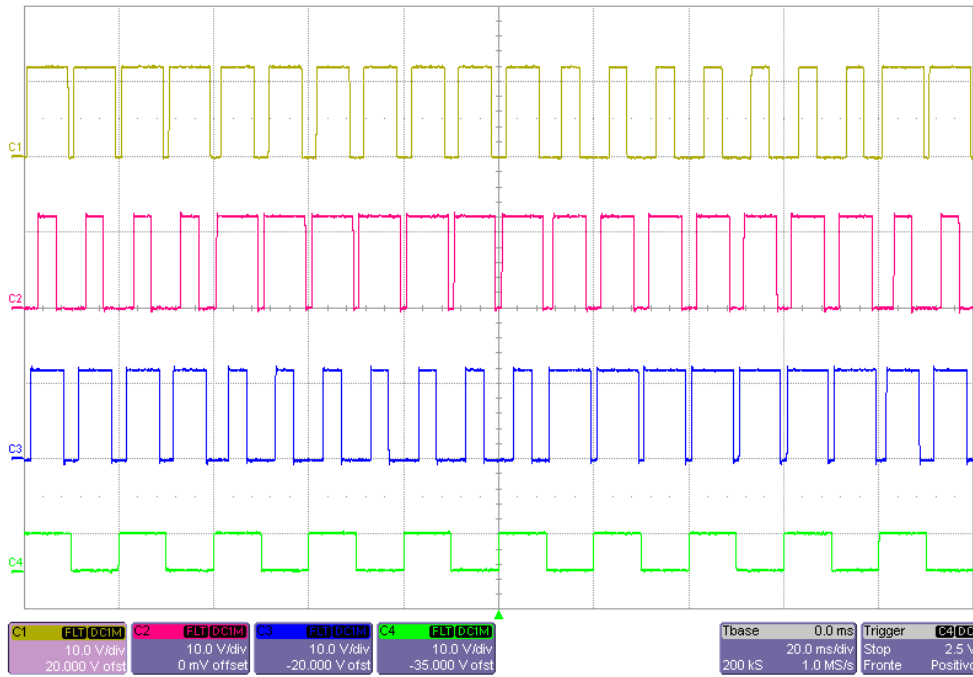

Fig. 7.10 MOSFETs control waveforms of each DC-blocks (channel 1-2-3) and synchronization signal (channel 4) for the 7-level MLI prototype with swapping based on the voltage level applied

The voltage applied to each DC-block is as follow:

Image	DC-source 1	DC-source 2	DC-source 3
a)	11.5 V	12.5 V	12 V
b)	12 V	12.5 V	11.5 V
c)	12.5 V	11.5 V	12 V

7.3.2 Tests on 11-levels

The Fig. 7.11 shows the output voltage and the relative spectrum for a 11-levels version of the realized prototype, with a resistive load of 100 Ω and DC-sources set at 12 V. Fig. 7.12 is relative to DC-sources set at 63V and a load of 100 Ω. Fig. 7.13 is relative to DC-sources set at 63V and a load of 225 Ω. Fig. 7.14 shows the voltage, current and power on a nominal 100 Ω load for the 11 levels MLI prototype and 63 V DC-sources; the average power delivered to the load is 349 W, whereas each DC-source provide about 73 W.

The calculated THD is: 6.5% for Fig. 7.11 (12 V, 100 Ω); 5.8% for Fig. 7.12 (63 V, 100 Ω); 5.4% for Fig. 7.13 (63 V, 225 Ω). The efficiency of the inverter is above 95% in all the tested conditions, and reach 99% with 12 V sources. Again, the power losses do not include the consumption of the logic part of the DC-blocks (about 50 mW for each slave), and the master connected to five slave and the H-bridge drivers (about 600mW).

Fig. 7.11 Output voltage waveform and spectrum produced by the MLI prototype with 11 levels enabled, 12 V DC-sources, and a load of 100 Ω

Fig. 7.12 Output voltage waveform and spectrum produced by the MLI prototype with 11 levels enabled, 63 V DC-sources, and a load of 100 Ω
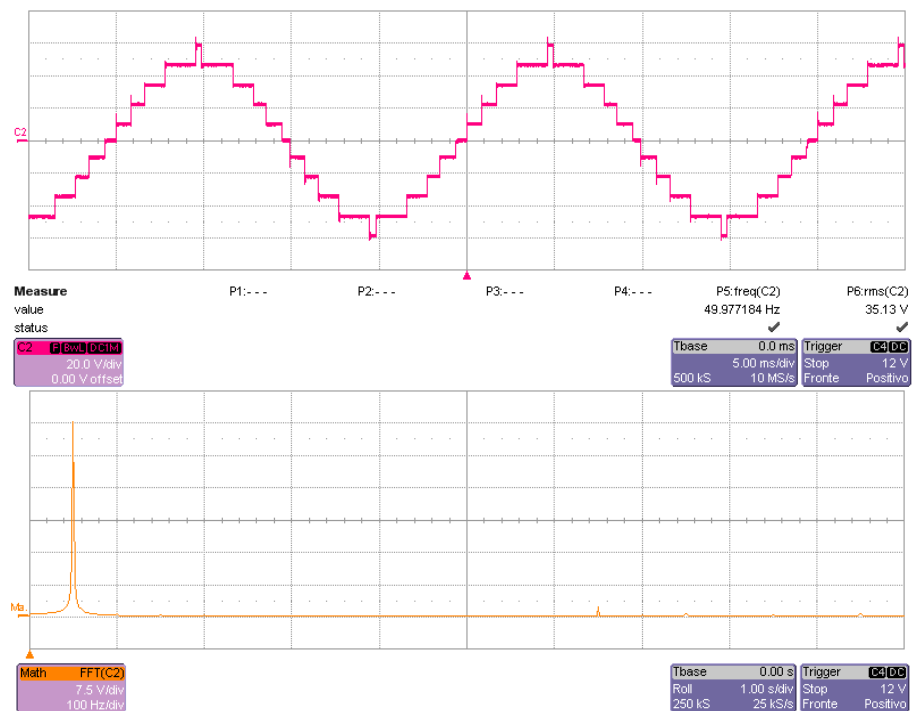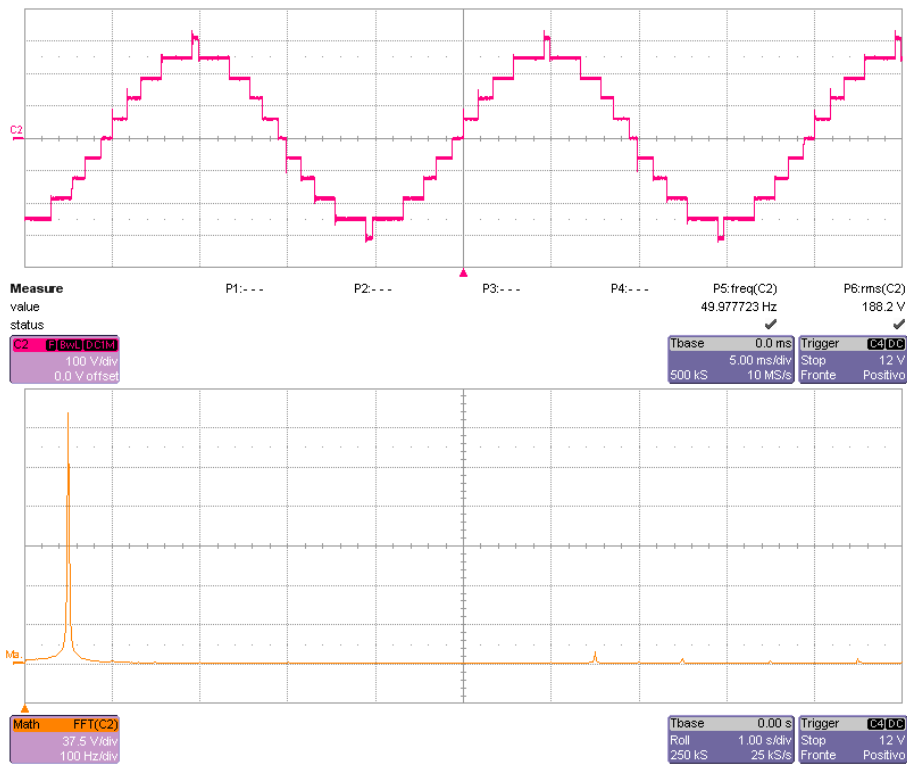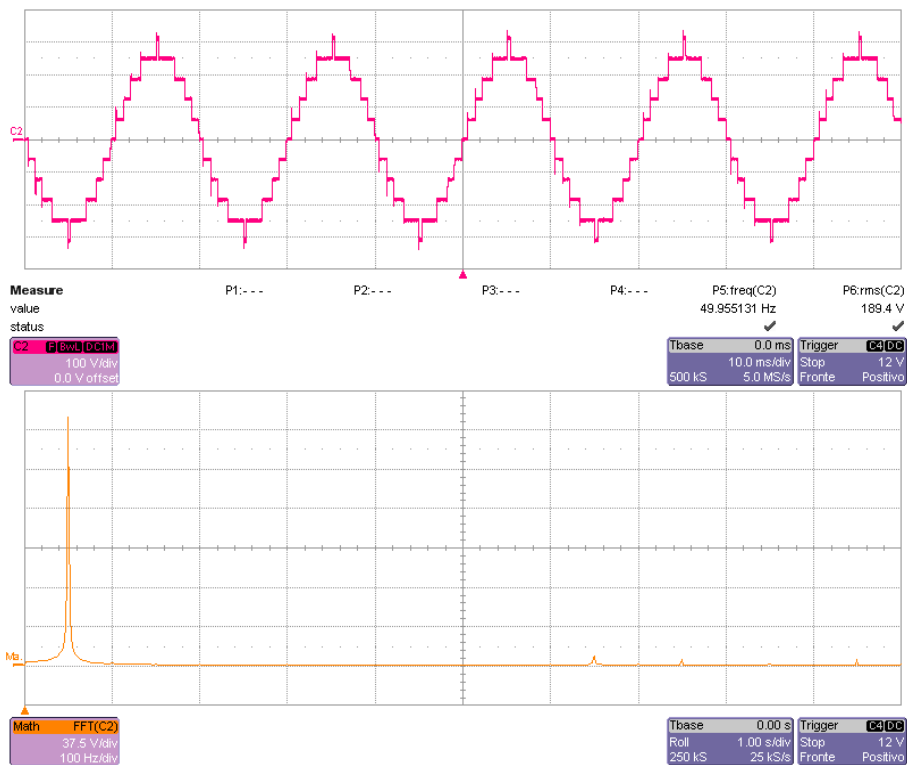

Fig. 7.13 Output voltage waveform and spectrum produced by the MLI prototype with 11 levels enabled, 63 V DC-sources, and a load of 225 Ω
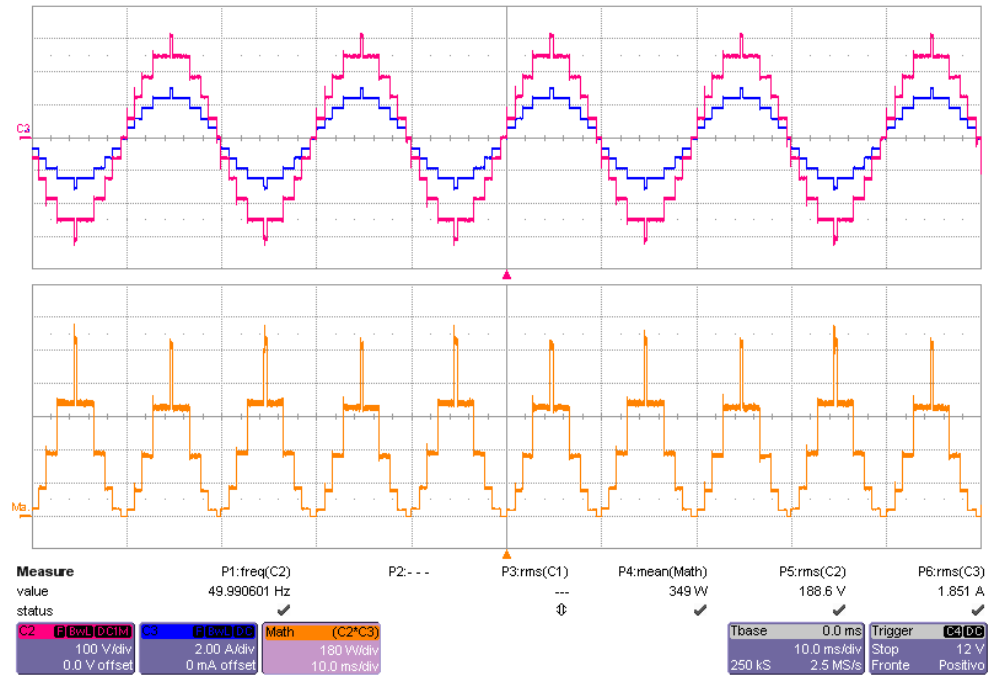
Fig. 7.14 Voltage, current and power on a 100 Ω load for the 11 levels MLI
prototype and 63 V DC-sources

8 Conclusions

8.1 Conclusions

The cost of photovoltaic energy is fast dropping in the last years and PV system are becoming almost cost competitive with conventional sources. The PV market status and a short review of the technologies for the construction of the PV cell have been considered in chapter 2. A description of the PV cells, the mechanism behind the conversion of the light into electrical energy, and the factors that limit the cell efficiency have also been shortly discussed. The chapter includes a description of a simple electrical model of the PV cell and its parasitic elements, and a double-diode model that model with major precision the recombination on the space-charge region, allowing to obtain better approximation at low polarization levels.

In parallel with the growth of the PV market, has increased the need of high efficiency and reliable inverters to convert the DC power in AC. Among the various inverters topologies, multilevel inverters are gaining interest thanks to the advantages that they provide over traditional inverters. An overview of the multilevel inverter topologies and their advantages, which include higher efficiency and quality of the output voltage, has been provided in chapter 3. The chapter includes an analysis of the three basic multilevel topologies with their advantages and drawbacks. In particular, a disadvantage of the MLI is the high number of power semiconductor switches, that increases costs and complexity of the system. A topology denominated multi-cell modified cascade, which solve some of the problems of the traditional MLI topologies, has been discussed and considered as the basis for this thesis work.

Multilevel inverters allow to obtain high-quality waveforms even operating at low switching frequencies thanks to the use of the SHE technique.

In fact, operating at low frequencies, the first harmonics in the spectrum of the output waveform are very close to the fundamental and therefore difficult to filter. However, the SHE technique allows to eliminate these low order harmonics, maintaining low the total harmonic distortion, and allows to achieve high efficiency because, thanks to the low switching frequency, the switching losses are negligible.

The chapter 3 also includes an analysis of the main characteristics and the power losses of power devices such as diodes and MOSFETs, with comments about some technologies (e.g., super-junction) and materials (e.g., SiC, GaN) that could allow to overcome the limits of traditional silicon power devices, increasing the converters efficiency. A thermal model for the power MOSFET, with information on the heating rate and the dissipation of the generated heat, has also been shortly discussed.

A power loss measurement apparatus based on the measurement of the heat-flux generated by a switching device is discussed in chapter 4. The chapter include a short review of the problematic that could affect the power loss measurement with traditional electric methods, and an overview of existing calorimetric methods. The realized calorimetric apparatus, based on a custom micromachined heat-flux sensor, allows the estimation of the power dissipated by a semiconductor device in steady-state conditions that is independent from electrical quantities, and therefore not affected by the errors of traditional measurement instruments. The set-up includes a thermoelectric module that absorbs the heat and keeps the device at the same temperature of air in order to minimise the heat exchanged and thus the heat leakage without the use of closed isolation chamber, making the set-up simpler than other calorimetric methods. A calibration procedure is necessary to establish the relation between the measured flux and the dissipated power, afterward the losses can be computed for arbitrary electrical signals from the calibration curve.

The characterizations of the first prototypes have provided satisfying results supported by simulations and comparison with measurements made with an oscilloscope. In future, the objective is to build a sensor mounted

between the device and the heat-sink, or integrated within the device case, to get a real-time estimation of the heat-flux and the system efficiency.

After the digression about the calorimetric apparatus, the thesis focuses on the realized multi-cell modified cascade multilevel inverter that has been presented with major details in chapter 5. This inverter, in conjunction with the SHE control technique, provides a way to lower the number of switches and ensure low power losses while maintaining high the quality of output waveform. A MATLAB routine has been developed for the calculation of the switching angles of the MOSFET based on the SHE technique, and the optimal switching angles for various number of levels are reported. It has been shown, with graphs about the THD and the spectrum of the output voltage, that, as the number of levels increase, the quality of the output waveform improves. A way to regulate the amplitude of the output voltage has also been discussed, and an algorithms that automatize the calculation of the SHE solutions for various modulation index has been provided, with graphs about the optimal switching angles and the relative THD as a function of the modulation index. Finally a duty cycle swapping technique that can be utilized prevent the uneven usage of the DC blocks has been discussed.

Extensive SPICE simulations on multilevel inverters have been done. A SPICE model of a complete photovoltaic system has been set up, including the photovoltaic modules, a modified cascaded multilevel inverter, and energy storage elements. In particular, the simulation of a single-phase 7-levels system composed of three DC blocks loaded by a resistance at the AC output terminals has been provided in chapter 6.

Once the device parameters are defined, the simulation inputs are the solar irradiance, the temperature, the storage capacitance, and the load. The model allows the characterization of the system dynamics; it can be used for example to evaluate the harmonic content of the output waveform and to study the behaviour at the same time of the overall system and its sub-components. Efficiency, power dissipation of each element, and power generated by the photovoltaic modules, for different values of the storage

elements and in presence e.g. of temperature or load variations can be evaluated.

It has been shown that storage elements of proper size placed in parallel to the PV modules are essential to get high conversion efficiency and low total harmonic distortion of the output waveform. The storage elements also help the modules operate close to their maximum power point in case of sudden load variations. The work has also shown the potentiality of the simulation of a complete photovoltaic system, that allows to obtain a deeper knowledge of the circuit performances. The use of PV cells as power generators of the inverter allows to obtain realistic simulation results compared those provided by DC voltage sources. An analysis of the power loss of the inverter has been carried out for two different couples of MOSFETs, and showed how the use of new generation devices could provide substantial increment in the efficiency of the system.

Finally a prototype of the inverter has been realized and the complete description of its elements has been provided in chapter 7. The prototype, based on the Multi-cell Modified Cascaded topology, is composed of three main elements: a DC-block (slave), a master and a H-bridge. Each DC-block is associated with a source; and contain a MOSFET, a diode, and a microcontroller that controls the MOSFET turn-on and monitors voltage and current at the DC-source. The master controls the system, generates the control signals for the H-bridge, synchronizes the slaves and determines the switching angles and the control strategy to use; the communication between the various blocks take place through the CAN serial bus on simple Ethernet cables. The advantages of this distributed architecture include the fact that the system is robust because if a DC-block (or its source) is damaged the system will automatically adapt and can continue to work with a reduced number of levels. Each DC-Block can work independently from the rest of the system, monitoring the voltage and current of the relative source. Moreover it is possible to add and remove sources and levels without disconnecting the load or the other sources.

Experimental measurements on the prototype with three and five DC-blocks connected have been carried out to verify the correct behaviour of the system with different voltage values of the sources and loads. The results shows the correctness of the control signals and the applied swapping technique. The harmonic spectrum for the various output has been reproduced to shows the correct application of the SHE technique and the cancelation of the lower order harmonics. Comments on the THD and efficiency are also provided.

8.2   Future works

Many aspects of inverter have been treated in this thesis. However, there are still many aspects that could be improved. For example the various elements of the prototype can be further optimized to achieve lower consumption and increase the efficiency.

Moreover, the SHE technique allows the regulation of the output voltage, but in this work it has been implemented in a static way with the only objective to minimize the harmonics. An algorithm to find the optimal switching angles for the desired value of the fundamental voltage has already been realized and described in paragraph 5.3.2. The next step is to implement the functionality e inside the prototype.

Finally, a MPPT function can be implemented to maximize the power extracted from the PV modules even with variation of the atmospheric conditions or the load. This can be achieved, even maintaining low the switching frequency, by modifying the application of the SHE to regulate the output, and with a proper distribution of the swapping strategy.

References

[1]   IEA PVPS, "Trends 2013 in photovoltaic applications," 2013. [Online]. Available: http://www.iea-pvps.org/index.php?id=1&eID=dam_frontend_push&docID=1733.

[2]   G. Kopp and J. L. Lean, "A new, lower value of total solar irradiance: Evidence and climate significance," *Geophysical Research Letters*, vol. 38, no. 1, Jan. 2011.

[3]   A. De Vos, "Detailed balance limit of the efficiency of tandem solar cells," *Journal of Physics D: Applied Physics*, 1980.

[4]   National Center for Photovoltaics (NCPV), "Research Cell Efficiency Records," 2013. [Online]. Available: http://www.nrel.gov/ncpv/images/efficiency_chart.jpg.

[5]   P. Basore, "Defining terms for crystalline silicon solar cells," *Progress in Photovoltaics: Research and …*, vol. 2, pp. 177–179, 1994.

[6]   Fraunhofer Institute for Solar Energy Systems, "Photovoltaics Report," 2013. [Online]. Available: http://www.ise.fraunhofer.de/en/downloads-englisch/pdf-files-englisch/photovoltaics-report-slides.pdf.

[7]   X. Deng and E. Schiff, "Amorphous silicon based solar cells," in *Handbook of Photovoltaic Science and Engineering*, 2003, pp. 506–565.

[8]   Fraunhofer Institute for Solar Energy Systems ISE, "World Record Solar Cell with 44.7% Efficiency," 2013. [Online]. Available: http://www.ise.fraunhofer.de/en/press-and-media/pdfs-zu-presseinfos-englisch/2013/press-release-world-record-solar-cell-with-44-7-efficiency.pdf.

[9]   M. C. Di Piazza and G. Vitale, *Photovoltaic Sources Modelling and Emulation*. Spinger, 2012.

[10]   C. Protogeropoulos and B. Brinkworth, "Evaluation of two theoretical models in simulating the performance of amorphous-silicon solar cells," in *Tenth E.C. Photovoltaic Solar Energy Conference*, 1991, pp. 412–415.

[11]   F. G. Sanchez, A. Ortiz-Conde, and J. Liou, "Calculating double-exponential diode model parameters from previously extracted single-exponential model parameters," *Electronics Letters*, 1995.

[12]   A. Cheknane, H. Hilal, and F. Djeffal, "An equivalent circuit approach to organic solar cell modelling," *Microelectronics Journal*, vol. 39, no. 10, pp. 1173–1180, 2008.

[13]   J. Gow and C. Manning, "Development of a photovoltaic array model for use in power-electronics simulation studies," *IEE Proceedings Electric Power Applications*, vol. 146, no. 2, pp. 193–200, 1999.

[14]   R. Baker and L. Bannister, "Electric power converter," *US Patent 3,867,643*, 1975.

[15]   J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.

[16]   J. Lai and F. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, 1996.

[17]   L. Tolbert, F. Peng, and T. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, pp. 36–44, 1999.

[18]   A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981.

[19] M. Marchesoni and M. Mazzucchelli, "Multilevel converters for high power AC drives: A review," *Industrial Electronics, 1993. …*, 1993.

[20] P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *IEEE Transactions on Industry Applications*, vol. IA-19, no. 6, pp. 1057–1069, Nov. 1983.

[21] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems-an overview," in *IEEE Int. Symp. Industrial Electronics*, 1998, pp. 224–229.

[22] G. Su, "Multilevel DC-link inverter," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 848–854, 2005.

[23] M. Manjrekar and T. Lipo, "A hybrid multilevel inverter topology for drive applications," in *Applied Power Electronics Conference and Exposition. APEC '98.*, 1998, vol. 00, no. c, pp. 523 – 529.

[24] M. Malinowski, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197 – 2206, 2010.

[25] M. Calais, V. G. Agelidis, and M. Meinhardt, "Multilevel converters for single-phase grid connected photovoltaic systems: an overview," *Solar Energy*, vol. 66, no. 5, pp. 325–335, Aug. 1999.

[26] L. Tolbert and F. Peng, "Multilevel converters as a utility interface for renewable energy systems," *Power Engineering Society Summer Meeting*, vol. 2, pp. 1271–1274, 2000.

[27] R. Carbone and A. Tomaselli, "A High-Efficiency AC PV-Module for High-Quality Connection to Modern Low-Voltage Distribution Grids," *International Review of Electrical Engineering*, vol. 6, no. 6, p. 2796, 2011.

[28] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *Eur. Power Electron. J.*, vol. 2, pp. 45 –50, 1992.

[29] E. Babaei, "Optimal Topologies for Cascaded Sub-Multilevel Converters," *Journal of Power Electronics*, vol. 10, no. 3, pp. 251–261, May 2010.

[30] P. Lezana and R. Aceiton, "Hybrid multicell converter: topology and modulation," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 3938–3945, 2011.

[31] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Energy Conversion and Management*, vol. 50, no. 11, pp. 2761–2767, Nov. 2009.

[32] M. Murugesan and S. Sivaranjani, "Seven Level Modified Cascaded Inverter for Induction Motor Drive Applications," *Journal of Information Engineering and Applications*, vol. 1, no. 1, pp. 36–45, 2011.

[33] L. Tolbert, F. Peng, and T. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, pp. 36–44, 1999.

[34] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737 – 1746, 2009.

[35] S. Fazel and S. Bernet, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," *IEEE Transactions on Industry Applications*, vol. 43, no. 4, pp. 1032–1040, 2007.

[36] R. Carbone and A. Tomaselli, "Numerical Analysis of Quality of Power Generated by an Innovative AC PV-module with On-board Energy Storage," in *12th WSEAS International Conference on Electric Power Systems, High Voltages, Electric Machines*, 2012, pp. 72–77.

[37] S. Busquets-Monge, "Multilevel diode-clamped converter for photovoltaic generators with independent voltage control of each solar array," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2713–2723, 2008.

[38] P. Flores, J. Dixon, and M. Ortúzar, "Static var compensator and active power filter with power injection capability, using 27-level inverters and photovoltaic cells," *Industrial Electronics …*, vol. 56, no. 1, pp. 130–138, 2009.

[39] H. Patel and R. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I--Harmonic Elimination," *IEEE Transactions on Industry Applications*, vol. I, no. 3, pp. 310 – 317, 1973.

[40] R. Perret, *Power electronics semiconductor devices*. Wiley, 2009.

[41] E. Pop, S. Sinha, and K. E. Goodson, "Heat Generation and Transport in Nanometer-Scale Transistors," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1587–1601, Aug. 2006.

[42] G. Wachutka, "Rigorous thermodynamic treatment of heat generation and conduction in semiconductor device modeling," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 9, no. 11, pp. 83–95, 1990.

[43] Y. Leung and A. Paul, "Heating Mechanisms of LDMOS and LIGBT in Ultrathin SOI," *IEEE Electron Device Letters*, vol. 18, no. 9, pp. 414–416, 1997.

[44] A. Raman, D. . Walker, and T. . Fisher, "Simulation of nonequilibrium thermal effects in power LDMOS transistors," *Solid-State Electronics*, vol. 47, no. 8, pp. 1265–1273, Aug. 2003.

[45] J. Roig, E. Stefanov, and F. Morancho, "Thermal behavior of a superjunction MOSFET in a high-current conduction," *IEEE Transactions on Electron Devices*, vol. 53, 2006.

[46] Yole Developpement, "Status of the power electronics industry." 2012.

[47] Infineon Technologies, "CoolMOS™ C7 : Mastering the Art of Quickness," 2013.

[48] G. Deboy, N. Marz, and J. Stengl, "A new generation of high voltage MOSFETs breaks the limit line of silicon," in *Electron Devices Meeting*, 1998.

[49] L. Lorenz, G. Deboy, A. Knapp, and N. Marz, "COOLMOS™- a new milestone in high voltage power MOS," in *Power Semiconductor Devices and ICs*, 1999, pp. 3–10.

[50] Yole Developpement, "Overview of Wide Band Gap semiconductors in power electronics," 2013.

[51] M. A. Briere, "GaN Based Power Devices: Cost-Effective Revolutionary Performance," *Power Electronics Europe*, no. 7, pp. 29–31, 2008.

[52] C. Xiao, G. Chen, and W. G. Odendaal, "Overview of power loss measurement techniques in power electronics systems," in *IEEE Industry Applications Conference, 2002. 37th IAS Annual Meeting*, 2002, vol. 2, pp. 1352–1359.

[53] D. Christen, U. Badstuebner, J. Biela, and J. W. Kolar, "Calorimetric power loss measurement for highly efficient converters," in *The 2010 International Power Electronics Conference*, 2010, pp. 1438–1445.

[54] W. Cao, K. Bradley, and I. French, "A review of calorimetric application for accurate power loss measurement," *Universities Power …*, no. l, pp. 550–554, 2006.

[55] S. Sridhar, R. M. Wolf, and W. G. Odendaal, "An accurate experimental apparatus for measuring losses in magnetic components," in *IEEE Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting*, 1999, vol. 3, pp. 2129–2133.

[56] G. Chen, C. Xiao, and W. G. Odendaal, "An apparatus for loss measurement of integrated power electronics modules: design and analysis," in *IEEE Industry Applications Conference, 2002. 37th IAS Annual Meeting*, 2002, vol. 1, pp. 222–226.

[57] T. E. Diller, "Heat Flux," in *The Measurement, Instrumentation, and Sensors Handbook*, CRC Press, 1999.

[58] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, vol. 52, no. 2, pp. 1114–1128, Feb. 2011.

[59] Cadence Design Systems, "Cadence Pspice A/D & PSpice Advanced Analysis." [Online]. Available: http://www.cadence.com/rl/Resources/technical_briefs/PSpice_tb.pdf.

[60] Internation Rectifier, "IRF3415 Datasheet," 2005. [Online]. Available: http://www.irf.com/product-info/datasheets/data/irf3415.pdf.

[61] Internation Rectifier, "12CGQ150 Datasheet," 2012. [Online]. Available: http://www.irf.com/product-info/datasheets/data/12cgq150.pdf.

[62] Vishay Siliconix, "IRFP360 Datasheet," 2011. [Online]. Available: http://www.vishay.com/docs/90292/sihfp360.pdf.

[63] Internation Rectifier, "IRFPS3815 Datasheet," 2001. [Online]. Available: http://www.irf.com/product-info/datasheets/data/irfps3815.pdf.

[64] Infineon, "IPW65R045C7 CoolMOS Datasheet," 2013. [Online]. Available: http://www.infineon.com/dgdl/DS_IPW65R045C7_2_1.pdf?folderId=db3a30431ff9 8815012019af55de3f2c&fileId=db3a30433e78ea82013e7901c1200031.

[65] P. Panagis, F. Stergiopoulos, P. Marabeas, and S. Manias, "Comparison of state of the art multilevel inverters," *Power Electronics Specialists Conference, 2008. PESC 2008*, pp. 4296–4301, 2008.

[66] D. Marquardt, "An algorithm for least-squares estimation of nonlinear parameters," *Journal of the Society for Industrial & Applied Mathematics*, vol. 11, no. 2, pp. 431–441, 1963.

[67] L. Castaner and S. Silvestre, *Modelling photovoltaic systems using PSpice*. John Wiley and Sons, 2002.

[68] MOTECH, "IM156-158 Datasheet," 2011. [Online]. Available: http://www.motech.com.cn/doc/cell/IM156_GM1.1.pdf.

[69] E. Beser, B. Arifoglu, S. Camur, and E. K. Beser, "A grid-connected photovoltaic power conversion system with single-phase multilevel inverter," *Solar Energy*, vol. 84, no. 12, pp. 2056–2067, Dec. 2010.

[70] Microchip Technology Inc., "PIC18F66K80 family Datasheet," 2012. [Online]. Available: http://ww1.microchip.com/downloads/en/DeviceDoc/39977f.pdf.

[71] BOSCH, "CAN Specification," 1991. [Online]. Available: http://www.bosch-semiconductors.de/media/pdf_1/canliteratur/can2spec.pdf.

[72] Analog Devices Inc., "ADM3054 Datasheet," 2013. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADM3054.pdf.

[73] Analog Devices Inc., "iCoupler Digital Isolation Products," 2005. [Online]. Available: http://www.analog.com/static/imported-files/overviews/iCoupler_Brochure.pdf.

[74] Exar, "SPX3819 Datasheet," 2012. [Online]. Available: http://www.exar.com/common/content/document.ashx?id=615&languageid=1033.

[75] Analog Devices Inc., "ADuM1280 Datasheet," 2013. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADuM1280_1281_1285_1286.pdf.

[76] Texas Instruments Inc., "INA283 Datasheet," 2012. [Online]. Available: http://www.ti.com/lit/ds/symlink/ina283.pdf.

[77] Infineon Technologies, "IPB038N12N3 Datasheet," 2009. [Online]. Available: http://www.infineon.com/dgdl/IPP_I_B041N12N3_Rev2.2.pdf?folderId=db3a3043 13b8b5a60113cee8763b02d7&fileId=db3a30432239cccd0122a75b86467ca4.

[78] Texas Instruments Inc., "UCC27537 Datasheet," 2013. [Online]. Available: http://www.ti.com/lit/ds/symlink/ucc27537.pdf.

[79] O. Semiconductor, "MBRS3100T3G Datasheet," 2012. [Online]. Available: http://www.onsemi.com/pub_link/Collateral/MBRS3100T3-D.PDF.

[80] Internation Rectifier, "IR2106(4)(S) Datasheet," 2004. [Online]. Available: http://www.irf.com/product-info/datasheets/data/ir2106.pdf.

[81] ST Microelectronics, "STW88N65M5 Datasheet," 2013. [Online]. Available: http://www.st.com/web/en/resource/technical/document/datasheet/DM00042858.pdf.