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Study and Assessment of Defect and Trap Effects on the Current Capabilities of a 4H-SiC-Based Power MOSFET

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Abstract: A numerical simulation study accounting for trap and defect effects on the current-voltage characteristics of a 4H-SiC-based power metal-oxide-semiconductor field effect transistor (MOSFET) is performed in a wide range of temperatures and bias conditions. In particular, the most penalizing native defects in the starting substrate (i.e., $EH_{6/7}$ and $Z_{1/2}$) as well as the fixed oxide trap concentration and the density of states (DoS) at the $4H\text{-}SiC/SiO_2$ interface are carefully taken into account. The temperature-dependent physics of the interface traps are considered in detail. Scattering phenomena related to the joint contribution of defects and traps shift the MOSFET threshold voltage, reduce the channel mobility, and penalize the device current capabilities. However, while the MOSFET on-state resistance (R_{ON}) tends to increase with scattering centers, the sensitivity of the drain current to the temperature decreases especially when the device is operating at a high gate voltage (V_{GS}). Assuming the temperature ranges from 300 K to 573 K, R_{ON} is about 2.5 $M\Omega\cdot\mu m^2$ for $V_{GS} > 16$ V with a percentage variation ΔR_{ON} lower than 20%. The device is rated to perform a blocking voltage of 650 V.

Keywords: 4H-SiC; power devices; ON-state resistance; defects states; interface traps

1. Introduction

Silicon carbide (SiC) is worldwide recognized as a semiconductor well suited for high-temperature and high-power applications. In particular, the 4H-SiC polytype presents a high thermal conductivity on the order of 3–4 W/Kcm, a high specific resistivity of about 10^{11} $\Omega\cdot$cm, and a wide bandgap close to 3.23 eV at room temperature. Moreover, 4H-SiC-based devices are characterized by high critical electric fields and low leakage currents [1].

In modern power electronics, metal-oxide-semiconductor field effect transistors (MOSFETs) are widely valued for their low ON-state resistance (R_{ON}), high efficiency, and noticeable switching capabilities. Typical 4H-SiC-based MOSFETs are designed to support high blocking voltages ranging from 600 V to 1.7 kV [2–4]. However, the fundamental electrical parameters of a MOSFET, namely the breakdown voltage, output current, and specific R_{ON}, could be heavily affected by explicit trap/defect concentrations located in the bulk as well as in correspondence of the inversion layer at the silicon oxide (SiO_2) interface [5–8].

From the literature, several papers have dealt with the 4H-SiC technological issues related, for example, to stacking faults, screw dislocations, and micro-pipes [9–12]. In more detail, in the MOSFET structure, a high density of states (DoS) at the $4H\text{-}SiC/SiO_2$ interface tends to prevent the realization of an efficient conductive channel, hence, reducing the carrier mobility. At the same time, the material intrinsic defects, in dependence of their capture cross sections, act as the primary carrier-lifetime killer in the drift region. Therefore,

the presence of carbon atoms leads SiC-based devices to face higher concentrations of defects and traps in comparison with the conventional silicon technology. Obviously, these concentrations strongly depend on the effective quality of the starting materials and gate oxide interfaces.

The aim of this work is to assess the impact of trap and defect effects on the current-voltage characteristics of a power MOSFET in 4H-SiC. In particular, by means of a detailed numerical simulation study carried out at different temperatures ($300 \leq T \leq 573$ K) and bias conditions, the joint contribution of defects and traps is investigated accounting for their fundamental physical parameters such as the charge density, the location inside the bandgap, and the occupation probability. The physics of the interface trap distribution is modelled as temperature-dependent. This dependence results in a DoS spreading near the conduction and valence band edges for increasing values of T.

The device is dimensioned for a breakdown voltage (BV_{DS}) of 650 V that meets the specifications of a huge market of power devices useful for several applications with special technical specifications (e.g., small size, thermal stability, low static power dissipation, ruggedness, 365-days-per-year operation under all weathers, etc.) which could be really satisfied by SiC technology. The MOSFET R_{ON} and its percentage variation with temperature (ΔR_{ON}) are considered key performance indicators during the simulations. In particular, R_{ON} is around 2.5 M$\Omega \cdot \mu m^2$ with ΔR_{ON} in the limit of 20% for T ranging from 300 K to 573 K when imposing a gate voltage (V_{GS}) higher than 16 V.

The presented study further extends the modelling efforts reported in recent authors' manuscripts [13–17] where, by assuming the MOSFET structure trap/defect-free, we have explored the opportunity of down-shifting the SiC lower bound for a voltage rating around 150 V. There, in fact, while it has appeared rather evident that the use of SiC tends to lose in part its advantages for such extremely lower BV_{DS} devices with respect to the use of silicon technology, preliminary results on the individual role of traps and defects have suggested the need to explore their combined effect in determining the effective MOSFET threshold voltage (V_{TH}) and the R_{ON} behavior through the channel resistance and drift region contribution.

2. Device Structure

By using a 2D TCAD physical simulator [18], the MOSFET cross-section (half-cell) has been designed as shown in Figure 1. Although simplified for simulation purposes, this structure is in principle compatible with an actual 4H-SiC technological process based on doping by ion implantation [19–21].
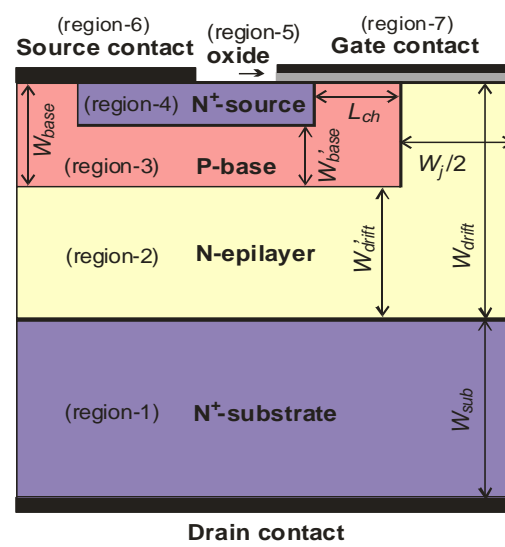

Figure 1. Schematic cross-sectional view of the metal-oxide-semiconductor field effect transistor (MOSFET) half-cell. The drawing is not to scale.

Seven regions can be identified as follows. The drain is a heavily nitrogen-doped N⁺-region (region 1) that coincides with the 4H-SiC substrate on which the drift layer (region 2) is grown by epitaxy. Region 3 is the aluminum-doped p-base where the MOS structure and the conductive channel under the gate oxide lie. Region 4 is the phosphorous-doped source region. Region 5 is the insulating SiO_2. Finally, region 6 and region 7 form the source and the gate contacts, respectively. Note that the source contact shorts the source and base regions to prevent the switch-on of the parasitic substrate(N⁺)-epilayer(N)-base(P)–source(N⁺) bipolar junction transistor.

Referring to Figure 1, the geometrical parameters and doping concentrations of the different MOSFET regions are summarized in Table 1. The half-cell width is 7.5 μm and the simulated device footprint is 7.5 μm².

Table 1. MOSFET structure.

Parameter	Value
Oxide thickness, t_{ox} (μm)	0.08
Channel length, L_{ch} (μm)	1
Base junction depth, W_{base} (μm)	1.5
Interspace, W'_{base} (μm)	1
Base-to-base distance, W_j (μm)	5
Epilayer thickness, W_{drift} (μm)	5
Base-to-substrate distance, W'_{drift} (μm)	3.5
Substrate thickness, W_{sub} (μm)	100
N⁺-source doping (cm⁻³)	1×10^{18}
P-base doping (cm⁻³)	1×10^{17}
N-epilayer doping (cm⁻³)	5×10^{15}
N⁺-substrate doping (cm⁻³)	1×10^{19}

The distance between the p-base regions, W_j, is set to 5 μm (accumulation region) while the W_{drift} thickness (5 μm) assures a MOSFET breakdown voltage close to 650 V as verified in [13]. This result is consistent with the calculations that we can perform by adapting to the P-base/N-epilayer/N⁺-substrate structure the standard expression valid for an abrupt junction p-i-n diode in punch-through condition [22], i.e.,

$$BV_{DS} = E_C W'_{drift} - \frac{q N_{epi} (W'_{drift})^2}{2\varepsilon_s} \tag{1}$$

where E_C = 2 MV/cm is the 4H-SiC critical electric field (typical value), q is the electron charge, and ε_s is the semiconductor dielectric constant. From the theory, the lower the desired BV_{DS} the higher the drift layer doping (N_{epi}), considering that, for a 4H-SiC-based MOSFET, N_{epi} is generally in the range 5×10^{15}–10^{16} cm⁻³ [20,21,23].

For the proposed device, the overall ON-state resistance is determined by the sum of six different terms:

$$R_{ON} = R_{N+} + R_{ch} + R_{acc} + R_{JFET} + R_{epi} + R_{sub} \tag{2}$$

where R_{ch} is the channel resistance, R_{N^+} is the source resistance, R_{acc} is the accumulation layer resistance, R_{JFET} is the resistance of the depletion layer between the P-base region and the N-epilayer, R_{epi} is the epilayer region resistance, and R_{sub} is the substrate resistance. The contributions R_{N^+} and R_{sub} are generally negligible because they are related to heavily doped regions. At the same time, R_{ch} and R_{acc} mainly depend on the gate bias level whereas R_{JFET} and R_{epi} are determined by the epilayer geometry and doping concentration.

3. Physical Models

The key physical models considered in this work include the standard expressions summarized in Table 2 [24–32].

Table 2. Physical models for numerical simulation.

Model	Expression
Bandgap energy	$E_g(T) = E_{g300} - \theta(T - 300)$
Auger recombination	$R_{Auger} = \left(C_{Ap}p + C_{An}n\right)\left(np - n_i^2\right)$
Shockley Read Hall recombination	$R_{SRH} = \dfrac{pn - n_i^2}{\tau_p\left(n + n_i \exp\left(\frac{E_{trap}}{kT}\right)\right) + \tau_n\left(p + n_i \exp\left(-\frac{E_{trap}}{kT}\right)\right)}$
Incomplete ionization of impurities	$N_{A',D}^{-\,+} = N_{A,D}\left(\dfrac{-1 + \sqrt{1 + 4g_{v,c}\frac{N_{A,D}}{N_{V,C}(T)}e^{\frac{\Delta E_{A,D}}{kT}}}}{2g_{v,c}\frac{N_{A,D}}{N_{V,C}(T)}e^{\frac{\Delta E_{A,D}}{kT}}}\right)$
Apparent bandgap narrowing	$\Delta E_{gp,n} = A_{p,n}\left(\frac{N_{A',D}^{-\,+}}{10^{18}}\right)^{\frac{1}{2}} + B_{p,n}\left(\frac{N_{A',D}^{-\,+}}{10^{18}}\right)^{\frac{1}{3}} + C_{p,n}\left(\frac{N_{A',D}^{-\,+}}{10^{18}}\right)^{\frac{1}{4}}$
Impact ionization	$\Gamma_{n,p} = a_{0n,p}\exp\left(-\frac{b_{0n,p}}{E}\right)$
Carrier lifetime	$\tau_{n,p} = \dfrac{\tau_{0n,p}\left(\frac{T}{300}\right)^{\lambda}}{1 + \left(\frac{N}{N_{n,p}^{SRH}}\right)}$
Carrier mobility for low-field and high-field conditions	$\mu_{n,p} = \mu_{0n,p}^{\min}\left(\frac{T}{300}\right)^{\alpha} + \dfrac{\mu_{0n,p}^{\max}\left(\frac{T}{300}\right)^{\beta} - \mu_{0n,p}^{\min}\left(\frac{T}{300}\right)^{\alpha}}{1 + \left(\frac{T}{300}\right)^{\gamma}\left(\frac{N}{N_{n,p}^{crit}}\right)^{\delta}}$ $\mu_{n,p}(E) = \dfrac{\mu_{n,p}}{\left[1 + \left(E\frac{\mu_{n,p}}{v_{sat}(T)}\right)^{\kappa}\right]^{\frac{1}{\kappa}}}$
Saturation velocity	$v_{sat}(T) = v_{sat300} + \left(\frac{300}{T}\right)^{\eta}$

The numerical simulation study solves the Poisson's equation and the carrier continuity equations for a finely meshed device structure [18]. In particular, a mesh spacing down to 0.5 nm is imposed around the MOSFET p-n junctions and within the channel region. For the models in Table 2, all the reference parameters are reported in recent papers of ours focused on different 4H-SiC-based devices and supported by experimental results [14,33–38].

The carrier mobility degradation in the inversion layer, which is due to different scattering phenomena (e.g., Coulomb scattering and surface scattering effects), is modelled considering the transverse electric field component for carriers ($E_\perp$) by means of the expression [18]

$$\mu_{n,p}(E_\perp) = \mu_{n,p}\left(1 + \frac{E_\perp}{E_{n,p}^{crit}}\right)^{-\frac{1}{2}} \tag{3}$$

where $E_{n,p}^{crit}$ is an adjustable parameter.

In addition to the simulation setup recalled above, in the presented analysis the defect/trap effects are carefully taken into account as described in the following. In fact, the quality of the 4H-SiC/SiO$_2$ interface as well as the presence of deep defect states in the 4H-SiC substrate and epilayer are crucial factors in determining the MOSFET electrical characteristics.

3.1. H-SiC/SiO$_2$ Interface Traps

In a poor-quality 4H-SiC/SiO$_2$ interface, a large number of interface-trapped charges related to traps having energy levels inside the semiconductor bandgap strongly affect the current capabilities of a physical device. The total amount of this trapped charges basically depends on the location of the intrinsic Fermi level, and an exchange of carriers with the valence and conduction bands takes place in turn through the trap capture and emission rates. In this study, the DoS induced by traps at the 4H-SiC/SiO$_2$ interface is modelled as a sum of different contributions, namely a deep level distribution of states in the midgap (D$_{Mid}$), which presents a constant density with energy, and two exponentially decaying

band tail states close to the conduction and valence band-edges (D_{TC}, D_{TV}) acting either as acceptor- or donor-like levels for free carriers [18]. As well known, acceptor-like centers are neutral when empty and become negatively charged when filled while donor-like centers are positively charged when empty and become neutral after capturing electrons (emitting holes). The model expressions for the tail state densities are in the form of

$$D_{TC}(E,T) = D_{TC}^0 \exp\left(\frac{E - E_C}{U_C(T)}\right) \tag{4}$$

$$D_{TV}(E,T) = D_{TV}^0 \exp\left(\frac{E_V - E}{U_V(T)}\right) \tag{5}$$

where U_C and U_V are the temperature-dependent characteristic energy decays of these profiles, and D_{TC}^0 and D_{TV}^0 are the tail state densities at the conduction band edge and valence band edge, respectively. This model is in accordance with different experimental results reported in the literature for different materials and dopants [39–44].

The DoS effects in the device channel region are accounted for by solving the following Poisson's equation for the electrostatic potential (ψ)

$$\nabla \cdot (\varepsilon \nabla \Psi) = q\left(n - p - N_D^+ + N_A^-\right) - Q_T \tag{6}$$

Here, in addition to the ionized impurity concentrations N_D^+ and N_A^-, which are expressed by the following standard expressions:

$$N_D^+ = \frac{N_D}{1 + 2\exp\left(\frac{E_{Fn} - E_D}{kT}\right)} \tag{7}$$

$$N_A^- = \frac{N_A}{1 + 4\exp\left(\frac{E_A - E_{Fp}}{kT}\right)} \tag{8}$$

where N_D and N_A are the substitutional n-type and p-type doping concentrations, E_D and E_A are the donor and acceptor energy levels, and E_{Fn} and E_{Fp} are the quasi-Fermi energy levels for electrons and holes, respectively, the trapped charge contribution Q_T is calculated as

$$Q_T = q(N_{tD}^+ - N_{tA}^-) \tag{9}$$

considering that the ionized densities of traps N_{tD}^+ (donor-like) and N_{tA}^- (acceptor-like) are terms which depend on the product between the trap density and its probability of occupation, i.e.,

$$F_t = \frac{v_{n,p}\sigma_{n,p} + e_{p,n}}{v_{n,p}(\sigma_p + \sigma_n) + (e_n + e_p)} \tag{10}$$

where $v_{n,p}$ is the carrier thermal velocity, $\sigma_{n,p}$ is the carrier capture cross section, and $e_{n,p}$ is the trap emission rate for electrons and holes given by

$$e_n = v_n\sigma_n n_i \exp\left(\frac{E - E_i}{kT}\right) \tag{11}$$

$$e_p = v_p\sigma_p n_i \exp\left(\frac{E_i - E}{kT}\right) \tag{12}$$

In Equations (11) and (12), n_i is the material intrinsic carrier concentration and E_i is the intrinsic Fermi level.

The DoS parameters used in the simulations at T = 300 K are summarized in Table 3 [44–46]. According to experimental data from the literature, we can put in evidence that the band-edge trap densities of states are over two orders of magnitude higher than the energy-constant midgap contribution [42,43].

Table 3. DoS reference parameters at T = 300 K.

Parameter	Value
Tail state density, $D^0{}_{TC,V}$ (cm^{-2} eV^{-1})	5.7×10^{13}
Band-tail energy decay, $U_{C,V}$ (meV)	67
Mid-gap density, D_{Mid} (cm^{-2} eV^{-1})	2.4×10^{11}
Thermal velocity, $v_{n,p}$ (cm/s)	1.9×10^7, 1.2×10^7
Capture cross section, $\sigma_{nA,D}$ (cm^2)	1×10^{-16}, 1×10^{-14}
Capture cross section, $\sigma_{pA,D}$ (cm^2)	1×10^{-14}, 1×10^{-16}

Finally, in the simulation setup we have considered a thin film of fixed oxide traps next to the 4H-SiC interface. Although the fixed oxide traps cannot exchange charge with carriers, due to their location they can act as Coulombic scattering centers that reduce the MOSFET threshold voltage and degrade the carrier mobility in the inversion layer. The effective concentration of the fixed oxide traps (N_{fix}) strictly depends on the device oxidation process and we have assumed typical values from the literature in the range 2×10^{11}–1.3×10^{12} cm^{-2} [41–43].

3.2. H-SiC Intrinsic Defects

In the design of the MOSFET structure in Figure 1, the presence of 4H-SiC intrinsic defects cannot be neglected. In fact, the minority carrier current generated in the channel region flows vertically through the epilayer and the N$^+$-substrate.

The most penalizing native defects in 4H-SiC-based devices are the so-called EH$_{6/7}$ and Z$_{1/2}$ centers [47]. These defects are both originated by a carbon vacancy due to, for example, electron radiations or high-temperature treatments. They are deep levels not independent each other and their concentration ratio is often considered unitary [48–51]. In more detail, Z$_{1/2}$ centers are located in the upper half of the 4H-SiC bandgap whereas the EH$_{6/7}$ level is close to the midgap (~1.65 eV). Although the EH$_{6/7}$ nature as recombination centers can be uncertain, in the n-type 4H-SiC Z$_{1/2}$ and EH$_{6/7}$ are usually recognized as the acceptor-level and the donor-level of a carbon vacancy, respectively [45,47–49].

Table 4 summarizes the capture cross sections and the energy levels from the conduction band used during the simulations for the EH$_{6/7}$ and Z$_{1/2}$ centers. These parameters are consistent with several sets of data reported in the literature [48,51–54]. In particular, a wide range of defect concentrations is investigated starting from $N_t = 2 \times 10^{14}$ cm^{-3} up to $N_t = 3 \times 10^{15}$ cm^{-3}.

Table 4. Intrinsic defect parameters.

	E_t (eV)	N_t (cm^{-3})	σ_n (cm^2)	σ_p (cm^2)
Z$_{1/2}$	0.67	2×10^{14}–3×10^{15}	2.0×10^{-14}	3.5×10^{-14}
EH$_{6/7}$	1.65	2×10^{14}–3×10^{15}	2.4×10^{-14}	1.0×10^{-14}

It is worthwhile noting that to account for carrier lifetime killing effects caused by the 4H-SiC intrinsic defects, we have considered the carrier lifetimes governed both by the doping-dependent model reported in Table 2 and by the following expression [18]

$$\tau_{n,p} = \frac{1}{v_{n,p}\sigma_{n,p}N_t} \tag{13}$$

where the minority carrier lifetime is inversely correlated with N_t. This behavior has been verified experimentally for 4H-SiC epitaxial layers of growing thickness with defect concentrations exceeding 1×10^{13} cm^{-3} by deep level transient spectroscopy (DLTS) and minority carrier transient spectroscopy (MCTS) measurements [54,55].

4. Results and Discussion

The simulation analysis starts considering the 4H-SiC MOSFET described in Table 1 as a device free of intrinsic defects and interface traps (fresh device). The drain current (I_{DS})-drain voltage (V_{DS}) output characteristics nearby and within the triode region of this device for $8 \leq V_{GS} \leq 20$ V are shown in Figure 2 (T = 300 K) and Figure 3 (T = 573 K). The value V_{GS} = 8 V can be roughly assumed close to the effective MOSFET threshold voltage.
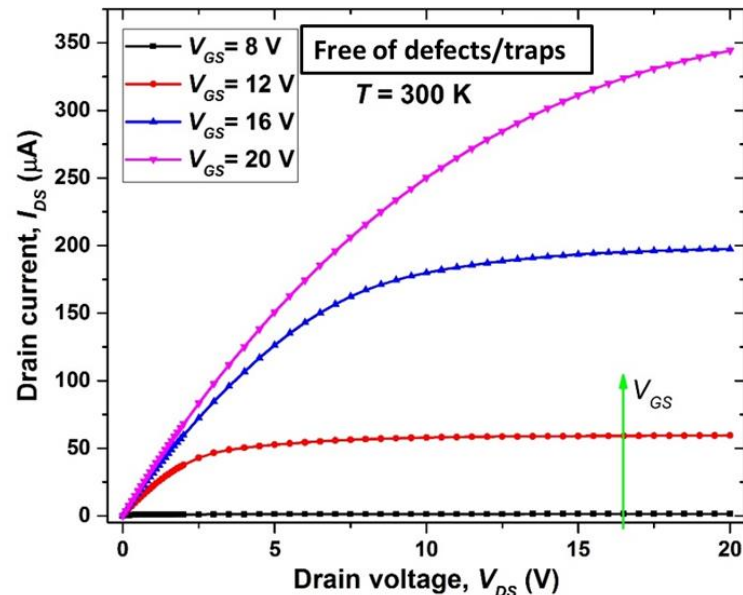

Figure 2. Forward I_{DS}-V_{DS} characteristics of the device in Table 1 at T = 300 K.
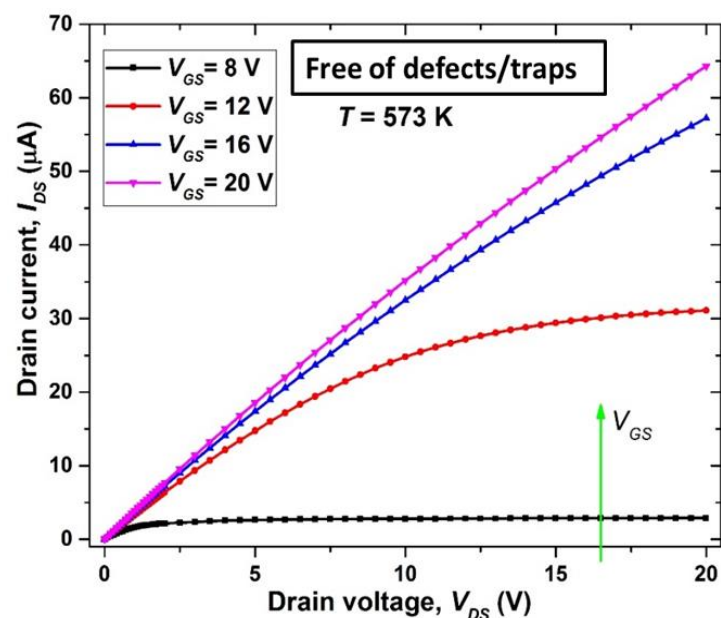

Figure 3. Forward I_{DS}-V_{DS} characteristics of the device in Table 1 at T = 573 K.

We can note that the drain current decreases harshly when increasing the temperature. This effect is mainly related to the temperature dependence of the carrier mobility in the inversion layer and drift region, determining an overall increase of the device ON-state resistance.

The calculated behaviors of R_{ON} as a function of V_{GS} are shown in Figure 4. Here, the percentage variation with temperature (ΔR_{ON}) is also reported. In particular, ΔR_{ON} quickly

tends to stabilize around 300%. As expected, an increasing value of T determines a change in the charge density both in the inversion and in the depletion region with a severe impact on the R_{ON} curve.
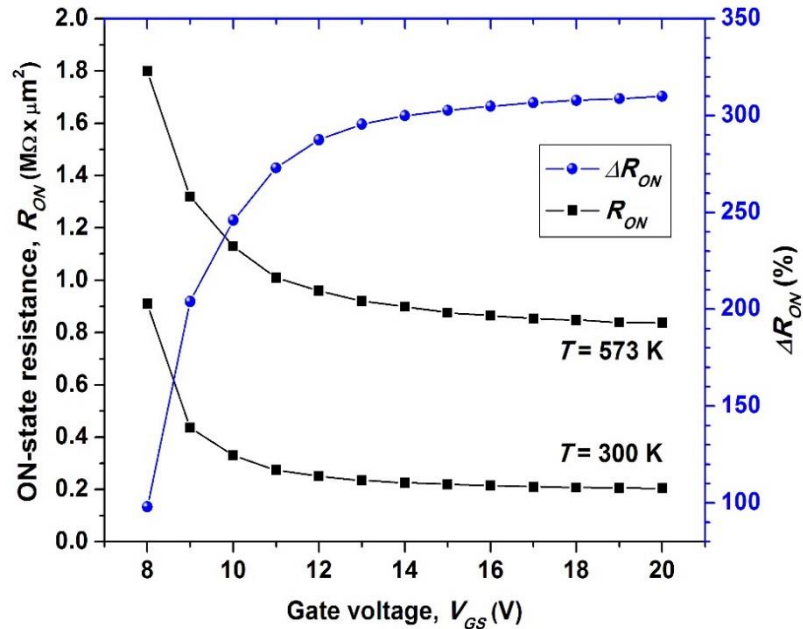

Figure 4. ON-state resistance versus V_{GS} for a fresh device. V_{DS} = 1 V.

It is important to note that the prediction capabilities of the adopted simulation setup have been tested in [13] by comparing the R_{ON} results for an almost similar device (BV_{DS} = 900 V) with the datasheet values of a commercial MOSFET in 4H-SiC [56]. In particular, a good agreement has been achieved calculating R_{ON} close to 520 k$\Omega \times \mu$m^2 for V_{GS} = 15 V and V_{DS} = 1 V at room temperature.

Introducing different $Z_{1/2}$ and $EH_{6/7}$ intrinsic defect concentrations for 4H-SiC in the proposed MOSFET structure, we have calculated the I_{DS}-V_{GS} characteristics showed in Figure 5.
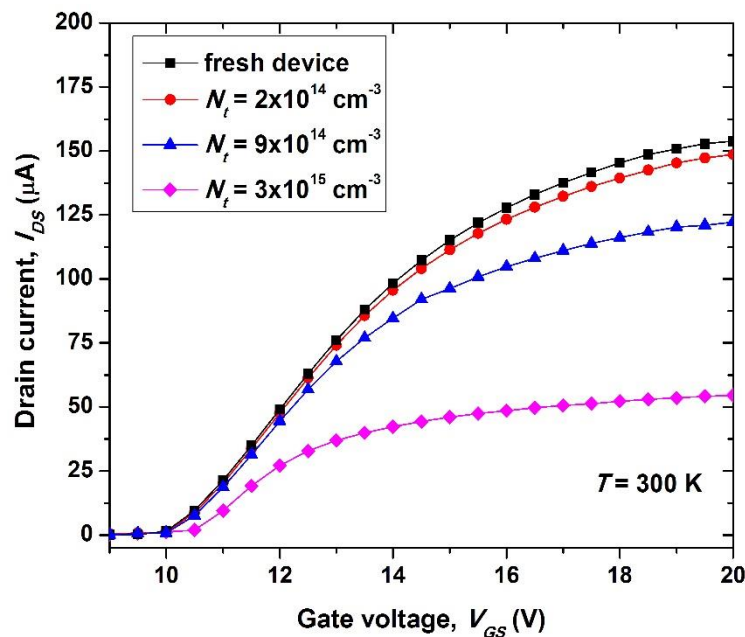

Figure 5. I_{DS}-V_{GS} curves for different 4H-SiC intrinsic defect concentrations. V_{DS} = 5 V.

As stated previously, the output current mainly flows vertically through the epilayer and substrate and therefore it is evident that as N_t increases I_{DS} decreases unavoidably. In particular, as verified during the simulations, $N_t = 2 \times 10^{14}$ cm^{-3} can be considered the limit value to preserve the drain current behavior in the whole explored V_{GS} range. In fact, the more N_t tends to become comparable to the epilayer doping concentration (5×10^{15} cm^{-3}) the more the device current capabilities are strongly penalized.

The main reason of the results in Figure 5 lies in the penalized flow of electrons due to the defect effects which originate in the MOSFET drift region increasing the local recombination rate. In other words, the drain current is degraded because these defects reduce the carrier lifetime and act as carrier traps in the device active region introducing high-resistive paths. The weight of the term N_t in penalizing the device current-voltage characteristics is almost the same for different temperatures when the MOSFET is firmly in ON-state. For example, in the 300–573 K temperature range, with respect to the fresh device, we can calculate always an I_{DS} reduction on the order of 5% and 20% for $N_t = 2 \times 10^{14}$ cm^{-3} and $N_t = 9 \times 10^{14}$ cm^{-3}, respectively.

On the contrary, the presence of 4H-SiC intrinsic defects affects the MOSFET threshold voltage variation with temperature differently. In fact, as shown in Figure 6, while V_{TH} tends to increase with increasing N_t for a fixed temperature, this effect tends to become less prominent at the higher values of T (>400 K). In Figure 6, V_{TH} is always calculated by imposing a subthreshold drain current in the limit of 10 nA.
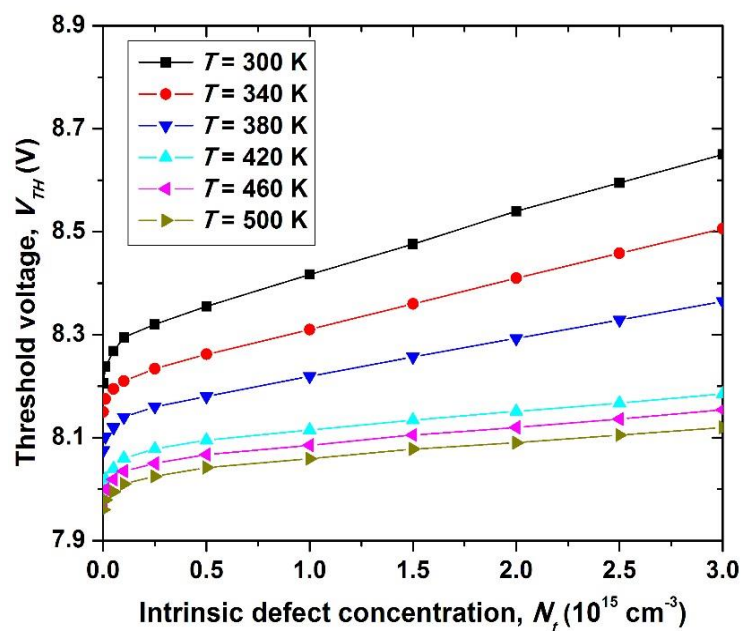

Figure 6. Threshold voltage behavior as a function of N_t at different temperatures.

The increase of the intrinsic defect concentration in the starting epilayer contributes to prevent the creation of the MOSFET conductive channel. In fact, defect effects enhance the recombination rate in the inversion layer via reducing the carrier lifetimes and excluding electrons from transport mechanisms. At each temperature, the filled traps originate Coulombic scattering phenomena that determine a positive shift of V_{TH} and reduce the device output current. On the other hand, the more the temperature increases the more the number of filled traps decreases. Thus, the threshold voltage variation with N_t decreases.

The carrier mobility is another fundamental physical parameter strongly affected by temperature and defects. In more detail, the total carrier mobility is a sum of different contributions depending on the material doping concentration as well as on the local electric field in the device structure and the scattering mechanisms from interface charges and ionized impurities in the bulk. For the proposed MOSFET, the carrier mobility degradation in the inversion layer due to the intrinsic defect concentration at different temperatures is

shown in Figure 7. With respect to the fresh device ($N_t = 0$), we can state that the increased recombination effects relate to the progressive increase of N_t have a severe impact on the channel mobility (μ_{ch}) at any value of T.
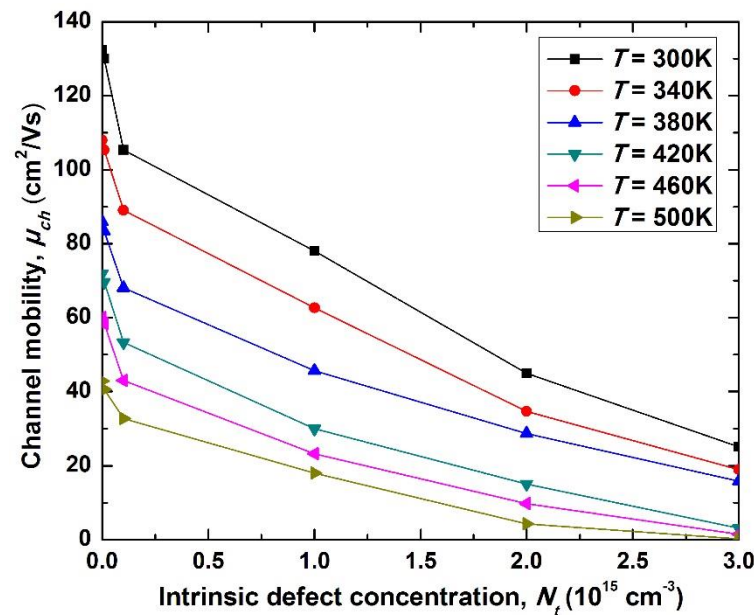

Figure 7. Channel mobility as a function of N_t at different temperatures. $V_{GS} = 12$ V, $V_{DS} = 1$ V.

The R_{ON} curves as a function of N_t for three different temperatures are shown in Figure 8.
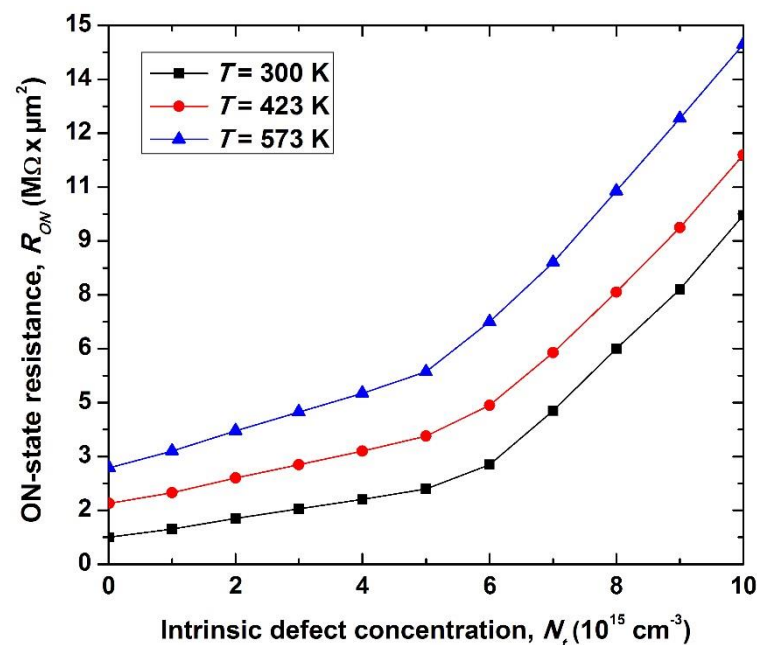

Figure 8. ON-state resistance as a function of N_t at different temperatures. $V_{GS} = 12$ V, $V_{DS} = 5$ V.

The presence of 4H-SiC intrinsic defects increases R_{ON} considerably with an almost similar behavior in dependence of T. This result is more noticeable the closer N_t approaches (overcomes) the epilayer doping concentration (5×10^{15} cm^{-3}). In fact, these defects act as efficient recombination centers both in the channel region and in the drift region causing higher resistive paths for the current flow. In particular, in a physical device, $Z_{1/2}$ centers with their negative-U nature (i.e., the Z_1 and Z_2 energy levels are very close to each other)

can be considered able to capture couples of electrons almost simultaneously. At the same time, the positively charged $EH_{6/7}$ defects (when empty), with their larger cross sections for electrons, are deeply involved in the detrimental effects in the channel region of an n-type MOSFET.

After fixing $N_t = 2 \times 10^{14}$ cm^{-3}, in order to refer the MOSFET analysis to a more realistic device, in the successive simulations the trap effects at the 4H-SiC/SiO$_2$ interface have been accounted for. As expected, these interface traps heavily affect the device performance by degrading the channel mobility and increasing the channel resistance contribution further. In a first step, we have investigated the role of the fixed oxide traps by assuming, in accordance with experimental data [41–43], a reference value $N_{fix} = 1 \times 10^{12}$ cm^{-2} into a thin film of SiO$_2$ located at the 4H-SiC interface. These centers, which number can be assumed independent from T, are positive charges responsible for the semiconductor band-bending at the interface [57,58]. The band-bending effect sustains the formation of the conductive channel for lower values of V_{GS} and therefore tends to reduce the MOSFET threshold voltage as shown in Figure 9.
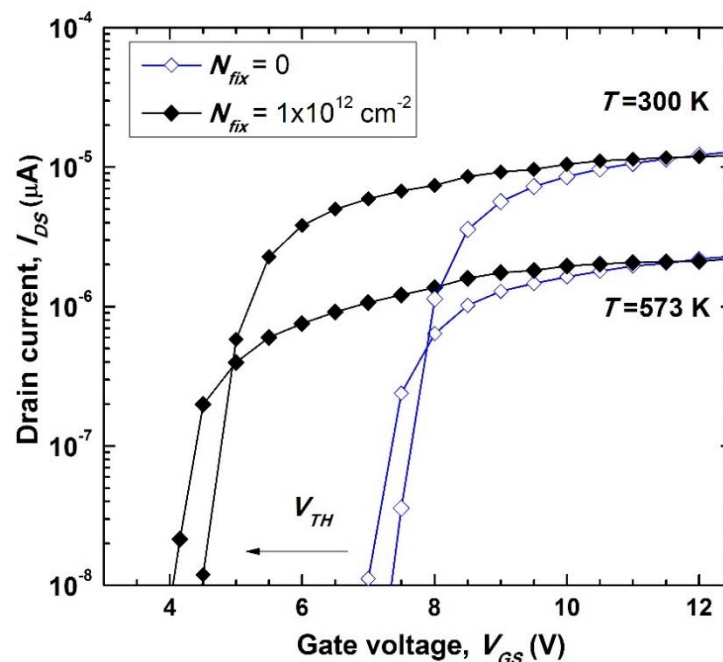

Figure 9. I_{DS}-V_{GS} curves for different values of N_{fix}. $V_{DS} = 1$V.

By comparing the I_{DS} curves for $N_{fix} = 0$ and $N_{fix} = 1 \times 10^{12}$ cm^{-2} we can note a significant shift to lower gate voltages. These behaviors aid to clarify the key role of the fixed oxide traps in determining the effective MOSFET V_{TH} both at low and high working temperature.

In a second step, we have finally involved in the simulations an explicit interface-trapped charge. In more detail, by assuming the DoS parameters listed in Table 3, from the simulations it was rather evident that the traps mainly affecting the MOSFET ON-state current capabilities are those located in the upper half of the bandgap. In fact, since the proposed device is a n-channel MOSFET operating in the inversion regime, the more the Fermi level moves in the upper half of the bandgap the more the traps with energetic states close to the conduction band govern the device electrical characteristics. On the other hand, in the subthreshold regime, when the Fermi level is close to the middle of the bandgap, it is the deep level distribution of states in the midgap to be occupied.

The tail traps effect on the MOSFET channel mobility and threshold voltage at $T = 300$ K is shown in Figure 10. In particular, starting in (4) from the reference value $D^0_{TC} = 5.72 \times 10^{13}$ cm^{-2} eV^{-1} [43], we have investigated a wide range of trap densities (1×10^{12}–1×10^{14} cm^{-2} eV^{-1}). It is important to note that the results in Figure 10 also

involve the combined effects due to the fixed oxide charge ($N_{fix} = 1 \times 10^{12}$ cm^{-2}) and the 4H-SiC intrinsic defect concentration ($N_t = 2 \times 10^{14}$ cm^{-3}).

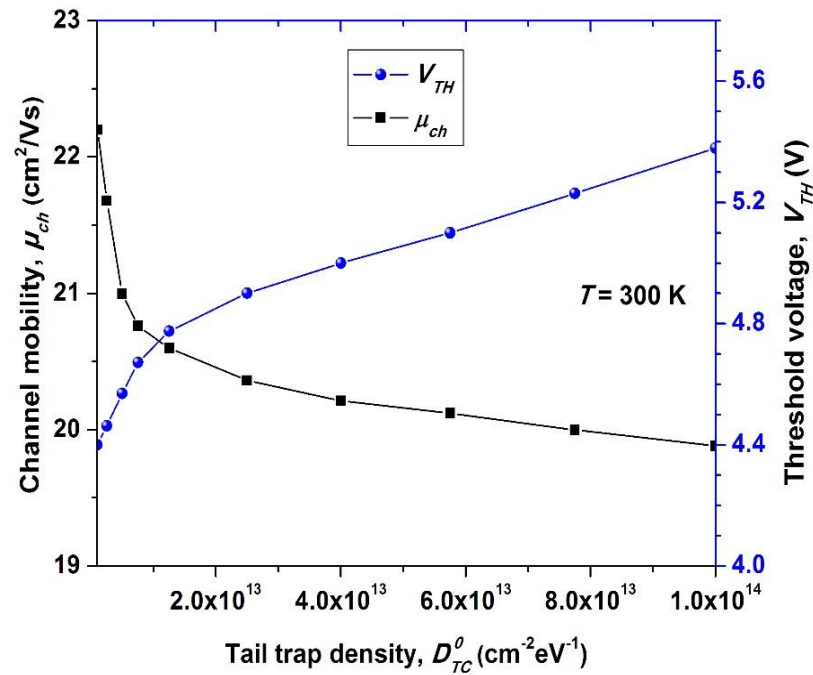**Figure 10.** Channel mobility ($V_{GS} = 12$ V, $V_{DS} = 1$ V) and device threshold voltage as a function of the tail trap density. $D_{Mid} = 2.4 \times 10^{11}$ cm^{-2} eV^{-1}.

When increasing the tail traps, they are able to trap an increasing number of electrons in the near-threshold regime of the device, preventing the complete channel formation and thus determining a positive shift of V_{TH} similarly to the intrinsic defect concentration effect. At the same time, the increased number of filled tail traps increasingly enhances the scattering phenomena of mobile charges in the inversion layer for $V_{GS} > V_{TH}$. For example, we can expect a channel mobility which is about 20 cm^2/Vs for $V_{GS} = 12$ V and $V_{DS} = 1$ V. In particular, a tail trap density up to 1×10^{13} cm^{-2} eV^{-1} leads to a faster variation of the μ_{ch} and V_{TH} curves. From the literature, a D^0_{TC} value close to 1×10^{13} cm^{-2} eV^{-1} was extracted experimentally in [41]. However, other experimental works dealt with a tail trap density of about 6×10^{13} cm^{-2} eV^{-1} [42,43]. Obviously, the exact value is strictly dependent on the available technology and device fabrication process.

In principle, we can assume that the carrier mobility behavior in the MOSFET structure is controlled by Coulomb scattering for low gate voltages around V_{TH} whereas for an increasing V_{GS}, which increases the transverse electric field and more and more confines electrons at the 4H-SiC/SiO$_2$ interface, the surface scattering effects in the channel region become dominant. In other words, for high gate voltages, due to an increased screening of the interface and fixed oxide traps by the inversion layer, Coulomb scattering is less effective.

By performing a detailed high-temperature analysis, interesting information on the interface trap effects can be extracted. In fact, although with an increasing temperature the fixed oxide charge can be assumed constant and the role of the midgap density of states remains negligible, the distribution of the band-edge interface trap densities is temperature-dependent through the band-tail energy parameter (U). In particular, while the temperature increases and the bandgap narrowing effect starts, the tail state profiles spread deeper into the bandgap with a reduction of the band-edge intercept densities. In more detail, to evaluate the MOSFET current capabilities at $T = 573$ K, we have used in (4) $U_C = 120$ meV (67 meV @$T = 300$ K) and $D^0_{TC} = 3.2 \times 10^{13}$ cm^{-2}eV^{-1} (5.7 $\times 10^{13}$ cm^{-2}eV^{-1} @$T = 300$ K).

These values are expected from the experimental data reported in [43] since their temperature dependence is almost monotonic.

Figure 11 shows the MOSFET R_{ON} behaviors calculated at low and high temperatures, assuming the joint contribution of all the defect/trap effects described previously. Here, the curves presented in Figure 4 for a fresh device are also reported for comparison.
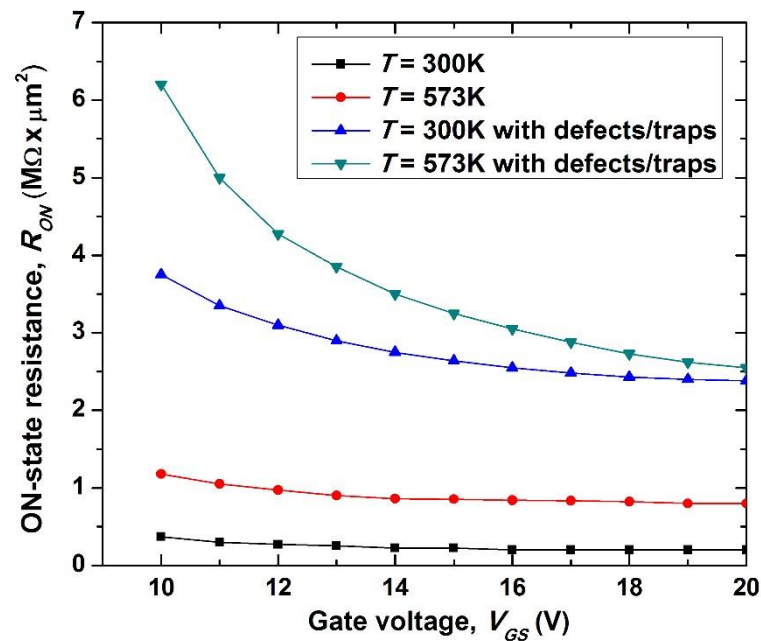

Figure 11. ON-state resistance versus V_{GS} for alternative devices with and without defect/trap effects. V_{DS} = 1 V.

It is worthwhile noting that, when the temperature increases from 300 K to 573 K, in contrast with the electrical characteristics of a fresh device, for a more realistic MOSFET the difference in the R_{ON} curves tends to reduce with V_{GS}. In particular, at the higher gate biases R_{ON} increasingly becomes slightly dependent on temperature although a large variation of T is considered. For example, $R_{ON} \approx 2.5$ MΩ·μm^2 with a ΔR_{ON} close to 10% for V_{GS} = 18 V. This limited R_{ON} increase with temperature for a MOSFET with defects and traps represents a key finding of the presented analysis. It can be explained by considering that while Coulomb scattering is directly proportional to the occupied density of states, it is inversely proportional to the device operation temperature. In other words, since mobile carriers have more energy with increasing values of T, they are less affected by the Coulomb potential at the 4H-SiC interface and, therefore, for a given ON-state bias condition, much more electrons are available for conduction in the inversion layer. From the simulations, the more the number of the interface trap states is large the more this effect is evident in counteracting the current reduction due to the lower carrier mobility in the channel region as verified for the fresh device.

In sum, the observed results in Figure 11 depend on both the occupied density of states and temperature. In particular, the fresh device presents a R_{ON} curve with a positive temperature coefficient that is almost constant in the whole explored V_{GS} range (i.e., $\Delta R_{ON} \approx 300\%$ @T = 573 K) whereas a MOSFET structure involving intrinsic defects and an explicit DoS at the gate oxide interface presents a decreasing ΔR_{ON} in dependence of V_{GS}. Obviously, the presence of defects and traps leads the MOSFET to operate with a lower drain current at any fixed bias voltage and temperature. As an additional result note that, with respect to the curves in Figure 11, by reducing the trapped charge density by a factor of 10 we have calculated an R_{ON} improvement on the order of 15% preserving about the same ΔR_{ON}. This improvement is certainly due to an increased inversion charge and an enhanced channel mobility.

Finally, it could be interesting to cite the state-of-the-art of Si-based super-junction power devices rated in the 600–700 V class which, while showing a specific R_{ON} around 2 MΩ·μm^2 at room temperature [59], suffer for a severe performance degradation with T ($\Delta R_{ON} \approx 150\%$ @T = 423 K) under test conditions [60]. On the other hand, datasheet values in terms of ΔR_{ON} for similar 4H-SiC-based MOSFETs [2–4] confirm the results obtained in this paper.

5. Conclusions

An exhaustive simulation study on the electrical characteristics of a power MOSFET in 4H-SiC is presented, accounting for trap and defect effects which originate in the bulk and at the gate oxide interface. Starting from a fresh device, the joint contribution of defects and traps determines a significative shift of the threshold voltage and increases the MOSFET R_{ON} at any working temperature. In more detail, the intrinsic defect concentration should result at least one order of magnitude lower than the epilayer doping concentration to avoid the formation of high-resistive paths for current. At the same time, the temperature-dependent physics of the density of states located at the SiO$_2$ interface plays a key role in determining the MOSFET output characteristics. In fact, in contrast with the electrical behavior of a fresh device, in presence of defects and traps, the calculated increase of R_{ON} with temperature decreases for increasing values of V_{GS}. In particular, for V_{GS} higher than 16 V, the R_{ON} value remains around 2.5 MΩ·μm^2 with a percentage variation in the limit to 20% although a large excursion of temperature is considered (300–573 K). The presented analysis turns useful to assess the effects of different scattering phenomena in the device inversion layer and drift region, thus supporting a clear understanding of the proven reliability of 4H-SiC-based MOSFETs for high-temperature applications.

Author Contributions: Conceptualization, F.P., L.D. and F.G.D.C.; methodology and validation, F.P., H.B., L.D. and R.C.; software, H.B., G.D.M. and M.M.; investigation, F.P. and H.B.; data curation, F.P., G.D.M. and M.M.; visualization, F.P. and R.C.; writing—original draft preparation, F.P.; writing—review and editing, F.P.; formal analysis and supervision, F.P., L.D. and F.G.D.C. All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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