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Study and Design of Silicon Carbide Power MOSFETs for Low Voltage Applications

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ABSTRACT

Advances in Silicon Carbide (SiC) crystal growth especially the development of chemical vapour deposition (CVD) have encouraged the fabrication of high-quality SiC. Nowadays, in the market are available wafers of quality similar to Silicon, and although the production costs are still high, they are continuously decreasing. This slow decrease in prices has aroused greater interest in SiC devices. Thus all the major worldwide manufacturers of electronic components faithful to the undisputed Silicon, have started to investing more resources to improve the production technologies of Silicon Carbide devices. Moreover, new wafer processing systems have developed for improving the wafers production yield and of final quality, while reducing costs.

Other developments have been achieved about post-treatment process for the wafer, indeed, nowadays the produced SiC wafers present a reduced impurity distribution that can be responsible for the formation of defects and traps. Impurities in semiconductors play an important role to modify their physical properties. The doping of a semiconductor introduces shallow defect levels to increase the conductivity. Impurities, especially transition metals, generate defect-levels deep inside the SiC bandgap, which are able to trap charge carriers and thus reduce the lifetime of charge carriers.

Thanks to this recent progress in SiC-technology, power devices are now commercially available from worldwide manufacturers such as Infineon, Cree, and GeneSiC. SiC guarantee excellent devices for power applications, for example, faster-switching speed compared to Silicon devices, which can lead to superior converters performances because converters can operate at higher switching frequencies with reduced switching losses.

SiC power MOSFETs are available only for above 600 V. The aim of the first part of my research is the prediction of the electric characteristics of a "novel" 4H-SiC MOSFET, tailored for power optimizers used in photovoltaic modules for low voltage category of DC-DC converters, therefore characterized by a breakdown voltage

BV_{DS} of 150 V, and currents of the order of 10 A. This study is based on numerical simulations. The obtained results show that the static characteristics would be comparable to those of Silicon MOSFETs rated for a comparable BV_{DS}, with an ON-state resistance R_{ON} in the order of 100 $k\Omega \times \mu m^2$. But, SiC MOSFETs show advantageous results in terms of dynamic characteristics, and in particular in terms of switching times. BV_{DS} and R_{ON} are inversely related to each other, therefore the R_{ON} optimization must be obtained without affecting the fixed BV_{DS} value. Power MOSFET optimization could be pursued in different ways. Recent scientific research has proposed new cells design, such as the super-junction and lateral trench gate, both introduced to reduce mainly the R_{ON} of power MOSFETs. This problem was also addressed in this Thesis. Thus, after having dimensioned the MOSFET cell for the set breakdown voltage value, the channel length has been optimized and next to the channel resistance which is a heavy component of ON-state resistance.

The second part of this dissertation was carried out to detail the relative weight of interface defects and traps in a 4H-SiC MOSFET. The experimental results confirmed the theoretical ones, in fact, numerical simulations have confirmed that these can affect (in variable measure depending on the ultimate SiC-wafer quality and by other extra chemical post-processes) deeply on the MOSFET's channel, increasing its resistance. As expected, at high power, degradation processes are mainly related to impact-ionization and of hot-carriers. That of hot-carriers is a phenomenon strictly correlated to the defect and trap distributions inside the bulk semiconductor and at the interface with the gate oxide. Accurate physical models for defects and traps distributions have been studied and applied to the designed MOSFET.
The role of an explicit defects state concentration at the SiO_2/SiC interface in determining the R_{ON} value of a 4H-SiC power MOSFET has been investigated. Numerical simulations have been performed and produced results have shown, for different temperatures, the traps distribution impact on the electrical characteristics. The percentage variation of R_{ON} was about 40% for low gate voltages at room temperature.

More complex has been the scenario in which were considered the conjoint contributions of defect and trap distributions inside the designed structure. First of all, the conjoint behaviour of traps and defects depends mainly on their relative concentrations and where they are located inside the structure. Moreover, it is important to consider the depth where these distributions have been allocated. In this context, also temperature plays an important role; in fact, it has a strong influence not only on the physical parameters of the device but even on the defects and traps distributions. From a theoretical point of view, we can affirm that the impact of defects and

traps on the physical and electrical properties of the device could be represented as a multi-parametric function with many degrees of freedom.

Note for the reader.

Almost all scientific publications are usually paginating with the formatting of text such to group all the figures together, along to the same line, in a group of two or even three elements. This choice undoubtedly allows for better appearance vision. In this thesis, I have preferred that the aforementioned group be reduced to a single figure. Although this choice could seem unprofessional, however, it greatly improves the reading of data, emphasizing better those details that in the other mentioned manner would be hard to read and therefore difficult to interpret. I apologize to readers who would have liked the other arrangement.

Outline of the thesis

The commercial SiC power MOSFETs are developed only in the voltage range from 650 V to 2.0 kV, thus below 650 V it is still the domain of Silicon.

In this thesis, the design of a SiC power MOSFET has been studied and numerically evaluated. After a deep study of the literature, we have considered SiC enough reliable and innovative, to develop a new device in the voltages-class not yet covered by the commercial devices. Thus, a "novel" 150-V-class has been designed, indeed a deep study has been developed to evaluate its electrical characteristics and so its performances. Due to the inevitable presence of defects and traps in SiC and oxide the performance of device they can also worsen exponentially, thus we have evaluated the weight of defects and traps that are inevitably present in the commercial devices and that tend to reduce their electrical performance.

The whole corpus of this thesis has been organized in two main parts, and in toto, it is composed of five chapters, which content is reported below. The first part contains a deep exposition on SiC, and a presentation of 4H-SiC MOSFET structure with its main physical models and parameters used to simulate our designed MOSFET structure. The second part contains the presentation and discussion of the main results obtained in this research's work and an outlook on its future development.

Chapter-1. This chapter contains a general introduction on the power devices, technical consideration and some information about the market-trend of power devices. In particular, the two most promising and discussed wide bandgap materials of the moment are taken into consideration: Silicon Carbide and Gallium Nitride. This brief presentation and comparison between the two contenders will try to highlight and explain our choices towards the choice of Silicon Carbide. Finally, has been presented the section on the objectives of the thesis work.

Chapter-2. In this chapter has been reviewed the main physical and electronic properties of SiC. All topics covered in this chapter have tried to cover up all the

fundamental properties recalled in chapter 3 and concerning the physical modelling of the MOSFETs in SiC. Particular emphasis is given to the 4H polytype, since, due to its properties, it is the most used polytype in the microelectronics industry.

Chapter-3. This section begins with a very brief presentation of the numerical simulation tool used for this research work, it is not a complete exposition of its features, which are entrusted in the massive Silvaco manuals. Have been reviewed very briefly the main power MOSFET structures, but, particular interest has been given to the vertical DMOSFET structure. Moreover, has been presented the main physical models used to perform the numerical simulations of designed 4H-SiC MOSFETs. In the last part are reported some consideration on robustness and reliability of SiC power MOSFETs.

Chapter-4. For a better exposure of the results this chapter has been shared out in further two parts:

The **Part I** contains the study and results achieved about the design of a novel SiC power MOSFET for photovoltaic ($BV_{DS} = 150\ V$) applications. This study has been further improved with the study of interface traps present at the interface between the channel region and gate oxide.

The **Part II** begin with the presentation of a SiC power MOSFET for higher voltage-class ($BV_{DS} = 650\ V$) than that of PV applications. For this structure has been evaluated the effects of interface defects and then, of the conjoint effects of defects and traps. The results obtained at room temperature, high temperature and very high temperature have been compared and discussed for the evaluation of the device's performance.

Chapter-5. Finally, has been discussed the conclusions about this research work and has been suggested a possible new line of research for optimization of performance for the designed power MOSFET. This could be possible thanks to the use of heavily doped semiconductor junctions used as top-layer at the interface of the channel region.

1

INTRODUCTION

Success is never definitive, failure is never fatal; it is the courage to continue that counts.

Winston Churchill

1.1 Introduction

NOWADAYS about 40% of the world energy use is provided by electric power. It is expected that this percentage is going to rise to about 60% until 2040. Total sales of power semiconductors are growing 10% per year. This is driven by the need to produce an efficient use of electricity, increasing the use of renewable energies and change to electric vehicles. Electricity has to be converted in many steps, from power generation to use, by adjusting voltage and frequency. Using conventional Silicon-based power electronics 5-10% of the energy is lost in each step and up to more of 20% with a classic passive 50 Hz transformers. With Silicon Carbide (SiC) these losses can be radically reduced, theoretically up to 90%! This will have a large impact on high power electrical systems. The main benefits with SiC power electronics are [1]:

1. Energy efficiency

- For an electric car where the current goes several times between battery and motor, SiC extends the driving range of about 10%.
- For a commuter train, efficient re-use of braking energy save 30% electricity.
- For industrial applications with the 24h operation, to replace an old transformer with an electronic module based on SiC devices, requires a ROI[1] less than 3 years.

[1] Return Of Investment

2. System efficiency

- Smaller size. Size reduction can increase switching frequency up to 1000%, and correspondingly reduce the size of capacitors, coils and magnets. Moreover, it is possible to use power transformers of about 80% smaller, and thus of lower weight.
- Less cooling. Lower losses generate less heat and thus require less cooling of a power transformer. This simplifies the whole system design by e.g. replacing water cooling with passive air-cooling.
- Lower cost. Less use of materials and use of a simplified cooling system reduce significantly total cost of the power section.

The first two generations of semiconductor materials are represented by Silicon (Si) and Gallium Arsenide (GaAs), respectively. Wide bandgap materials, such as SiC and Gallium Nitride (GaN), are known as the third generation semiconductor materials. SiC was discovered in 1824 by Berzelius during his diamond synthesis experiment. The first use of SiC was as an abrasive. This was followed by electronic applications. SiC became popular since 1907 when H. J. Round produced the first LED by applying a voltage to a SiC crystal and observing yellow, orange and green emissions at the cathode. This result attracted curiosity and interests of electronic researchers, thus across years the 60s and 70s, the interest in SiC of the semiconductor industry was recognized. Compared with Silicon, the most widely-used semiconductor material, SiC has many remarkable electronic properties including wide bandgap (WBG), a large critical electric field (E_{cr}), high thermal conductivity, high electron saturation velocity ($\nu_{n,sat}$)[2] [2], chemical inertness, and radiation hardness [3].

These excellent properties make SiC very well-suited for high-voltage, high-power, and high-temperature applications. Nowadays, the commercial availability and developing of SiC devices are rapidly growing. Process technology, such as high-quality single-crystal substrate and device fabrication processes at a low price, has had great progress.

Since 2001, Infineon Corporation started to supply SiC Schottky diodes. Now SiC diodes, JFETs, BJTs, MOSFETs, and other SiC three-terminal devices are available, GeneSiC, CREE, Toshiba, STMicroelectronics, SiCED and other companies have the ability to supply SiC power devices. However, the main obstacles for the development of SiC-based devices are the quality and costs of SiC materials compared with its Si-based counterparts. With the recent progress in the process of SiC epitaxial materials, it is feasible to obtain high-quality 4H-SiC substrates and epilayers, and thus achieve

[2] For 4H-SiC at $T = 300\ K$ result: $\nu_{n\parallel}^{sat} = 2.2 \times 10^7\ [cm/s]$ and $\frac{\nu_{n\perp}^{sat}}{\nu_{n\parallel}^{sat}} = 1.16$

excellent power performances for SiC power devices. Great interest in SiC of more researchers and companies are paying attention to SiC materials, a heavy drop in costs is forthcoming and affordable costs can be expected in the near future; which, in turn, will promote the development of SiC power devices.

Power devices are required for applications that operate over a broad spectrum of power levels and frequencies. In Fig. 1.1 [4], the applications for power devices are shown as a function of operating frequency. High power systems, such as HVDC (High Voltage Direct Current) power distribution and locomotive drives, which require the control of the high level of power (in the Megawatts order) operate at relatively low frequencies. As the operating frequency increases, the power ratings decrease for the devices with typical microwave devices handling about 100 W. Today, all of these applications are served by Silicon devices.

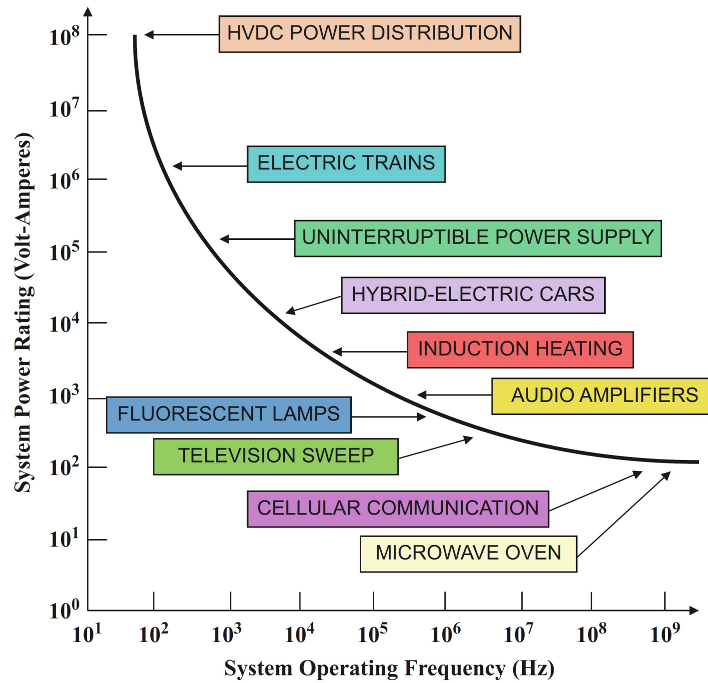

Fig. 1.1. Applications for power devices.

The development of power devices from wide bandgap semiconductors, such as SiC, allows extending the operating voltage of unipolar structures to at least 5 kV. In modern power circuits, it is regular to utilize power transistors as switches to control power flow to the load, while power rectifiers are used to control the direction of current flow.

1.2 The choice: SiC or GaN for low voltage converters?

Wide band-gap (WBG) semiconductor technologies such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are the hot topics of the moment, promising anything from universal wireless charging to power converters shrunk to almost no size. However, the choice between the technologies and devices available is not always straightforward.

Silicon Carbide and Gallium Nitride (GaN) semiconductors are competing for use in automotive and industrial applications with performance superior to current Silicon technology. SiC and GaN are wide bandgap (WBG) semiconductors that have attracted a great level of attention for many years, thanks to their several material properties making them ideally suited for high power, high-frequency applications (the semiconductor bandgap indicates the amount of energy required to push an electron into a conducting state).

For GaN these properties are the following:

- It has $E_g = 3.4\ eV$ [5] over $3\times$ that of Silicon. This large energy gap gives it the ability to withstand high electric fields (GaN has a $BV_{DS} = 3.3\ MV/cm$), high operating temperatures [6], [7].
- High electron mobility ($\approx 900\ cm^2/V \cdot s$ in GaN) coupled with the ability to withstand high voltages permits reaching for higher saturation velocities ($2.7\times 10^7\ cm/s$) and higher operating frequency [5].
- High mechanical/thermal stability combined with good thermal conductivity for dissipating heat essentially for devices on SiC substrate, so devices can operate at higher temperature and power.

Thus, WBG devices include GaN and SiC, which are listed in the Table1.1 [8] [3].
The WBG benefits include:

- Elimination of up to 90% of the power losses that occur during power conversion.
- Up to 10X higher switching frequencies than Si-based devices.
- Operation at higher maximum temperature than Si-based devices.
- Systems with reduced life-cycle energy use.

Although WBG semiconductors now cost more than Silicon devices, they may eventually be competitive as manufacturing capabilities improve and market applications grow. Several challenges must be addressed to make WBG materials more cost-effective, including:

[3] Note:(*) respectively value of epitaxial layers and bulk value. (**) respectively the bulk value and the 2-dimensional gas value (2DEG)

Table 1.1. ELECTRICAL PROPERTIES OF GaN, 4H-SiC.

Property	**GaN**	**4H-SiC**
Energy Band Gap $[eV]$	3.40	3.26
Electron Affinity $[eV]$	1.84	3.70
Thermal Conductivity $[W/cm-K]$	1.3/3.0(*)	3.0 - 4.0
Intrinsic Carrier Concentration $[cm^{-3}]$	10^{-9}	10^{-7}
Satured Electron Drift Velocity $[10^7 cm/s]$	2.5	2.0
Breakdown Field $[MV/cm]$ @ $N = 10^{17}\ cm^{-3}$	3.0	$\|\|$ 3.20 $\perp$ 1.00
Electron Mobility $[cm^2/Vs]$	990-2000(**)	800
Relative Dielectric Constant	9.0	10.00

- Production of larger-diameter WBG wafers.
- Use of novel designs that exploit the properties of WBG materials.
- Use of alternative packaging that enables higher-temperature WBG devices.
- Design of systems that integrate WBG devices so that they take advantage of their unique capabilities.

GaN and SiC semiconductor materials allow for smaller, faster, more reliable devices with higher efficiency than their Silicon-based competitors. These capabilities make it possible to reduce weight, volume, and life-cycle costs in a wide range of power applications. Fig.1.2 compares the breakdown voltage and R_{ON} of Silicon, SiC, and GaN devices.

Coming later than SiC, GaN has had slow adoption due to cost, yield and reliability concerns. It is certainly theoretically capable of higher switching speed than SiC or Silicon, with its higher electron mobility, but with a thermal conductivity lower than SiC by a factor of three, its power density potential is limited. Currently SiC devices are common at around 650 V through 2.0 kV rating and higher, while GaN is limited to around 650 V, where it struggles to compete with the current lower cost and proven robustness of the more mature SiC offering at the same voltage. GaN suppliers are hoping that the lower voltage/power market including data centers, EV/HEV and photovoltaics.

Compared to Silicon, SiC has:

- R_{ON} up to two orders of magnitude lower.
- Reduced power loss in power-conversion systems.
- Higher thermal conductivity, and higher temperature operation capability.
- Enhanced performance due to material advantages inherent in its physical properties.

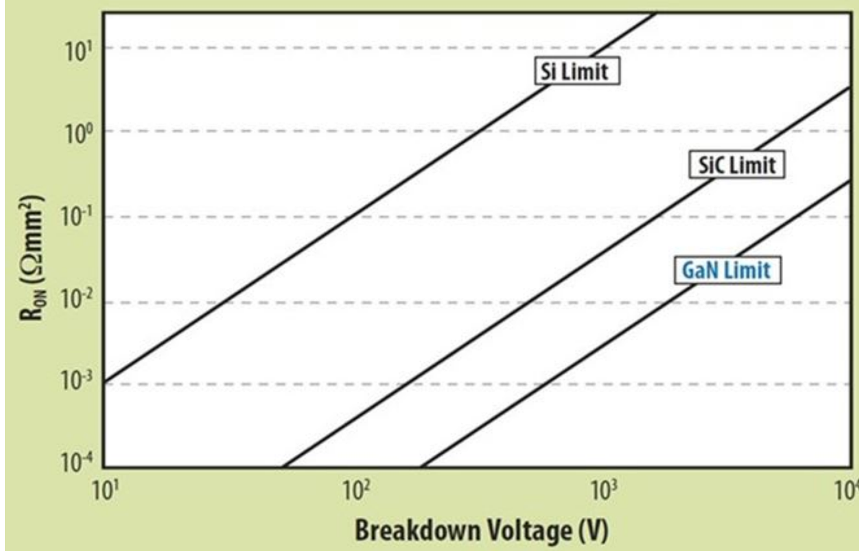

Fig. 1.2. theoretical ON-state resistances: comparison of Si, SiC, and GaN.

SiC excels over Silicon as a semiconductor material in 600 V and higher-rated breakdown voltage devices. Compared to Silicon, GaN has:

- GaN FETs present the temperature coefficient of R_{ON} positive as the Silicon MOSFET, but the magnitude is significantly less.
- Compared to a Silicon semiconductor, GaN presents higher electron mobility and smaller-size device for a given R_{ON} and breakdown voltage.

As a result, GaN devices can be physically smaller and have electrical terminals closer together for a given breakdown voltage requirement. Silicon power MOSFETs have not been able to keep pace with the changes in power electronics applications. Silicon has reached its theoretical performance limit, thus, for the power and R.F. applications, we need to turn to other semiconductor materials, such as GaN or SiC. The devices realized for high frequencies (approximately 300 kHz to over 300 GHz) and high powers that can exploit the advantageous features of the GaN represent variants of the FET transistors and are mainly made up of **MESFET** (MEtal Semiconductor Field Effect Transistor) and **HEMT** (High Electron Mobility Transistor); in particular the latter represents the most promising technology and can guarantee far superior performance.

While MESFETs are devices whose operation is based on the realization of a metal-semiconductor Schottky junction, with the possibility of controlling a conductive channel formed on a homogeneous substrate, the HEMTs exploit the advantages of GaN in making heterostructures. In fact, HEMT transistors are also called HFET (Heterostructure Field Effect Transistor) and their heterostructure leads to the for-

mation, in correspondence of the GaN / AlGaN etiquette, of a 2DEG electronic gas, characterized by electronic mobility and carrier density (10^{13} cm^{-2}) high. The combination of these two characteristics leads to a high current density and low channel resistance, very important factors in high-frequency applications and high power. These excellent properties of the 2DEG are a consequence of the strong polar nature of the GaN crystal and of the mechanical stresses that are generated in the deposition of materials with different reticular constants to form the heterostructure, which lead to further piezoelectric polarization. Moreover, the GaN allows to realize heterostructures of two different polarities, Ga-Polar and N-Polar; while at first the attention was concentrated almost exclusively on the Ga-Polar technology, which enjoys better electrical qualities and stability of the materials, with the development of epitaxial growth techniques the realization of N-Polar transistors has opened up to new possibilities and design solutions; in particular, proceeding with the reduction of the size of the devices and with the increase of the operating frequencies, the N-Polar allow to overcome some limits that are encountered with the Ga-Polar transistors, ensuring low contact resistance and better electronic confinement in the 2DEG channel. Considering this, it was considered of particular interest to proceed to the study of the functioning of the devices made on GaN, with special attention to the levels of reliability and with an investigation also aimed at the degradation mechanisms to which such devices can incur, so as to identify solutions that allow the technology to achieve even better robustness and performance. In Fig.1.3 [9] for Silicon, SiC, GaN and GaAs are reported the trends of their specific ON-state resistance as a function of critical electric field for the breakdown. SiC and GaN have similar properties, but chipmakers for high-frequency applications prefer to use the GaN for its superior electron mobility (Fig.1.3) that allow reaching higher frequency. The well-known Fig. 1.4 [9] compare on a radar-diagram the main physical material properties of the semiconductor considered here. In this case, it is clear that the good SiC temperature behaviour combined with its higher reliability, decree the SiC as an elected material for power applications.

Figure 1.4 shows a comparison between GaN, Silicon and GaAs advantages for RF and power supply circuits. The GaN is preferable for high-frequency, high-power, high-voltage, and low-loss operating specifications transistors [5]. But, for application in harsh environments at high temperature it is preferable to use SiC, thanks to its higher capacity to work at high temperature and also to its superior thermal conductivity.

Scientific research is moving towards the study of multi-material structures, ie devices in which SiC and GaN coexist, and where each material is delegated to the functions it performs best. In this case, it is understood that the power section would be made in SiC, while the R.F. section in GaN.

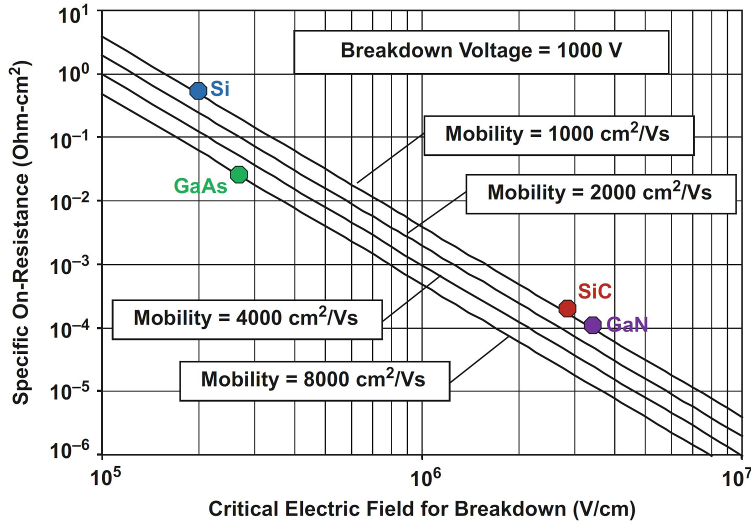

Fig. 1.3. ON-state resistance vs critical electric field for Breakdown voltage.

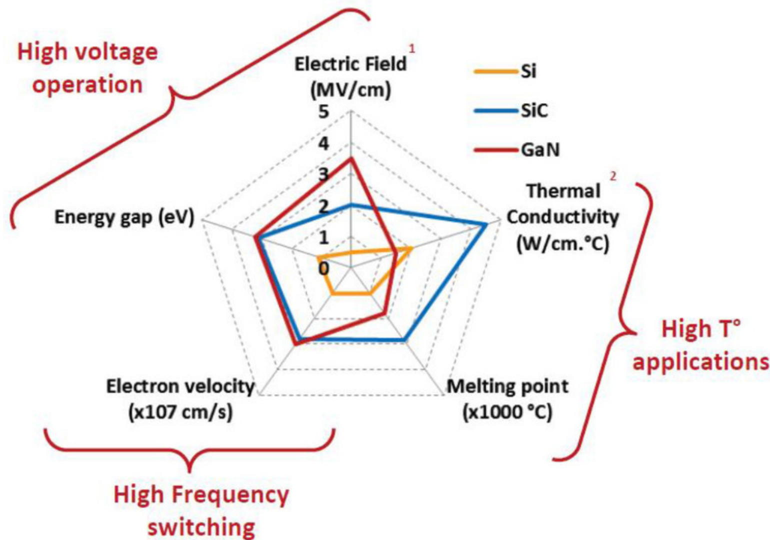

Fig. 1.4. Comparison: GaN vs SiC vs Si.

1.2.1 GaN Reliability issues

Del Alamo et al. [10] have presented new evidence behind an electrical degradation mechanism for GaN HEMTs that is associated with the strong piezoelectric effect of GaN. Indeed, at high voltage conditions, the high electric field that is produced is responsible for strong stress inside the GaN HEMT. This produces an increase in accumulated elastic energy inside the cell. But, if this energy exceeds a critical value, there will be the production of crystallographic defects electrically active. This provides a path for the excess of gate leakage current and it also results in electron trapping that exhaust the sheet charge in the channel resulting in degradation of many figures of merit. This degradation mechanism can be mitigated through opportune technological steps, but this makes us understand that for power applications (hot carriers, high impact ionization, etc) the GaN is less reliable than SiC. Despite the very good material properties, the device design that has become matured with intensive studies and large effort spent in recent years and the excellent device performances for both RF and high power switching applications, there are still some issues that limit the device practical applications. Reliability is one of the most important parameters before marketing a product. It is defined as the ability of a component, circuit or system to perform an intended or required function or mission without failure or degradation.

One important parameter to evaluate the reliability of a device is the Mean Time To Failure (MTTF). It is a statistical parameter referring to the time elapsed from the start of operation and the first failure. It assumes that the mathematical model of reliability is an exponential function, which value value represents the time where 63% of the samples under test will have suffered their first failure. This is a number often used to estimate the number of units needed to be stocked for replacements.

The reliability of semiconductors devices is associated with the failure rate $\lambda(t)$ [11] [4] over time described by a curve called "bathtub-curve". The main stress tests to assess reliability are electrical, thermal, mechanical, humidity, etc. The bathtub-curve represents the typical development of failures over time. There are three distinct zones: infant mortality; constant (random) failure; and wear-out failure. In the constant failure rate zone, failures occur in a random order – making it difficult to predict which failure mode will occur - but the rate of failures is predictable. Figure 1.5 represents a typical pattern of the 'failure rate' over a period of time.

[4] The failure rate is expressed as the ratio of the total number of failures to the total operating time: $\lambda(t) = K/T$, where K is the number of failures and T is the total operating time.

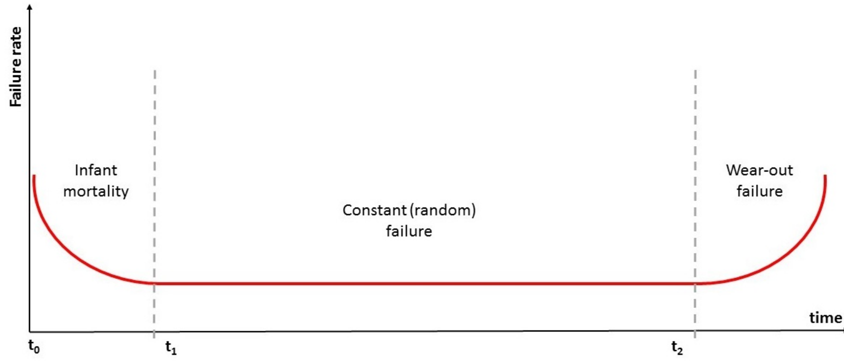

Fig. 1.5. The typical bathtub-curve.

Although impressive results were published for GaN-based transistors in a large frequency range, the performance and the reliability demonstration is still limited by a number of mechanisms and conflicting mean time to failure (MTTF) data on existing device designs which are a very important subject of concern.

In Fig. 1.6 [12] are reported a summary of the main failure mechanisms plaguing the GaN HEMT performances and reducing the device reliability.

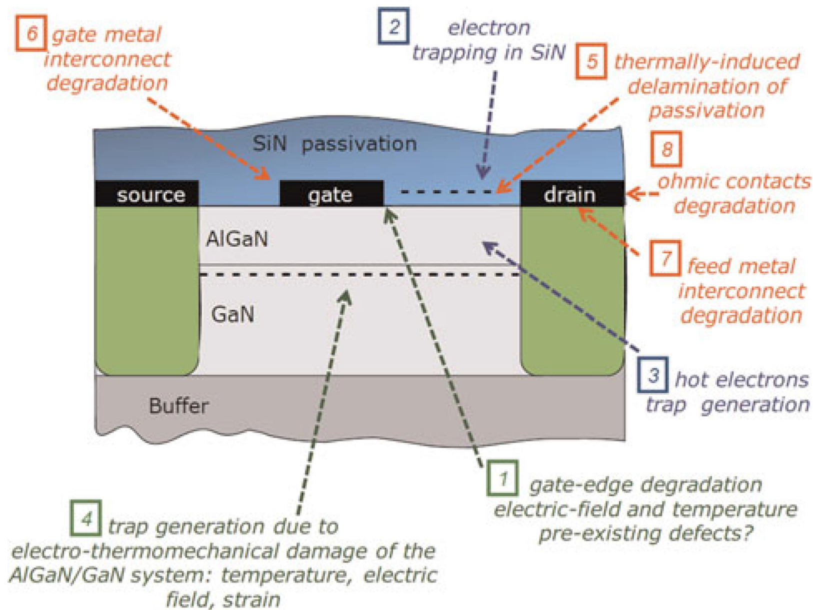

Fig. 1.6. Failure mechanisms identified on GaN based HEMTs. Red: Thermally-activated mechanisms/ Blue: mechanisms related to the presence of hot electrons (trapping effects)/ Green: mechanisms due to the polar and piezoelectric nature of the semiconductor material.

All these considerations make SiC more interesting and mainly more reliable for power applications.

1.3 Power MOSFETs in smart power switches

Originally, power MOSFET technologies were based on a double-diffusion process in which the formation of the inversion layer was obtained by controlling the depth of two junctions. Power devices realized in such a way, called Vertical-Diffused MOSFET (VD-MOSFET), had the drawback of a quite limited current capability due to their substantially large internal resistance (also called ON-resistance or ON-state resistance), which in turn represented a prominent limiting factor for both the device power management and the efficiency of the circuits in which they were utilized. Therefore, in the early 1990s, an improved technology was introduced for realizing new generations of power MOSFETs, i.e. the so-called trench technology. In general, compared to a VD-MOSFET, a power trench MOSFET shows a reduced ON-state resistance and allows higher operating frequencies (up to several MHz). In the last decades, along with the progressively improved power MOSFET technologies, automotive applications have impressively grown due to more demanding user requirements for increasing car performance, safety and comfort. Such a trend has led to a great development of automotive electronics towards higher complexity, which has resulted in a growing integration and miniaturization of power switches. Nowadays, most of the discrete switches used in the automotive environment, such as power transistors or electromechanical relays, have been replaced by complex semiconductor-based circuits, the so-called Smart Power (SP) switches. Those devices integrate within a single chip one or more power MOSFETs together with several analog circuits for driving and protecting the power devices and the loads, and the logic circuitry for managing the data exchange with the car control unit. In automotive applications, SP devices are mainly used for motor controllers, power supplies and lamps ballasting. In general, an SP device must reliably withstand a wide variety of electrical and thermal stresses during his operation in the harsh automotive environment. Some of the aforementioned stresses result from critical biasing conditions which may drive the power transistor towards a dangerous operating regime called thermal instability. Typically, main MOSFET parameters show a substantial temperature dependence, as a result of that a mutual interaction takes place between the electrical and the thermal field within the semiconductor device. Consequently, by defining margins of the thermally stable/unstable operating regime, the electro-thermal interaction may seriously limit the device lifetime. Therefore, today's semiconductor manufacturers particularly focus their attention on the electro-thermal robustness and reliability of power MOSFETs integrated into modern SP switches in order to guarantee a long operating lifetime during their use in the car environment. Afterwards, their Safe Operating Area (SOA)

in forward-biasing operations will be briefly recalled and concepts of reliability and robustness will be introduced accordingly.

1.4 Objectives of the thesis work: challenges and contributions

The core around which has been developed this dissertation are the numerical simulations. Thus, the study of two different MOSFET structures and the study about the defects and traps distributions inside the designed MOSFET structure have been studied thanks to a TCAD software and to a FEM (Finite Element Method) simulator which implements the physical models and run numerical simulations.

Nowadays, numerical simulations are considered an excellent estimation tool to shows the behaviour of a specific device. Most simulators are very good for Silicon, but for SiC the simulation shows divergent results. This is due to the different models for 4H-SiC adopted by each TCAD simulator. Even if certain models are the same, the parameters values may be different. Thus, after a preliminary evaluation phase about the choice of the more appropriate numerical simulator for our simulations needs, the next step was that to design a new geometric structure of power MOSFET adapt for PV applications. The work proceeded with the choice of all correct physical sub-models and parameters to apply for developing the whole final physical model, before proceeding with the numerical simulations and finally with the data analysis and interpretation. The motivations of this study are born around the idea that higher efficiency in photovoltaic (PV) conversion requires the use of small Maximum Power Point Trackers (MPPT) to be placed on board the PV modules. Such circuits require in turn power transistors with low energy losses, high switching speed and blocking voltages lower than 150 V. Thus, was investigate the more adequate semiconductor circuit topologies of power MOSFET used for commercial devices. In this process have been evaluated both planar and vertical power MOSFET structure, but after a deep introduction in literature was decided to take in account only vertical structures in SiC of type VMOS, UMOS and DMOS 3.3. However, there are still many challenges related to the development and optimization of a power DMOSFET. In Fig. 1.7 [13] is shown the Silicon and SiC shared market. For SiC MOSFETs below 600 V does not exist any commercial device. Thus, is born the idea to explore this empty research field, proposing the design of a "novel" device for photovoltaic applications.

Thus, starting from a conventional 4H-SiC power DMOSFET [5], a novel device for PV applications has been designed and numerically simulated in order to determine its

[5] DMOSFET: is vertical power Double-Diffused MOSFET, a technology developed for the formation of P-base and source regions

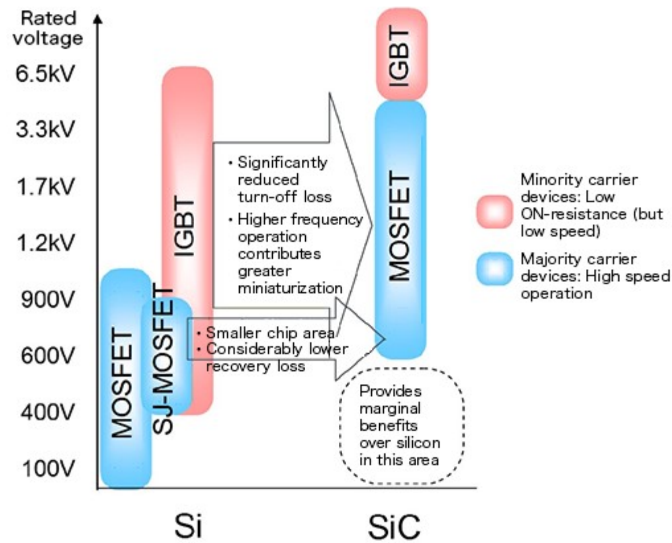

Fig. 1.7. Silicon and Silicon Carbide shared market. For SiC MOSFETs below 600 V it is an unexplored research field.

electrical characteristics including the ON-state resistance for different bias voltages (R_{ON}) that is an important electrical parameter to compare devices performance. The resulting value of R_{ON} was compared to that of a commercial Si-based MOSFET performing the same breakdown voltage. In order to accurately predict the switching behaviour of SiC-based power switching converters, it was necessary to use accurate physical models for the SiC MOSFET and to use the more recent 4H-SiC parameters in the switching loops of converters. The main difficulties faced during this project has been the following:

Firstly, to use an appropriate SPICE® software for the extraction of SPICE parameters from the physical model used in numerical simulation and the prediction of high-speed switching behaviour. This work has requested a SPICE simulator that also implemented the VDMOS SPICE model. Due to lack of software that implemented even the Vertical DMOSFET structure (used in this research work), the most part of SPICE extraction phase has request long simulation time and a very fine-tuning of each parameter.

Secondly, the evaluation of conjoint contributes to defects and traps distributions at the interface between channel MOSFET and gate oxide.

Has been produced two interesting contributions in this thesis. The first contribution is the design of a "novel" 4H-SiC DMOSFET device accounting for low voltage applications. Until now, commercial power MOSFETs has been developed in the voltage range from 600 V to about 2 kV. Below to 600 V (as is shown in Fig.1.7) is normally a domain of Silicon devices. Compared with SJ-MOSFETs (Super-Junction

MOSFETs) with a comparable voltage-class, the SiC MOSFETs present a lower ON-state resistance and thus reduced chip areas and losses. The second contribution is related to the study of ON-state resistance for a device with defects and traps distributions between the MOSFET inversion channel and the gate oxide. The period 2016-2018 has been crucial for SiC MOSFETs as well as for the whole SiC industry. Actually, SiC MOSFET manufacturers have improved device performance and reliability compared to the first generation of products. Nowadays, SiC MOSFET is gaining the confidence of numerous customers and has clearly begun to penetrate into different power applications. The outlook on the SiC scenario seem undoubtedly very promising and the market of power devices is still in progress. This market trend can be validated and certified by all the market analysis, and by the upward trend of the devices' production that is constantly growing year by year. In 2018 many manufacturers worldwide have improved the SiC wafer production, indeed the quality of production is greatly improved reducing significantly the production costs. This improvement has allowed the chipmakers to gain a new position in the market of semiconductors. The most reliable market analysis, and therefore also the most critical, have shown the forecasting data up to 2030. One of the most accredited market analysis companies in the field of chipmakers worldwide is Yole Développement, that has released recently their, more than positive, SiC outlook on the trend of market request up to 2030, Fig.1.8. This figure shows the projected SiC growth by the application area. The traditional markets in power supplies for SiC diodes and unipolar power devices are rapidly being supplemented by growth in (electric vehicle) EV on-board chargers and charging stations, and 2020 is expected to see growth of SiC transistors in power supplies, previously the domain of Silicon super-junction (SJ) MOSFETs.

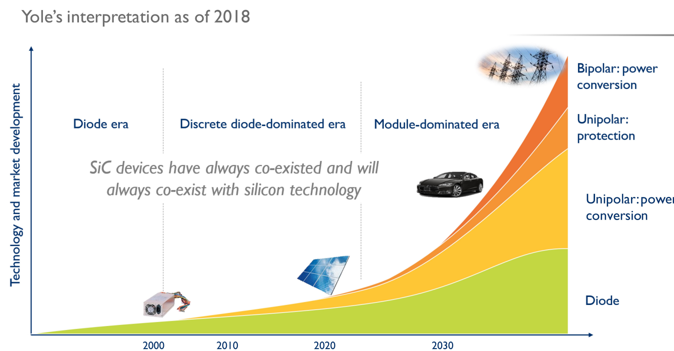

Fig. 1.8. Roadmap for SiC power industry drivers. Source: Yole Développement.

Part I

Silicon Carbide for Power MOSFETs

2

SILICON CARBIDE: the key-role material for a new era of power electronics

2.1 Silicon Carbide crystal structure and crystal defects

SILICON CARBIDE (SiC) is a tetrahedron crystal composed by four Carbon atoms with a Silicon atom in the centre (Fig. 2.1 [14]). Exists also a similar structure that has a rotation of 180° with respect to the first one. The atomic distance C-Si is 1.89 Å whereas that C-C is 3.08 Å. SiC exhibits a 2D polymorphism called polytypism. All polytypes have a hexagonal frame of SiC bi-layers. The hexagonal frame should be viewed as sheets of spheres with the same touching radius as is shown in Fig. 2.2 [14]. Thus, indicating with A, B, and C each of three layers, it is possible to construct polytypes simply by arranging the sheets in a specific repetitive order. Thus, the cubic polytype is 3C-SiC, which has the stacking sequence $\overbrace{ABCABC}$... while the hexagonal structure is 2H-SiC, which has the stacking sequence $\overbrace{ABAB}$.... The two more interesting polytypes for electronics are the 6H-SiC and 4H-SiC, which have the following stacking sequences $\overbrace{ABCACBABCACB}$... and $\overbrace{ABCBABCB}$..., respectively. The number in the notation of the resulting crystal structure determines the number of layers before the sequence repeats itself, and the letter determines the resulting structure of the crystal: C for cubic, H for hexagonal, and R for rhombohedral. All SiC polytypes show the same proportions of Silicon and Carbon atoms, but the stacking sequence between the planes are different, thus the electronic and optical properties are different.

In these structures is possible to find Nitrogen atoms who substituting a Carbon atom in its lattice, in each site positions indicate with "**k**" or "**h**" in 4H-SiC. The **k** site is a lattice site that displays cubic symmetry, whereas the **h** site has hexagonal symmetry. The Nitrogen chain tends to create different core binding energy. Thus, 4H-SiC presents two binding energies for the Nitrogen donor, which has consequences when designing devices. While 6H-SiC presents three energy levels for Nitrogen and 3C-SiC presents only one energy level. More complex polytypes such as rhombohe-

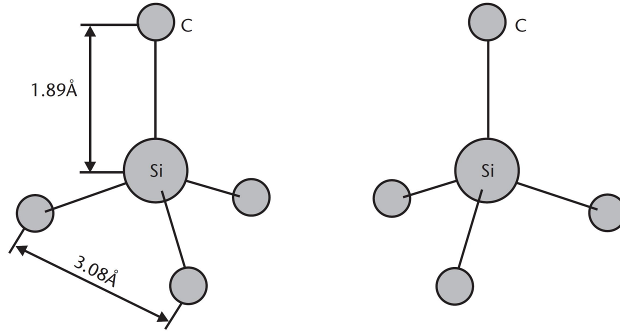

Fig. 2.1. The characteristic tetrahedron building block of all SiC crystals. Four Carbon atoms are covalently bonded with a Silicon atom in the centre. Two type exist. One is rotated 180° around the c-axis with respect to the other, as shown.

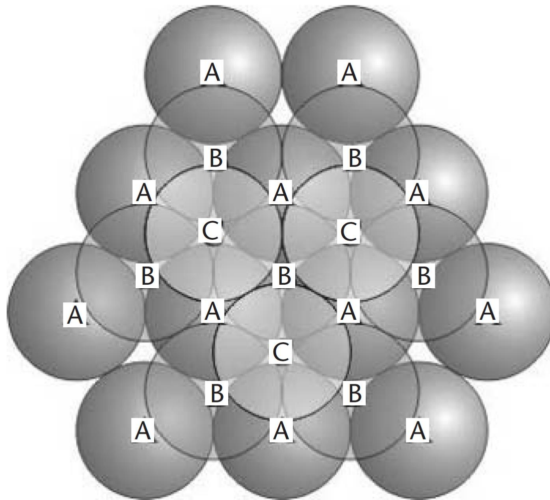

Fig. 2.2. Illustration of three close-packed planes of spheres. The first layer is a layer of "A" atoms, followed by a layer of atoms on a "B" position, with a layer of atoms on "C" positions on top of that. The resulting structure in this example is 3C-SiC.

dral (15R-SiC) has no less than five binding energies, although only four have been identified [15].

The stacking sequences of Silicon and Carbon atoms in the structures have these stacking sequences as is shown in Fig. 2.3 [16].

Since SiC has many polymorphs differing only in stacking sequence, it readily forms defects known as *stacking faults*, caused by mixing different stacking patterns during crystal growth. Since the step-flow epitaxy [17] mentioned above is associated with growth in the directions of the a, b, c axes, a consistent stacking sequence will be formed, allowing the growth of an epitaxial film containing few stacking faults. Figure 2.4 [16] shows the crystal orientation and c-axis off-angle relative to the orientation

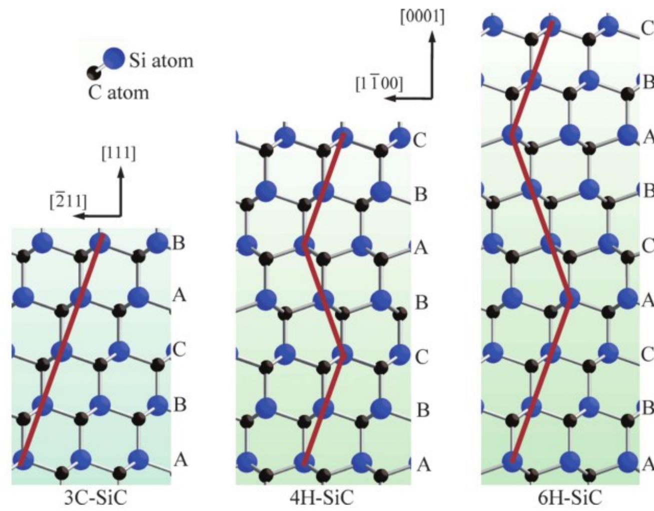

Fig. 2.3. Crystal structures of 3C-, 4H-, and 6H-SiC. Each has a different stacking sequence perpendicular to the close packed plane.

flat for the 4H-SiC wafer, currently the most recent development to enter actual device applications. These specifications are defined in the *SEMI standard* [18].

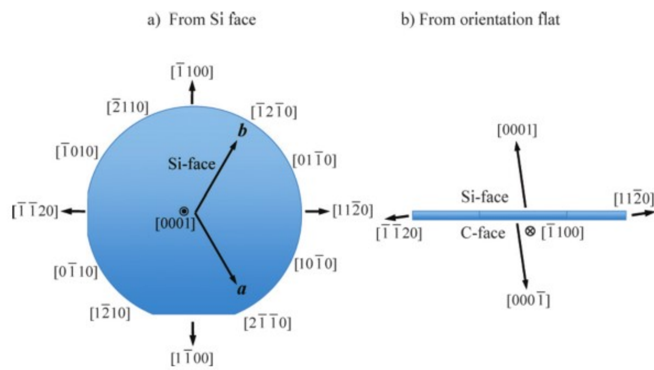

Fig. 2.4. Relationship between the orientation flat and crystallographic orientation of 4H-SiC wafer as defined in the SEMI standard. (a) Viewed from Si plane; (b) viewed from first orientation flat.

SiC crystals are produced under very high temperatures. The commercial wafers contain many crystal defects, as threading screw/edge dislocation, and basal plan dislocation [16]. These defects are called micropipes and are characterized by minute holes measuring over 10 μm in diameter at the dislocation centre. These dislocations influence device characteristics and performance. Anyway, recent advances in SiC technology have allowed producing 4-inch wafers containing practically no micropipes.

Most threading screw and edge dislocations in the substrate are known to be carried into the epitaxial film, while 95% or more of basal plane dislocations are converted to threading edge dislocations [19]. Certain threading screw dislocations also initiate stacking faults and large defects referred to as carrot defects [20].

Since numerous crystal defects including dislocations are inevitable with SiC wafers made by current technologies, fabrication of devices must assume that crystals have such defects. Thus, *the focal point is to declare the relationship between crystal defects and device characteristics*. However, ordinary crystal defect inspections based on etching probe, are destructive and cannot provide a direct correspondence between the presence of defects and device characteristics. Instead, X-ray measurements, are capable of evaluating the substrates and epitaxial films in a manner non-destructive. In Fig. 2.5 [16] are shown two areas where dislocations concentrate to form dark paths.

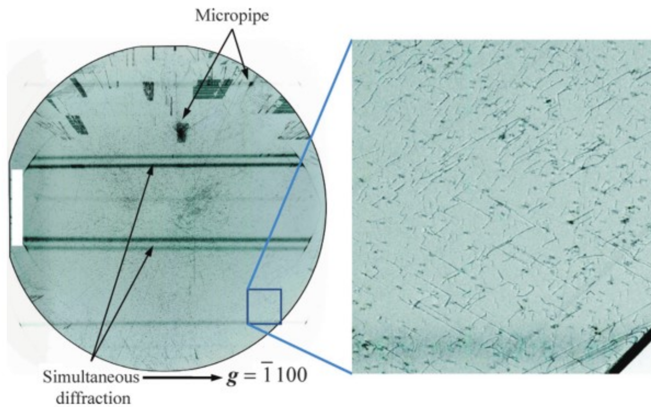

Fig. 2.5. Transmission topography images of 3-inch 4H-SiC wafer, which shows micropipes and dislocation.

X-ray topography allows to measure the positions and types of defects on the wafer and investigate the connection between device characteristics and crystal defects at the same position. The SiC polytypism phenomenon is very interesting for semiconductors for use in electronics because it is possible to extend the electronic property of SiC and thus to use the more appropriate polytypes. In Fig.2.6 [14] is shown that the sites are not equivalent in the polytypes 6H-SiC and 4H-SiC, instead, in Fig. 2.7 [14] are reported the different SiC structures for polytypes 2H, 3C, 4H and 6H.

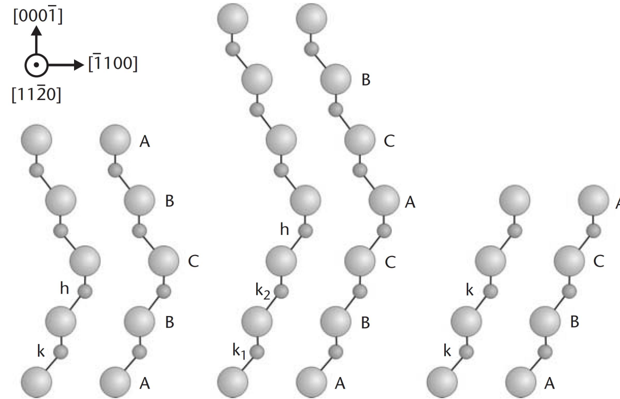

Fig. 2.6. The three most common polytypes in SiC viewed in the [1120] plane. From left to right, 4H-SiC, 6H-SiC, and 3C-SiC; **k** and **h** denote crystal symmetry points that are cubic and hexagonal, respectively.

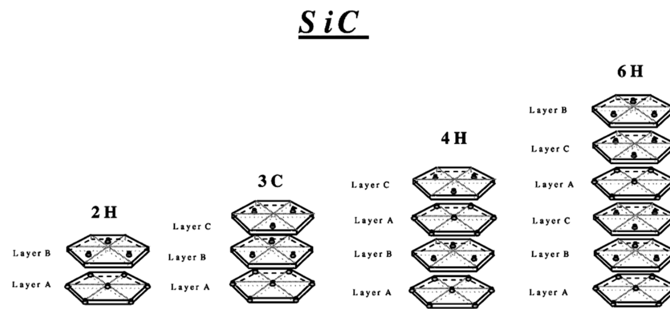

Fig. 2.7. Illustration of the stacking of successive layers of Si and C to represent the polytypes of SiC.

2.1.1 Notes on the construction of crystallographic indices

The hexagonal and rhombohedral lattices are based on the stacking of hexagonal planar lattices in sequence AAA .. (simple hexagonal) or ABCABC ... (rhombohedral). The hexagonal layers stand at the 'base' of the cell (axes **a** and **b**), while the axis **c** is perpendicular to it and parallel to the stacking direction. At least three different reference cells can be used, Fig.2.8 [21].

In Fig.2.8(a): primitive hexagonal cell, with axes **a** and **b** of equal length and with angle $\gamma = 120°$. This simple choice does not reveal the hexagonal symmetry of the lattice.

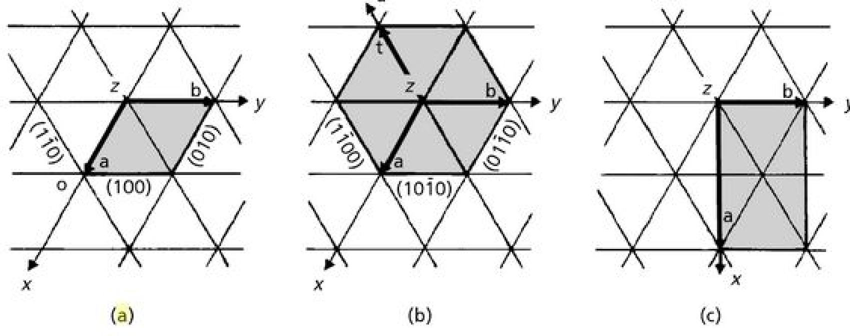

Fig. 2.8. Hexagonal net of the hexagonal P lattice showing (shaded) (a) primitive hexagonal unit cell with the traces of the six prism faces indexed *hkl*, (b) hexagonal (four-index) unit cell with the traces of the six prism faces indexed *hkil*, (c) orthohexagonal (B-base or C-centred) unit cell. The z-axis is out of the plane of the page.

For example, the side faces (equivalents for symmetry - form 100) of a straight hexagonal prism have *Miller* indices of the type: (100), (010), (110) (plus the centrosymmetric), making them look of different types and nature.

To overcome this apparent inconsistency, we introduce a not independent fourth axis, called "u", at 120° both from X and from Y. The four axes of *Miller-Bravais* "*x, y, u, z*" are defined by cell vectors **a, b, t, c**, and involve *Miller-Bravais* type indices (*hkil*). Thus, a primitive hexagonal cell with 4 axes Fig.2.8(b) is introduced with indices (*hkil*), where, by construction, $\mathbf{h}+\mathbf{k}+\mathbf{i}=\mathbf{0}$, or $\mathbf{i}=-(\mathbf{h}+\mathbf{k})$.

The third choice provides an ortho-hexagonal cell (ortho-rhombic with $a/b=\sqrt{3}$), which does not highlight the hexagonal symmetry of the lattice, but can be used when small distortions from the ideal make down the symmetry from true hexagonal to real orthorhombic. With the *Miller-Bravais* indexes (planes) and *Weber* symbols (axes), *Weiss*'s law becomes:

$$h\mathbf{U}+\ k\mathbf{V}+\ i\mathbf{T}+\ l\mathbf{W}=\mathbf{0}$$

2.2 Electronics properties

More than 200 SiC polytypes exist, but only the polytypes, 3C, 4H, and 6H are the most commonly available nowadays for the microelectronics industry. Each SiC polytype exhibits different electrical, optical, and thermal properties due to differences in the stacking sequence. Some of the SiC key electrical parameters for 3C, 4H, and 6H are listed in Table 2.1 [15, 22]. The significative electrical difference among these polytypes, clearly shows that it is essential to use only a single polytype (single crystalline) for electronic device fabrication. Indeed, some attempts to create stacks of

different polytypes did not have great success due to the low replicability of joining different atomic sheets without creating defects to the semiconductor structure.

Table 2.1. Electrical properties of Si, 6H-SiC, 4H-SiC, and 3C-SiC.

Property	**Si**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Energy Band Gap $[eV]$	1.10	2.96	3.26	2.36
Electron Affinity $[eV]$	4.05	3.45	3.70	4.00
Thermal Conductivity $[W/cm-K]$	1.50	3.0 - 4.0	3.0 - 3.8	3.0 - 4.0
Intrinsic Carrier Concentration $[cm^{-3}]$	10^{10}	10^{-5}	10^{-7}	10
Sat. Electron Drift Velocity $[10^7 cm/s]$	1.0	2.0	2.0	2.5
BDV Field $[MV/cm]$ @ $N = 10^{17}\ cm^{-3}$	0.30	$\|\|$ 3.00 $\perp$ 2.50	$\|\|$ 3.20 $\perp$ 1.00	1.80
Electron Mobility $[cm^2/Vs]$	1200	$\|\|$ 60 $\perp$ 400	800	750
Relative Dielectric Constant	11.90	9.70	10.00	9.60

Fabrication of devices is directly tied to the quality of SiC wafers and is hindered by the difficulty of surface doping. Therefore, is normally used the direct ion-implantation into the substrate [23]. Low defects, controlled doping, and dopant uniformity of both substrate and epilayers are crucial for device applications. In terms of the device type, low-resistivity substrates are vital for power devices as they reduce power losses due to the parasitic substrate and contact resistances. However, for devices and circuits operating at microwave frequencies, it is necessary to have semi-insulating substrates to achieve low dielectric losses and reduced device parasitics. Most current SiC-based electronic devices are fabricated using either 4H-SiC or 6H-SiC, where 4H-SiC has substantially higher carrier mobility, shallower dopant ionization energies, and low intrinsic carrier concentration Table 2.1. Thus, it is the most favourable polytype for high-power, high-frequency, and high-temperature device applications. In addition, 4H-SiC has an intrinsic advantage over 6H-SiC for vertical power device configurations because it does not exhibit electron mobility anisotropy while 6H-SiC does. Therefore, many SiC device fabrication efforts have shifted towards 4H-SiC as it has become more readily available. Figure 2.9 shows the physical material properties of Silicon and 4H-SiC [24].

Thanks to the high forbidden gap, SiC-based devices can operate at high temperatures. In addition, SiC has a high thermal conductivity, about three times greater than that of Silicon (4.9 $W/cm \cdot K$ for 4H-SiC, against 1.5 $W/cm \cdot K$ for Silicon). The thermal resistance is given by [23]:

$$R_{th,jc} = \frac{d}{\lambda A} \tag{2.1}$$

where λ is the thermal conductivity, d is the length of the device and A is the area of the section. It emerges that for the device in 4H-SiC it is over 3× lower, this means that the heat generated can be more easily transferred from the encapsulation case to the heat sinks, and therefore to the environment. Typically the maximum operating temperature is around 923 K, with a peak around 1173 K.

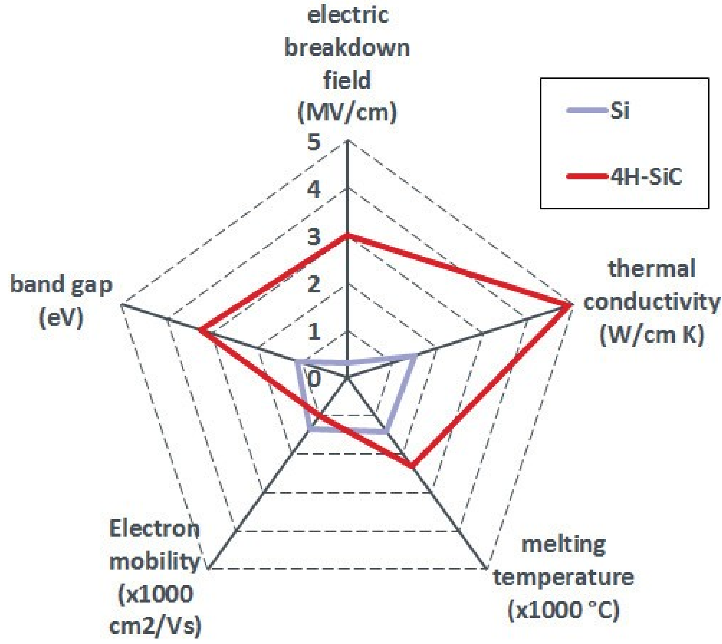

Fig. 2.9. Physical material properties of Si and SiC suitable for power electronic semiconductors.

2.3 Intrinsic carrier concentration

The intrinsic carrier concentration is determined by:

$$n_i = \sqrt{n \cdot p} = \sqrt{N_C \cdot N_V} \exp\left(-\frac{E_g}{2kT}\right) \tag{2.2}$$

Its value depends on the thermal generation of electron-hole pairs across the energy bandgap of a semiconductor. Where (E_G) is the bandgap energy, (N_C) and (N_V) represents the density of states respectively in the conduction and valence bands, and k is Boltzmann's constant (1.38 x 10^{-23} J/K) and T is the absolute temperature.

We remember that for Silicon, the intrinsic carrier concentration is given by:

$$n_i = 3.87 \times 10^{16} T^{3/2} \exp\left(-\frac{7.02 \times 10^3}{T}\right) \tag{2.3}$$

while for 4H-SiC, it is given by:

$$n_i = 1.70 \times 10^{16} T^{3/2} \exp\left(-\frac{2.08 \times 10^4}{T}\right) \tag{2.4}$$

Thanks to the equations 2.3 and 2.4 it is possible to rewrite the 2.2 as a function of temperature. The intrinsic carrier concentrations for Silicon and 4H-SiC are plotted in Figs. 2.10,2.11 [23].

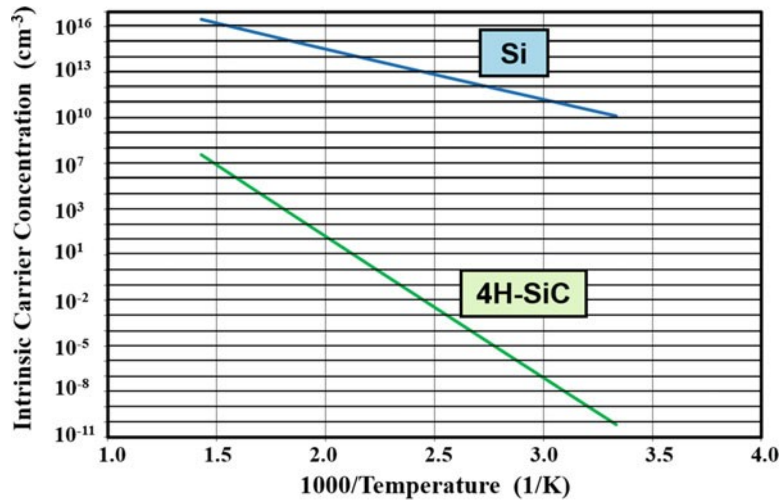

Fig. 2.10. Intrinsic carrier concentration in Silicon and 4H-SiC.

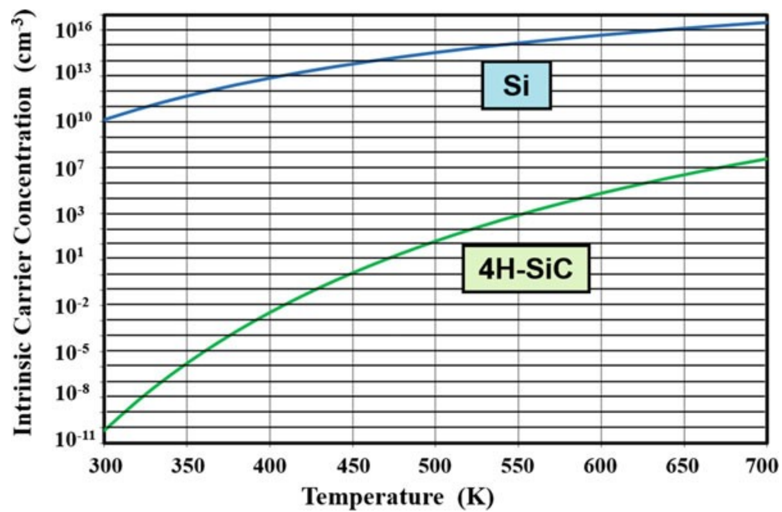

Fig. 2.11. Intrinsic carrier concentration in Silicon and 4H-SiC.

2.4 Bandgap narrowing

The reduction of the bandgap can be induced both by doping and by injection of carriers. Until models were available that adequately describe this phenomenon for 4H-SiC, the following formulation used for Silicon was used:

$$\Delta E_g = \alpha \cdot \left[\ln\left(\frac{N}{\beta}\right) + \sqrt{\left(\ln\frac{N}{\beta}\right)^2 + \gamma} \right] \tag{2.5}$$

With $\alpha = 0.009$, $\beta = 1 \times 10^{17}$, $\gamma = 0.5$.

However Lindefelt et al. [25] carried out theoretical studies on bandgap narrowing in 3C, 4H and 6H-SiC, relating it to the concentration of actually ionized dopants or to the concentration of carriers. Other details related to the simulation parameters are in chapter 4 and in Appendix B.

The energy band diagram for Silicon and SiC are shown in Fig. 2.11 [23]. The donor and acceptor levels are located at discrete positions within the bandgap and are separated from the conduction and valence band edges. The distance between the conduction and valence band edges is called the energy bandgap (E_G). In semiconductor highly doped the band structure is altered by three effects:

1. As the impurity density becomes large, the spacing between the individual impurity atoms becomes small. The interaction between adjacent impurity atoms leads to a splitting of the impurity levels into an impurity band as illustrated in Fig.2.12-b. This phenomenon is observed when the doping concentration exceeds $10^{18}\ cm^{-3}$.

2. The conduction and valence band edges no longer exhibit a parabolic shape. The statistical distribution of the dopant atoms in the lattice introduces point-by-point differences in local doping concentration and lattice potential leading to disorder. This results in the formation of band tails as illustrated in Fig. 2.12b by the dashed lines. This phenomenon is observed when the doping concentration approaches $10^{21}\ cm^{-3}$.

3. The interaction between the free carriers and more than one impurity atom leads to a modification of the density of states at the band edges.

This phenomenon is well known and is called "rigid bandgap narrowing". Bands impurity, band tails, and the rigid bandgap narrowing have significant carrier effects related to the reduction of space between the dopant atom in the semiconductor lattice. Moreover, the high concentration of majority carriers and the electrostatic

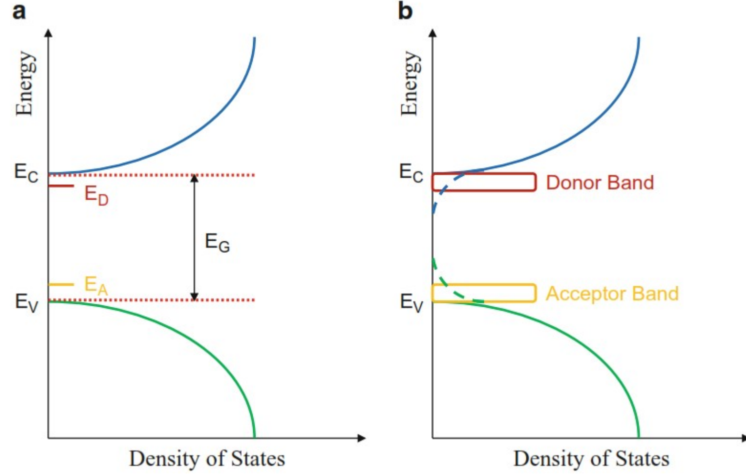

Fig. 2.12. Energy band diagrams at (**a**) low and (**b**) high doping concentrations.

interaction of the minority carriers tend to reduce the thermal energy required to create an electron-hole pair [23].

$$\Delta E_G = \frac{3q^2}{16\pi\varepsilon_S}\sqrt{\frac{q^2 N_D}{\varepsilon_S kT}} \tag{2.6}$$

The bandgap narrowing phenomenon has a heavy impact on the equilibrium concentrations of electrons and holes in a heavily doped semiconductor material. The eq. 2.7 can be still considered valid even for lightly doped semiconductors:

$$n \cdot p = n_{ie}^2 \tag{2.7}$$

Equation 2.8 allows to link the intrinsic concentration to the bandgap narrowing:

$$n_{ie}^2 = n_i^2 \exp\left(\frac{q\Delta E_G}{kT}\right) \tag{2.8}$$

where n_i is the intrinsic carrier concentration defined in eq. 2.2. We can see that ΔE_G is the reduction of the bandgap due to mainly the combined effects of band tailing and impurity band formation.

2.5 Built-in potential

The built-in potential (V_{bi}) determines the zero-bias depletion width which is an important device parameter for calculation of the ON-state resistance in power D-MOSFETs. The built-in voltage is given by:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A^- \cdot N_D^+}{n_i^2} \right) \tag{2.9}$$

where N_A^- and N_D^+ are the ionized impurity concentrations on the two sides of an abrupt P-N junction. For Silicon, there are small dopant ionization energy levels, thus result: $N_A^- \approx N_A$ and $N_D^+ \approx N_D$. Figure 2.13 [23] shows the built-in potential for Silicon and 4H-SiC. Baliga [23] reports that: $N_A^- \cdot N_D^+ = 1 \times 10^{19}\ cm^{-3} \times 1 \times 10^{16}\ cm^{-3} = 10^{35}\ cm^{-6}$. From Fig. 2.13 results that $V_{bi(4H-SiC)} > V_{bi(Si)}$ due to the smaller values for the intrinsic carrier concentration (n_i^2) in SiC.

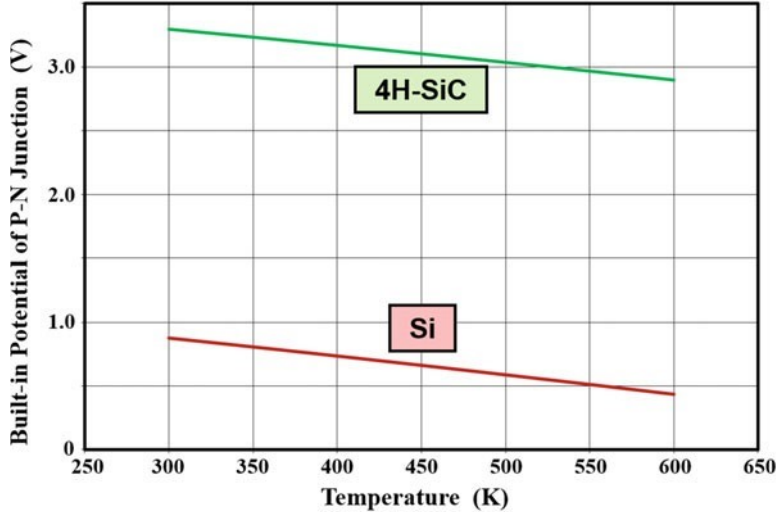

Fig. 2.13. Built-in potential for a P-N junction in Silicon and 4H-SiC.

2.6 Zero-bias depletion width

The Zero-Bias depletion widths (ZBDW) for Silicon and 4H-SiC are shown in Fig. 2.14 [23] as a function of the doping concentration. The ZBDW for SiC is about 2× larger than for Silicon at the same doping concentration. Results that, for a given breakdown voltage, $N_{SiC} \geq 100 \times N_{Si}$. As a consequence, the ZBDW(Si) << ZBDW(4H-SiC) for devices with the same breakdown voltage.

2.7 Impact ionization coefficients

The impact ionization coefficient[1] for holes/electrons (α_p) / (α_n) is defined as the number of electron-hole pairs created by a hole/electrons traversing 1-*cm* through

[1] Detailed information are in Appendix B.2.

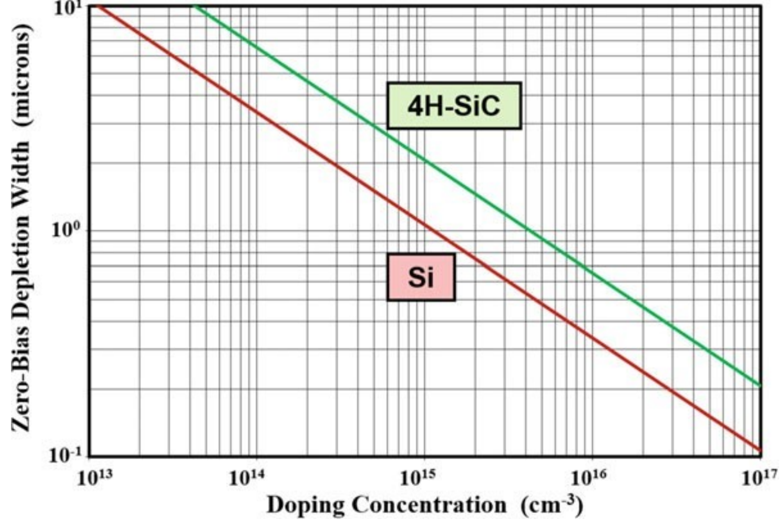

Fig. 2.14. Zero-bias depletion width in Silicon and 4H-SiC.

the depletion layer along the direction of the electric field. The impact ionization coefficients for semiconductors are given by *Chynoweth*'s law [23]:

$$\alpha = a \cdot \exp\left(-\frac{b}{E}\right) \tag{2.10}$$

where E is the electric field component in the direction of the current flow. The parameters a and b are constants that depend upon the semiconductor material and the temperature. From Baliga [23] results that the impact ionization coefficient parameters for holes and electrons in 4H-SiC are given by:

$$\begin{aligned} a_p\,(K)\,4H - SiC &= 8.07 \times 10^6; b_p\,(K)\,4H - SiC = 1.5 \times 10^7 \\ a_n\,(K)\,4H - SiC &= 3.13 \times 10^8; b_n\,(K)\,4H - SiC = 3.45 \times 10^7 \end{aligned} \tag{2.11}$$

Numerical simulations are often performed using the coefficients given in Eq. 2.11 because this provides agreement with measured breakdown voltages in 4H-SiC material containing defects. The impact ionization coefficients for 4H-SiC can be compared with those for Silicon in Fig. 2.15 [23].

In Silicon and SiC exist a marked relation of the ionization ($a_p(K)$, $a_n(K)$) coefficients with the electric field, E. This relationship has a negative impact on the breakdown voltage of power devices, because it results reduced by the presence of a high localized electric field within the structure. From Fig. 2.15 can be seen that in the case of the 4H-SiC it is necessary a higher electric field value than the Silicon in order to produce a significant generation of carriers by impact ionization. Consequently, the breakdown voltage for a 4H-SiC devices occurs when the electric field is in the range $E = 2 \div 3 \times 10^6\ V/cm$

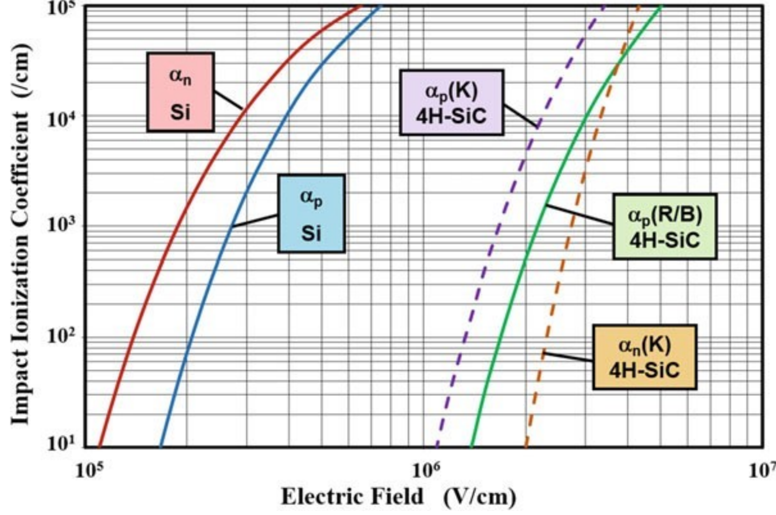

Fig. 2.15. Impact ionization coefficients for Silicon and 4H-SiC.

As a consequence, the breakdown in 4H-SiC devices occurs when the electric field is in the range of $2 \div 3 \times 10^6\ V/cm$; i.e. it results from an order of magnitude larger than that of Silicon. This means that an higher value of critical electric field $E_{cr}(4H-SiC) > E_{cr}(Si)$, and thus, results for breakdown that BV_{DS}(4H-SiC) $>$ BV_{DS}(Si). This increase the Baliga's figure of merit [2] [26].

2.8 Carrier mobility

The resistivity (ϱ) of a semiconductor region is given by:

$$\rho\,(T) = \frac{1}{(q \cdot \mu \cdot N)} \tag{2.12}$$

where μ is the mobility, which is a function of the carrier type (electrons or holes), (N) is the doping concentration, and (T) the lattice temperature. The mobility (μ) is defined as:

$$v_D = \mu \cdot E \tag{2.13}$$

The eq. 2.13 is valid for $E_{cr} < 10^4\ V/cm$. For power devices the velocity v_D does not increase more proportionally to the electric field, E. In this case the velocity tend to be a constant value known as the saturated drift velocity.

[2] $BFOM = \varepsilon \cdot \mu \cdot E_G^3$

where, ε is the dielectric constant of semiconductor; μ is the mobility; E_G is the bandgap semiconductor

2.8.1 Mobility: temperature dependence

In a semiconductor lightly doped the scattering of free carriers occurs meanly by interaction with the crystal lattice vibrations; these vibrations are due mainly to acoustical phonons or optical phonons. For $E_{cr} < 10^4\ V/cm$ the dominant scattering mechanism is due to acoustical phonons, instead for $E_C >> 10^4\ V/cm$ the dominant scattering mechanism is due to optical phonons [27]. This scattering can be formally treated in the same way as intra-valley scattering by optical phonons [28, 29].

For Silicon of high purity grade and lightly doped has been determined that acoustical phonon scattering is dominant at $T < 50\ K$, and the mobility varies as $T^{-3/2}$, where T is the absolute temperature. Moreover, at room temperature, intra-valley scattering begins to manifest, and the mobility for Silicon is given for electrons and holes respectively by: [23]:

$$\mu_n\,(Si) = 1360\left(\frac{T}{300}\right)^{-2.42} \tag{2.14}$$

$$\mu_p\,(Si) = 495\left(\frac{T}{300}\right)^{-2.20} \tag{2.15}$$

This variation of the mobility for electrons and holes in Silicon is shown in Fig. 2.16 [23]for the case of low doping concentrations ($N < 10^{15}\ cm^{-3}$) in the semiconductor.

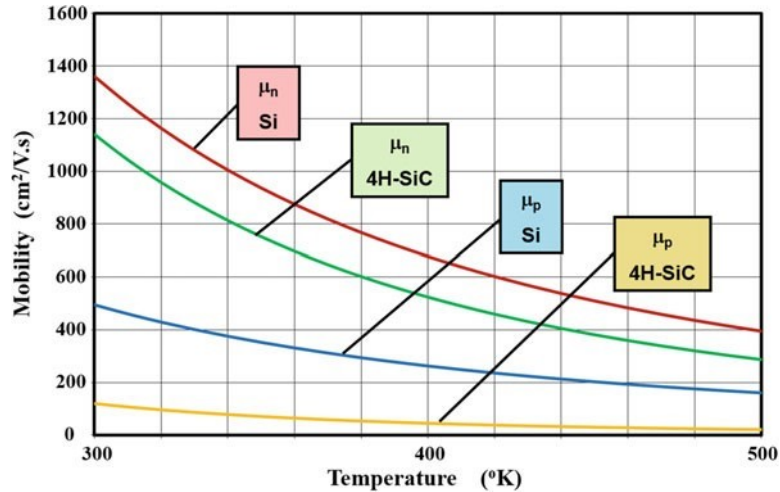

Fig. 2.16. Temperature dependence of the mobility for electrons and holes in Silicon and 4H-SiC.

There is a quick reduction of mobility with increasing temperature. For a 4H-SiC device, the mobility dependence from the temperature at low doping concentrations can be modelled by [23]:

$$\mu_n\,(4H-SiC) = 1140\left(\frac{T}{300}\right)^{-2.70} \tag{2.16}$$

$$\mu_p\,(4H-SiC) = 120\left(\frac{T}{300}\right)^{-3.4} \tag{2.17}$$

This variation is shown in Fig. 2.16. The electrons/holes mobility in 4H-SiC is important for modelling the n-type/p-type drift-regions/resistance-of-P-type regions of a unipolar devices.

2.8.2 Mobility: doping dependence

The semiconductor lattice contains ionized donor (acceptor atoms) which contributes to a reduction of mobility due to the additional *Coulomb* scattering of the free carriers. At low temperature, the impact of ionized impurity scattering is greatly extended because became less strong the link with lattice scattering. For semiconductors highly doped, the impact of ionized impurity scattering begins vastly and consequently, we assist in a reduction of mobility.

For Silicon [23]. At room temperature and for doping of $N = 10^{15}\ cm^{-3}$, the ionized impurity scattering has negligible effects, thus the mobility for electrons and holes can be considered independent of the doping concentration with a magnitude of 1360 and 495 $cm^2/V-s$ respectively, see equations 2.14, 2.15.

At room temperature and for doping of $N >> 10^{16}\ cm^{-3}$, the mobility of electrons can be modelled as eq. 2.18.

At room temperature and for doping of $N >> 10^{19}\ cm^{-3}$, the mobility for electrons tend to a constant value around 90 $cm^2/V \cdot s$. This behaviour is shown with red-line in Fig. 2.17 [23]. Similarly can be modelled the mobility of holes in Silicon room temperature as reported in eq. 2.19.

$$\mu_n\,(Si) = \frac{5.10\times10^{18} + 92N_D^{0.91}}{3.75\times10^{15} + N_D^{0.91}} \tag{2.18}$$

$$\mu_p\,(Si) = \frac{2.90\times10^{15} + 47.7N_A^{0.76}}{5.86\times10^{12} + N_A^{0.76}} \tag{2.19}$$

For Silicon Carbide [23].

The mobility of electrons and holes at room temperature as a function of the doping concentration can be modelled as eq. 2.20 and eq. 2.21:

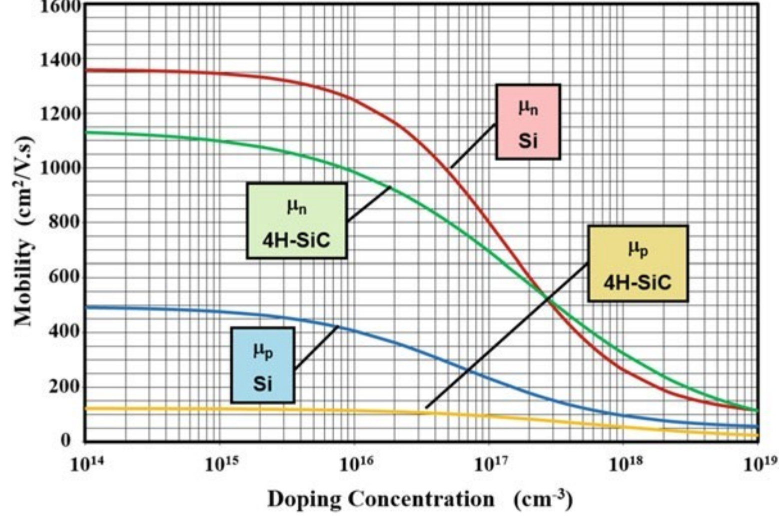

Fig. 2.17. Bulk mobility for electrons and holes in Silicon and 4H-SiC at room temperature.

$$\mu_n\,(4H - SiC) = \frac{4.05 \times 10^{13} + 20N_D^{0.61}}{3.55 \times 10^{10} + N_D^{0.61}} \tag{2.20}$$

$$\mu_p\,(4H - SiC) = \frac{4.05 \times 10^{13} + 10N_A^{0.65}}{3.3 \times 10^{11} + N_A^{0.65}} \tag{2.21}$$

These equations are plotted in Fig. 2.17 as a function of doping concentration.

2.8.3 Mobility: electric field dependence

The Silicon mobility for electrons and holes already seen in eq. 2.14 and 2.15, result independent from the magnitude of electric field if it is $E < 10^3\ V/cm$. In this case, the carriers velocity increase linearly with increasing electric field, but when $E = 10^3$ V/cm the electrons and holes velocity tend to increase sublinearly with increasing electric field, as shown in Fig. 2.18 [23], until it reaches a saturated value.

In Silicon lightly doped, the velocity for electrons and holes are dependent from the electric field using, as reported in equation 2.22, 2.23:

$$\nu_n = \frac{9.85 \times 10^6 E}{\left(1.04 \times 10^5 + E^{1.3}\right)^{0.77}} \tag{2.22}$$

$$\nu_p = \frac{8.91 \times 10^6 E}{\left(1.41 \times 10^5 + E^{1.2}\right)^{0.83}} \tag{2.23}$$

At $E < 10^3\ V/cm$, result that ν_n and ν_p tend to a constant value. But, when $E \geq 10^5$

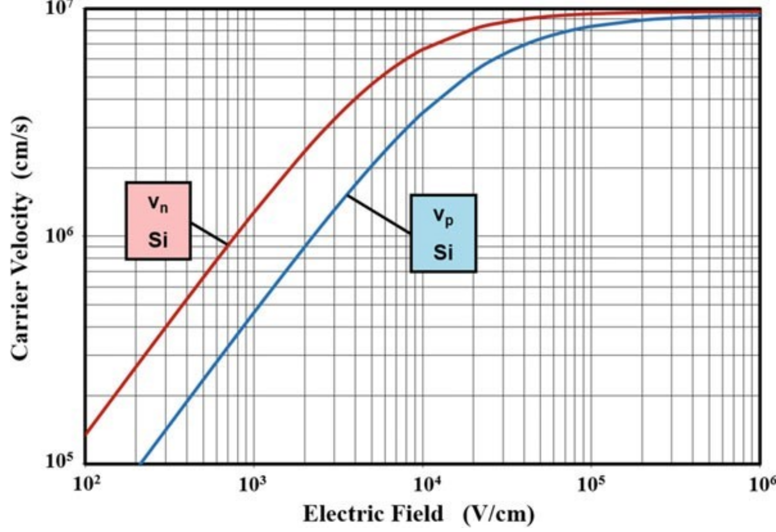

Fig. 2.18. Velocity for electrons and holes in Silicon.

V/cm, result that ν_n and ν_p are expressed in eq. 2.22 and 2.23 where the velocities are inversely proportional from the electric field.

For a high electric field, these equations can be approximated because the second term in the denominator becomes dominant. In this case, both the velocities tent to the "drift velocity saturation". Since the carriers mobility depends on the temperature of the lattice, it turns out that the "saturated drift velocities" is dependent on the temperature. For the case of electrons and holes transported along the crystallographic $<111>$ direction inside Silicon [23], [30]:

$$\nu_{sat,n} = 1.434 \times 10^9 \cdot \frac{1}{T^{0.87}} \tag{2.24}$$

$$\nu_{sat,p} = 1.624 \times 10^8 \cdot \frac{1}{T^{0.52}} \tag{2.25}$$

where T is the absolute temperature in K.

Considering that power devices usually operate in the thermal range of ($248\ K \div 423\ K$), the decrement of saturated drift velocity ($\nu_{sat,n}$ and $\nu_{sat,p}$) with temperature is shown in Fig. 2.19 [23].

For Silicon result that $\nu_{sat,n} >> \nu_{sat,p}$, but the difference becomes smaller as the temperature increases, see Fig. 2.19. For SiC lightly doped, result that $\nu_{sat,n}$ and $\nu_{sat,p}$ is given by eq. 2.26 and eq. 2.27, and are shown in Fig.2.20 [23]:

$$\nu_n\left(4H - SiC\right) = \frac{2.20 \times 10^7 E}{\left[2.27 \times 10^5 + \left(E^{1.25}\right)\right]^{0.80}} \tag{2.26}$$

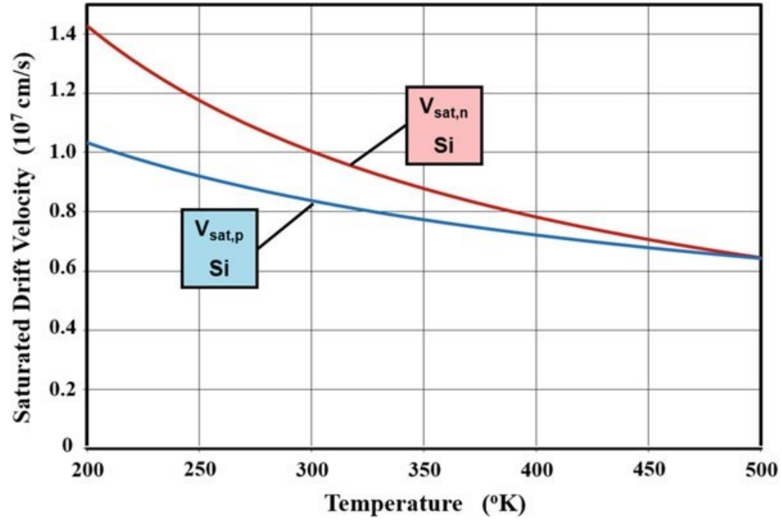

Fig. 2.19. Saturated drift velocity for electrons and holes in Silicon.

$$\nu_p\,(4H - SiC) = \frac{1.30 \times 10^7 E}{\left[1.16 \times 10^5 + (E^{1.20})\right]^{0.83}} \tag{2.27}$$

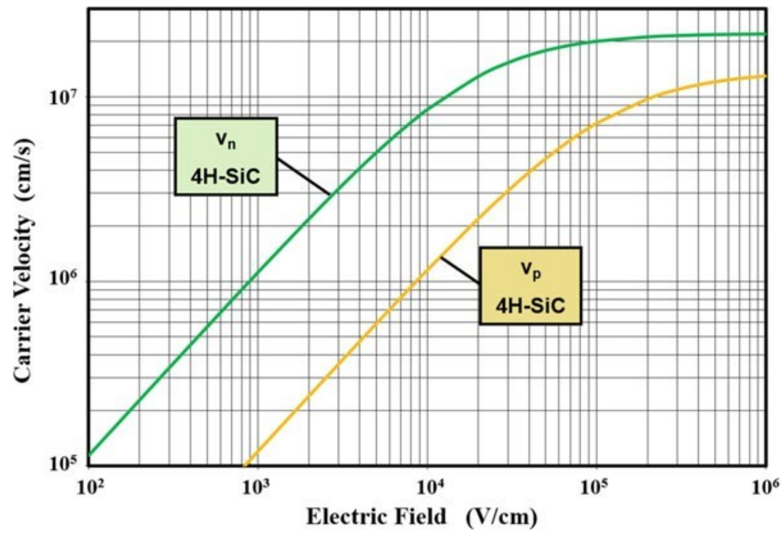

Fig. 2.20. Velocity for electrons and holes in 4H-SiC.

2.9 Avalanche breakdown

A power device can work with a maximum voltage and current, but beyond these values, it begins to work outside the safety area (SOA)[3] breaking the semiconductor junctions. Between source and drain, the structure of the MOSFET contains a parasitic (npn) bipolar transistor in parallel to the MOS channel, as shown in Fig. 2.21 [23]. This parasitic transistor would lead to many problems [31]:

- The blocking voltage tends to decrease due to this bipolar npn transistor.
- Applying a V_{DS} with a high dv/dt gradient, a displacement current is generated due to the charging of the depletion layer of the collector-base junction.

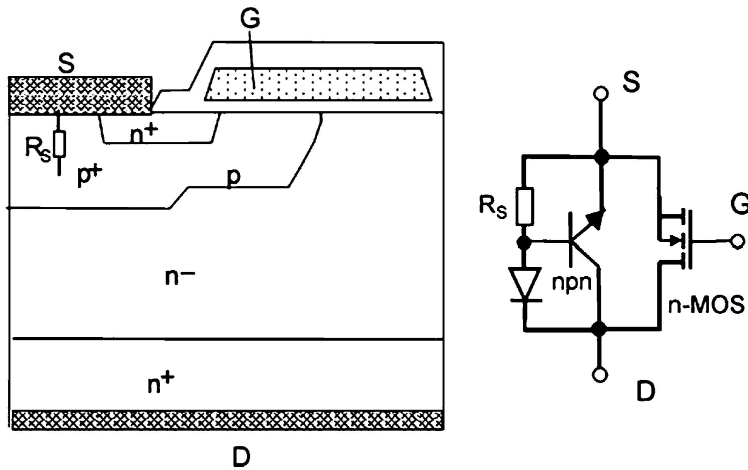

Fig. 2.21. MOSFET with its equivalent circuit, containing the parasitic npn-transistor and the parasitic diode.

This displacement current turn-ON the parasitic BJT and, thus, the MOSFET SOA will be limited by the second breakdown effect. Therefore, the base-emitter junction has to be short by a low resistance R_S between the source contact and the p-well region. This resistance can be reduced through an increasing the doping in this region with an additional p^+ ion-implantation.

The maximum voltage supported by a power device before it begins to flow a significant current is limited by the avalanche breakdown phenomenon. In these devices, the voltage is applied to the depletion region, where mobile carriers are accelerated by means of electric field until they become sufficiently energetic to create hole-electron pairs through collision with the lattice atoms. This allows beginning the ionization

[3] Safe Operating Area. Normally reported in the device datasheet.

process that determines the current flowing through the depletion region in the presence of a high electric field. The impact ionization coefficients already defined in eq. 2.11 and shown in Fig. 2.14 represents the number of electron-hole pairs created by a mobile carrier that flow through the depletion region for 10-mm in the same direction of electric field. [23]. Semiconductor devices are able to support high voltages in the OFF-state, without having a significant drain leakage current (I_{leak}). A structure of a typical power MOSFET is shown in Fig.2.25 [32]. The Silicon and SiC breakdown voltage as a function of the doping concentration is shown in Fig. 2.22, and we can see that the breakdown voltage decreases with increasing doping concentration.

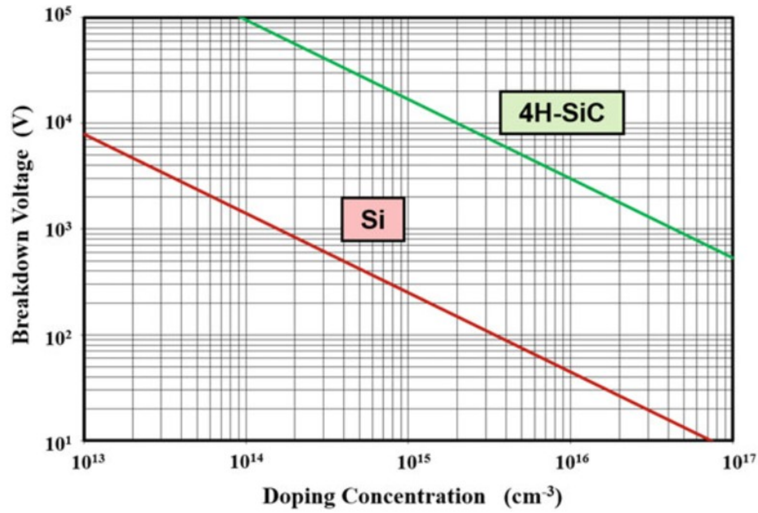

Fig. 2.22. Breakdown voltage for abrupt parallel-plane junctions in Si and 4H-SiC.

Of course, for 4H-SiC is possible to apply a higher voltage compared to Silicon for any given doping concentration. Instead, for a given breakdown voltage, it is possible to use a higher doping concentration in the drift region for 4H-SiC devices. The maximum depletion width reached the beginning of the breakdown is shown in Fig. 2.23 [23] for Silicon and 4H-SiC. We can observe that the thickness of the lightly doped side of the junction must be increased as the doping level is reduced in order to support larger voltages. This fact is normally used by designers for the dimensioning of the breakdown voltage value.

The critical electric fields (E_{cr}) for the breakdown in Silicon and SiC are given respectively by [23]:

$$E_{cr}\,(Si) = 3700 \times \sqrt[8]{N_D} \tag{2.28}$$

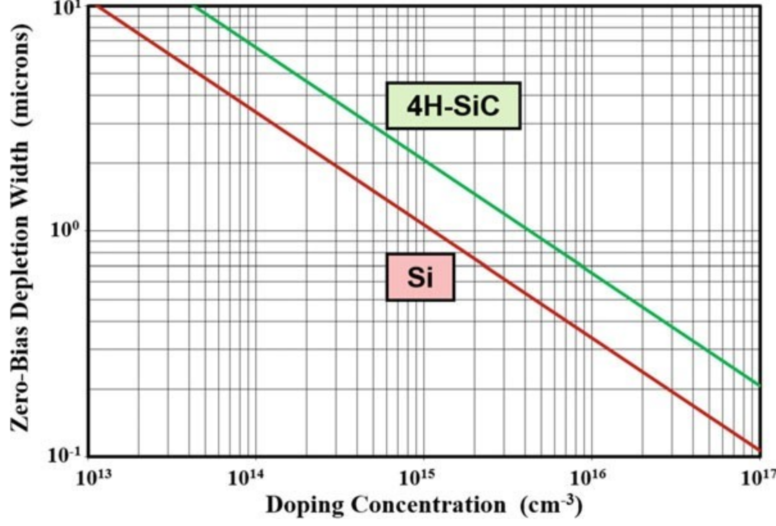

Fig. 2.23. Maximum depletion width at breakdown in Si and 4H-SiC.

$$E_{cr}\left(4H - SiC\right) = 33000 \times \sqrt[8]{N_D} \quad (2.29)$$

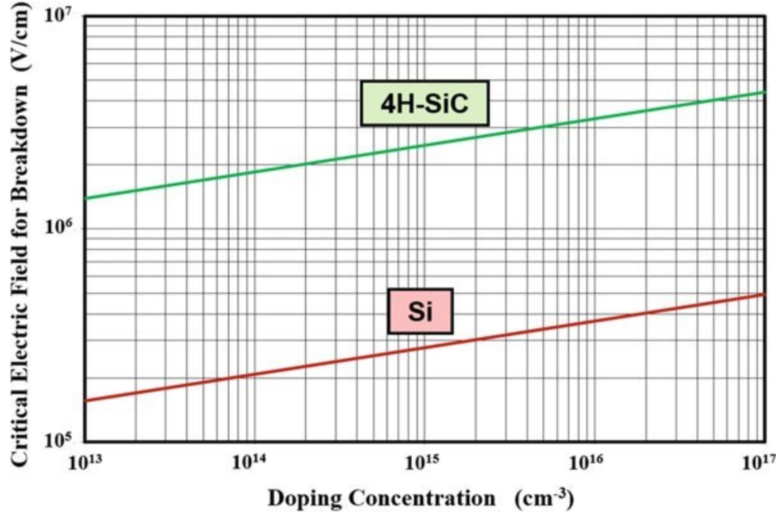

Fig. 2.24. Critical electric field for breakdown in Si and 4H-SiC.

The critical electric field (E_c) for 4H-SiC can be compared with that for Silicon in Fig. 2.24 [23]. From equations 2.28 and 2.29 we can see that:

$$E_{cr}\left(SiC, Si\right) \propto \sqrt[8]{N_D}$$

$$E_{cr}\left(SiC\right) \approx 9 \times E_{cr}\left(Si\right)$$

The critical electric field is a useful design parameter because it allows identifying when beginning the avalanche breakdown in power device structures. Avalanche

breakdown can be assumed to occur approximately when $E \approx E_{cr}$ within of any region of a power device. The precise breakdown value can be calculated analytically [23, 26]. Power devices have a strong dependence by temperature, indeed when carriers scattering is active, the mean free path for electrons and holes tend to become shorter with increasing temperature. Thus, the carriers gain less energy from the electric field, and consequently, the impact ionization coefficients for electrons and holes decrease with increasing temperature. In the case of Silicon, the avalanche breakdown voltage tend to increase at the rate of 0.454 $V/^{\circ}C$ which corresponds to about 20% increase from 300 to 500 K [23].

Designers have to take into account that, the doping of N-drift layer (N_{drift}) is carefully chosen to obtain the desired breakdown voltage (BV_{DS}). The thickness of the N-drift layer has to be accurately evaluated, because it contains the full depletion layer width (W_{drift}) corresponding to the BV_{DS} of the designed device. Of course, the doping and thickness of W_{drift} layer have to be designed leaving a thickness of security to avoid that the depletion region reaching the N^{+} substrate region as it causes punch through. However, from Fig.2.25 [32] result that:

$$V_{BD} = \frac{\varepsilon_S \cdot E_{cr}^2}{2q \cdot N_{drift}} \tag{2.30}$$

$$W_m = \sqrt{\frac{2\varepsilon_S \cdot V_{BD}}{q \cdot N_{drift}}} \tag{2.31}$$

For 4H-SiC, Equations 2.30 and 2.31 could be written as a function of N_{drift} only as presented in equations 2.32 and 2.33 [32]:

$$V_{BD}\,(V) = 3.0 \times 10^{15} \cdot \frac{1}{\sqrt[4]{N_{drift}^3}} \tag{2.32}$$

$$W_{drift}\,(\mu m) = 1.82 \times 10^{11} \cdot \frac{1}{\sqrt[8]{N_{drift}^7}} \tag{2.33}$$

The ratios are [33]:

$$\frac{V_{BD}^{SiC}}{V_{BD}^{Si}} = 100\frac{N_{drift}^{Si}}{N_{drift}^{SiC}} \tag{2.34}$$

$$\frac{W_D^{Si}}{W_D^{SiC}} = \frac{E_{BD}^{SiC}}{E_{BD}^{Si}} = 11 \tag{2.35}$$

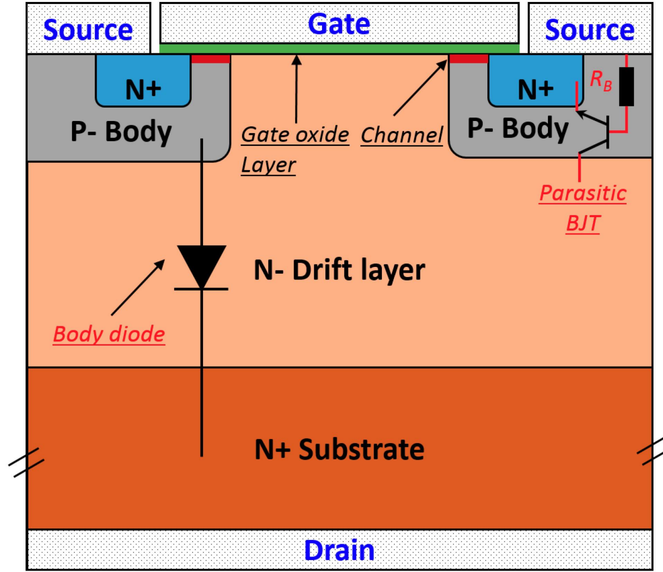

Fig. 2.25. Structure of an n-channel power MOSFET: with highlighted the parasitic BJT and the Body diode.

At the same doping concentration of the drift region N_{drift}, the avalanche breakdown voltage of the SiC-MOSFET is 100 times higher than that of the Si-MOSFET. At the same breakdown voltage V_{BD}, the doping concentration of the drift region N_{drift} of the SiC-MOSFET can be 100 times higher and the drift region thickness W_{drift} can be 11 times lower than those of the Si-MOSFET. The avalanche breakdown voltage V_{DSS} decreases as the junction temperature T_J decreases. The minimum breakdown voltage $V_{DSS(min)}$ occurs at the lowest junction temperature $T_{J,min}$. At lower temperatures, the average distance between collisions, called the mean free path of charge carriers, is longer because the amplitude of the atom oscillations is lower. Therefore, the impact ionization rate is higher, yielding a lower avalanche breakdown voltage V_{BD}. The thermal coefficient of the breakdown voltage is $(\Delta V_{DSS}/V_{DSS})/\Delta T = 10^{-3}/^{\circ}C$. The breakdown voltage $V_{BD} = V_{DSS}$ is measured at $V_{GS} = 0\ V$ and $I_{DS} = 0.25\ mA$ [33]. The breakdown voltage V_{DSS} depends on the defects in the semiconductor structure, especially the defects on the surface and in the curved areas, where the electric field is the strongest. Since it is impossible to predict accurately the distribution of defects, the calculations of the breakdown voltage are uncertain. Manufactures' datasheets for power MOSFETs usually give lower values of the breakdown voltage than the actual ones.

2.9.1 Blocking voltage

In vertical power MOSFETs, each region has to be defined mainly for its doping and thickness. Thus, the N-drift region plays a twice role, indeed, its thickness is carefully designed to support the maximum blocking voltage. Instead, its doping is tied to the maximum current that flows through the structure.

The maximum doping concentration of the P-base region (N_{P-base}) is chosen to achieve the desired threshold voltage (V_{TH}).

For the designed MOSFET with a $BV_{DS} < 150\ V$ and reported in chapter 4, result that the doping $N_{P-base} \approx N_{drift}$. This is a positive thing for the R_{ON} reduction. However, designers prefer to make the P-base region with a depth smaller to reduce the channel length (L_{ch}) and consequently to reduce the relative channel resistance (R_{ch}). However, the design of the P-base region must take into account reduction of the BV_{DS} due to the depletion region in the P-base region that can move towards to the source region, N^+.

An important parameter obtained from the electrical characteristics of the MOSFET is the ON-state resistance, which must have the lowest value possible, because in this way it allows dissipating less energy during operation, and also allows switching to higher frequencies

2.9.2 Safe operating area (SOA)

The SOA of a power device defines the maximum allowed V_{DS} together with the maximum allowed I_D at which the device can be operated without destructive failure. In Fig.2.26, the typical SOA of a power MOSFET is depicted using logarithmic scales for both V_{DS} and I_{DS}. The limits visible in Fig.2.26 define the border of the biasing area where the device can reliably work without experiencing a failure. In the following, a short description of those limits is given:

- The region A is intrinsically defined by the power MOSFET operation. In this region device operation is limited by the V_{DS} drop, which is defined by its R_{ON} at low-current operations (namely the R_{ON} in the triode region).
- The region B is a consequence of the maximum drain current I_{DS} allowed for the device. This limit is typically related to the maximum current that device source bond wires can sustain without fusing.
- The region C determines the maximum V_{DS} blocking voltage that the device can handle without experiencing avalanche failures.

- The region D is mainly determined by the maximum allowed junction temperature T_{jmax}, which is defined by device biasing conditions and its junction to case thermal impedance Z_{thj-c} by means of:

$$T_j - T_c = Z_{j-c}^{th} \cdot V_{DS} I_{DS} \tag{2.36}$$

where T_c is the case (package) temperature which is commonly equal to the ambient temperature. In this region, the range of maximum allowed V_{DS} and I_{DS} is eventually larger in pulse operation. In fact, in this case, a reduced duty cycle implies a smaller effective power dissipation compared to the one obtained in the DC operation. Therefore, this SOA limit enlarges as the pulse width is reduced. The definition of the SOA limits depicted in Figure 2.26 is based on just purely thermal considerations and neglects possible further limitations related to electro-thermal interactions which commonly take place within a power MOSFET.

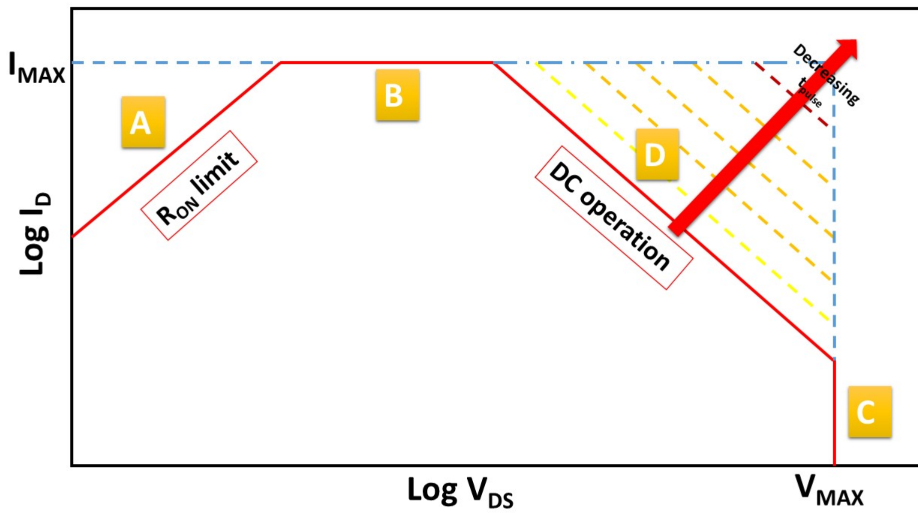

Fig. 2.26. SOA of a power MOSFET in DC and pulsed operation.

2.10 Recombination lifetime

In a semiconductor in thermal equilibrium conditions, there is a continuous dynamic balance between the generation and recombination of electron-hole pairs. At non-thermal-equilibrium can create an excess of carriers, but when the semiconductor reach again the equilibrium happens that the excess of generating carrier begin to decays, thus allowing to the semiconductor to return at thermal equilibrium. The rate of recovery depends upon the minority carrier lifetime. The recovery in equilibrium conditions occurs due to several simultaneous recombination processes:

a. An electron dropping directly from the conduction band into the valence band.

b. An electron dropping from the conduction band. And a hole dropping from the valence band into a recombination level located within the energy bandgap.

c. Electrons from the conduction band and holes from the valence band dropping into surface traps.

The transitions of these recombination processes are shown in Fig. 2.27 [23]. During the recombination processes, the carriers energy is dissipated with one of the following mechanisms:

1. (**Radiative Recombination**): emission of a photons.
2. (**Multi-Phonon Recombination**): emission of phonons.
3. (**Auger Recombination**): transmission of the energy to a third particle, hole or electron. The Auger Recombination process becomes of importance in determination of the minority carrier lifetime in very heavily doped regions.

In Appendix B.3 are reported the parameters of physical models used in the numerical simulator introduced in the next chapter.

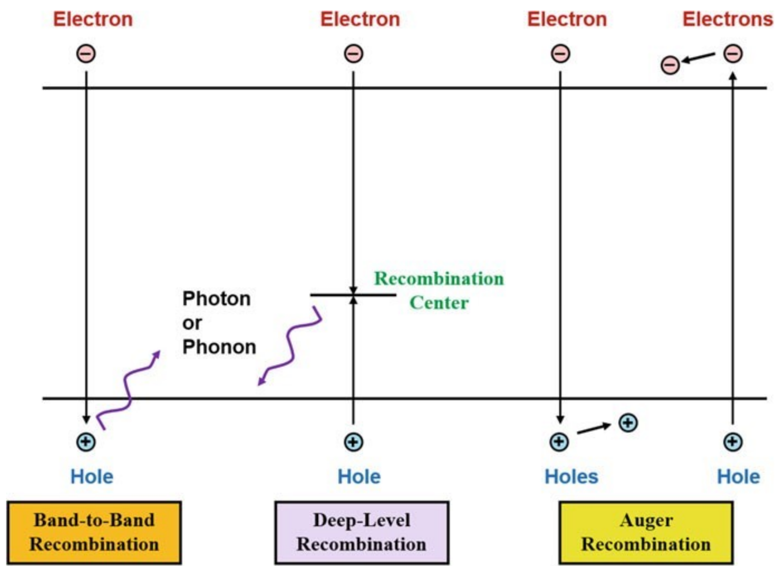

Fig. 2.27. Recombination processes in a semiconductor.

3

POWER MOSFETs PHYSICAL MODEL

3.1 Introduction

Silvaco ATLAS® is a 2D and 3D device simulator that performs DC, AC, and transient analysis for Silicon, binary, ternary, and quaternary material-based devices. ATLAS enables the characterization and optimization of semiconductor devices for a wide range of technologies. Device simulation helps researches understand and depict the physical processes in a device and to make reliable predictions of the behaviour of the next device generation. Two-dimensional device simulations with properly selected calibrated models and a very well-defined appropriate mesh structure are very useful for predictive parametric analysis of novel device structures. The 2D and 3D modelling and simulation processes help users obtain a better understanding of the properties and behaviour of new and current devices. Simulating SiC devices is more challenging compared to Silicon. Indeed, very low intrinsic concentration combined with high doping values is usually detrimental to convergence. This problem can be handled thanks to the different composition and discretization of mesh, indeed, the mesh-layer influence results and CPU-time. Simulation code is written with the Silvaco DevEdit® editor. It can be used to generate a new mesh on an existing structure and can be used to create or modify a device. These devices can then be used by 2D and 3D simulators. A limitation of device simulators prior to DevEdit® was inadequate or poor structure meshes. A mesh containing too many obtuse triangles or an insufficient number of triangles (a grid too coarse) may provide an inaccurate result or no result at all. A mesh containing too many triangles (too fine a grid) can result in excessive simulator processing time. Since the time most simulators use grows geometrically with the number of triangles (or grid points), it is critical to keep the number of triangles down to a reasonable number. Specifying a good mesh is a crucial issue in device simulation. There is a trade-off between the requirements of accuracy and numerical efficiency. Accuracy requires a fine mesh that

resolves the structure in solutions. Numerical efficiency is greater when fewer points are used. The critical areas to resolve are difficult to generalize since they depend on the technology, transport phenomena, and bias conditions. Typical areas that require fine mesh include:

- High electric fields at the drain/channel junction in MOSFETs
- Transverse electric field beneath the MOSFET gate
- Areas of high impact ionization

The CPU time required to obtain a solution is typically in proportion to Na, where N is the number of nodes and "a" varies from 2 to 3, depending on the complexity of the problem. Therefore, it is most efficient to allocate a fine grid only in critical areas and a coarser grid elsewhere. Poor meshes can lead to inaccurate answers, poor convergence times or even lack of convergence, leaving you without a solution.

3.2 Basic semiconductor equations

This physical model consists of a set fundamental equations set derived from Maxwell's laws. They are mainly the equations of the:

1. *Poisson*'s equation
2. Transport equation
3. Continuity equations
4. Carrier densities
5. Electrostatic potential

The *Poisson*'s equation describes variations of electrostatic potential of local charge densities. The continuity equations describe how the electron and hole densities evolve as a result of transport, generation and recombination processes.

The *Poisson*'s equation relates the electrostatic potential of a space charge density, is given by eq. 3.1:

$$\nabla \cdot (\varepsilon \nabla \psi) = -\rho \tag{3.1}$$

where ψ is the electrostatic potential, ε is the local permittivity, and ρ is the local space charge density. Silvaco ATLAS choice as reference potential the "intrinsic *Fermi* potential" ψ_i. Moreover, this simulator shapes the local space charge density in the sum of all fixed and mobile charges, including holes, electrons and ionized impurities.

The electric field (**E**) is given by:

$$\mathbf{E} = -\nabla \psi \tag{3.2}$$

The continuity equations for electrons and holes are defined respectively by equations 3.3 and 3.4:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \mathbf{J}_n + G_n - R_n \tag{3.3}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot \mathbf{J}_p + G_p - R_p \tag{3.4}$$

where n and p are the electron and hole concentration, $\mathbf{J}_n$ and $\mathbf{J}_p$ are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the electric charge. The current density equations $\mathbf{J}_n$ and $\mathbf{J}_p$, are expressed in terms of the quasi-*Fermi* levels ϕ_n and ϕ_p

$$\mathbf{J}_n = -q\mu_n n \nabla \phi_n \tag{3.5}$$

$$\mathbf{J}_p = -q\mu_p p \nabla \phi_p \tag{3.6}$$

where μ_n and μ_p are the electron and hole mobilities.

The carrier concentrations are given by:

$$n = n_{ie} \exp\left[\frac{q(\psi - \phi_n)}{K \cdot T_L}\right] \tag{3.7}$$

$$p = n_{ie} \exp\left[\frac{-q(\psi - \phi_p)}{K \cdot T_L}\right] \tag{3.8}$$

where n_{ie} is the effective intrinsic concentration and T_L is the lattice temperature.

3.3 Silicon carbide unipolar devices: MOSFETs

SiC power MOSFETs can operate at the higher switching frequency and operating temperatures compared with conventional Silicon MOSFETs. It has been expected to be the next-generation switching device to replace conventional Silicon power devices in many applications. The first SiC power MOSFET was born in 1994, it had the form of a vertical trench gate structure (UMOSFET). I this new structure the breakdown voltage was limited by the high electric field inside the gate oxide and in the corner of the trench. To overcome this obstacle was proposed a SiC planar gate MOSFET with a p-base formed by a double implantation MOS process (DMOSFET). Figure 3.1 [1]

shows the schematic diagram of the structure of the typical UMOSFET (UMOS) and DMOSFET (DMOS). In Fig. 3.1-a is shown the V-MOSFET, in which the gate has a V-shaped groove, this solution presents the problem to concentrate a high electric field at the tip of the V-shaped groove, in order to create a current crowding that degrades the device performance. The solution to this problem was the innovative structure of Fig. 3.1-b (U-MOSFET), which is similar to the V-MOSFET, but was developed to reduce the ON-state resistance thanks to the elimination of JFET component within the structure. In Fig. 3.1-c is presented the D-MOSFET which uses the double diffusion process that allows producing devices with very short channels interdependently from the lithographic mask process. Power MOSFETs have different structures:

- In a planar structure, the current and breakdown voltage ratings are both functions of the channel dimensions (respectively width and length of the channel), resulting not optimized for Silicon device".
- In a vertical structure (VDMOSFET), the current rating is a function of the channel width, while the breakdown voltage rating is a function of the doping and thickness of the epilayer. This is the motivation of why this structure can sustain high blocking voltage and high current.

The main advantage of D-MOSFET is related to the avoidance to get a high electric field in corners. For this structure, the doping level and thickness of the N_{drift} region are important parameters that determine the drain blocking voltage capability.

On the other hand, there is a parasitic bipolar N-P-N device in the power MOSFET structures, as already seen in Fig.2.25. To prevent that this bipolar transistor start-ON during power MOSFET operation, the P-base and N^+ source (emitter) are shorted ($V_{BE} = 0\ V$).

Unfortunately, the 4H-SiC MOSFETs presents a very low inversion channel electron mobility, and consequently, it has slow dynamic performance. Electron mobility in the channel has been proved to be low when measured on p-regions after the implantation process that damage the crystalline structure. SiC has a higher density of dangling bonds at the SiO_2/SiC interface due to its higher density of atoms (per unit area) compared with Silicon. Therefore, various intrinsic defects not related to dopants or impurities are present at the SiO_2/SiC interface.

These defects appeared in the energy gap of SiC as traps for electrons leading to the low channel mobility in 4H-SiC.

To try to increment the channel mobility, improving performance at high temperature, and device reliability, it is important to reduce the density of states of at

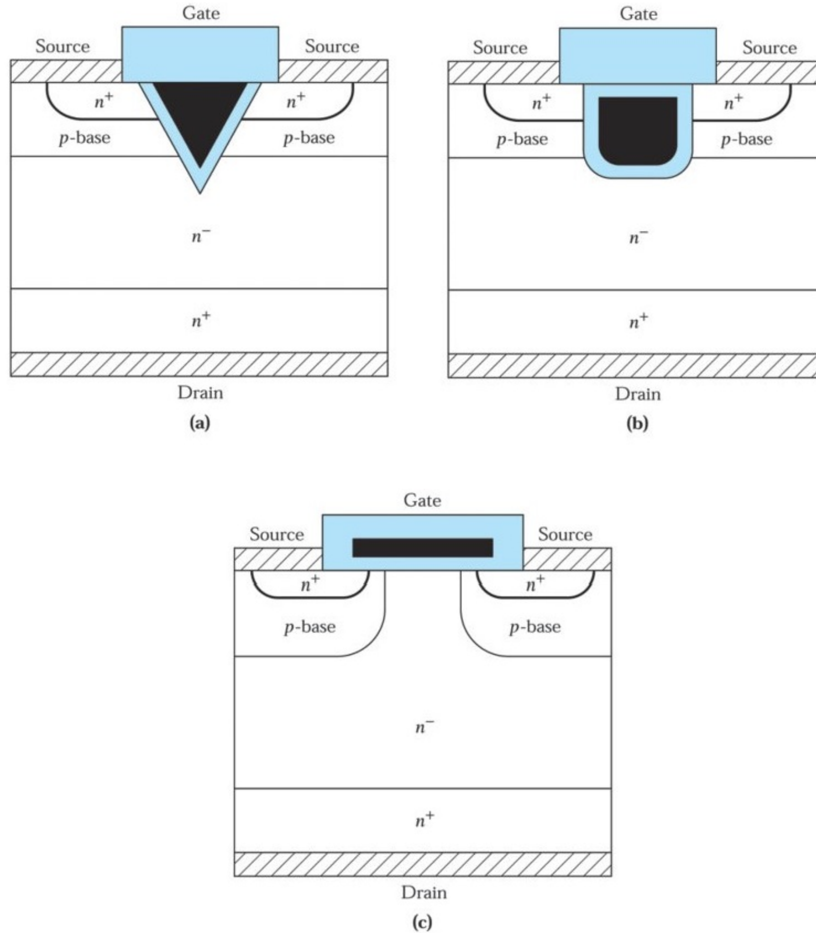

Fig. 3.1. Schematic diagram of SiC (a) V-shaped (VMOS), (b) U-shaped (c)UMOS), and double-diffused MOS (DMOS) power device structures.

the SiO_2/SiC interface. Nowadays, has been adopted two main solutions, the first-one use Nitrogen during the post-oxidation annealing and the second-one consider to use specific crystal faces for the formation of channel MOSFET. Thanks to the new technological processes the mobility in the channel have greatly improved, but the interface states of density are still of two magnitude orders higher than devices fabricated by using the Silicon MOS technology.

The "high-k gate dielectric" technology contrast effectively the problem of gate leakage. Moreover, its higher dielectric breakdown field improves the reliability and channel carrier mobility of the device. The gate oxide SiO_2 allow to MOS devices to present an high-input-impedance, this feature is very interesting in power-device applications. Thus, this technology allows to obtain devices with a very low gate leakage current, this is important also because the device does not require an extra driving hardware at its input. In circuits for fast switching, it is preferable to use

MOSFETs because they are faster than power bipolar device. This last point can be better understood because the unipolar characteristics of MOSFET do not involve storage or recombination of minority carriers during the turn-OFF phase. For these MOSFETs devices, obtaining a high current is tied to the design of a channel with a large width. Power MOSFETs, normally present thicker oxides, deeper junctions, and have longer channel lengths. These geometrical and physical characteristics tend to limit the device performance such as the trans-conductance (g_m) and switching speed (f_T).

3.4 Ideal specific Drift Region

Power MOSFETs performance is limited by internal resistance. Thus, designers have to set the minimum value for internal resistance compatibly with the blocking voltage which also depends on the internal resistance. In the ideal case, is considered the structure that supports the blocking voltage without any degradation effect due to the edge contact and to the local enhanced electric field inside the regions of the structure. All the single resistances of device regions, apart from the drift region (R_{drift}), are considered to be parasitic resistances that have to be reduced as much as possible to the minimal values. Thus, the thickness and resistance of the drift region are important design parameters. Now, proceed with the ideal ON-state resistance dimensioning; begin to consider the distribution of electric field in the case of an abrupt parallel-plane junction, Fig 3.2 [23]. The resistance of the ideal drift region can then be related to the blocking voltage, and the basic properties of the semiconductor material, as doping concentration and thickness.

The solution of *Poisson*'s equation leads to a triangular electric field distribution, as shown in Fig. 3.2, within a uniformly doped drift region with a field profile slope being determined by the doping concentration. The maximum voltage that can be supported by the drift region is determined by the maximum electric field (E_{max}) which must not reach the value of the critical electric field (E_{cr}) for the breakdown of semiconductor material. The critical electric field for breakdown condition and the doping concentration then determine the maximum depletion width (W_D). The specific resistance (per unit area) of the ideal drift region is given by [23]:

$$R_{ON,sp} = \frac{4BV_{PP}^2}{\varepsilon_S \mu_n E_{cr}^3} \tag{3.9}$$

where BV_{PP} is the breakdown voltage parallel to the plane, ε_S is the dielectric constant for the semiconductor, μ_n is the electron mobility, and E_{cr} is the critical

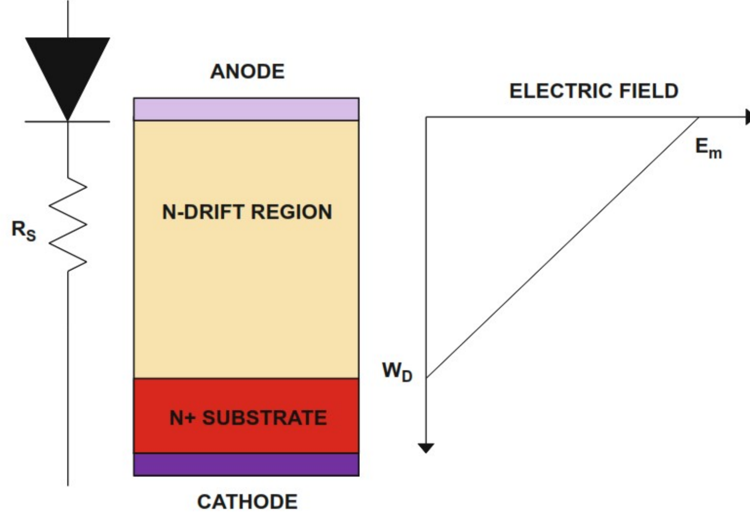

Fig. 3.2. The ideal drift region and its electric field distribution.

electric field for breakdown. Instead, the depletion width under breakdown conditions is given by:

$$W_D = \frac{2BV}{E_{cr}} \tag{3.10}$$

where BV is the desired breakdown voltage. The "required" doping concentration in the drift region to fix the breakdown voltage is given by:

$$N_D = \frac{\varepsilon_S E_{cr}^2}{2qBV} \tag{3.11}$$

Combining these equations, the specific resistance of drift region is given by [23]:

$$R_{ON,sp} = \frac{W_D}{q\mu_n N_D} \tag{3.12}$$

Instead, the ideal resistance of drift region is given by [23]:

$$R_{ON,ideal} = \frac{4BV^2}{\varepsilon_S \mu E_{cr}^3} \tag{3.13}$$

The equation term $(\varepsilon_S \mu_n E_{cr}^3)$ is commonly called as *Baliga's figure of merit* $(BFOM)$[1] for power devices. This FOM is an indicator of the impact of the semiconductor material properties on the drift region resistance.

[1] In Appendix C are reported more detailed information on Figures of Merit.

From eq. 3.13 it is clear the strong (cubic) dependence of the $R_{ON,ideal}$ with the critical electric field (E_{cr}^3) for the breakdown voltage. This relation favours the WBG semiconductors such as SiC. In Fig. 3.3 [34] is shown for Silicon and other WBG semiconductors, the behaviour of specific ON-state resistance for the drift region versus the critical electric field for a breakdown voltage fixed to 1000 V.

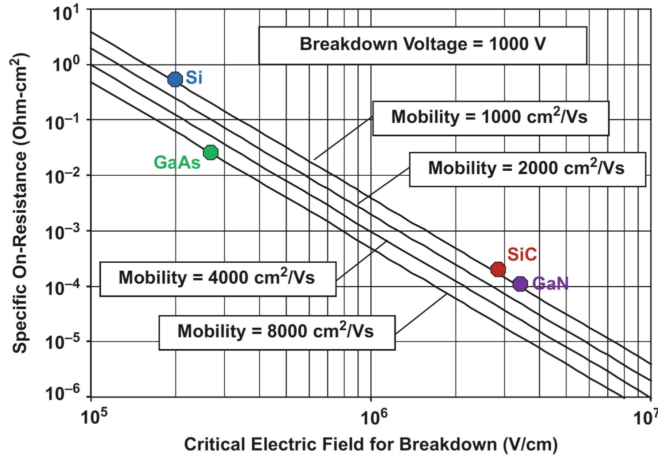

Fig. 3.3. Specific ON-resistance of the ideal drift region.

The improvement in drift region resistance for SiC in comparison with Silicon is largely due to its much larger critical electric field for the breakdown.

The Fig. 3.4 [35] is interesting because shows mainly the Silicon and SiC comparison of their specific ON-state resistances at $T = 25$ °C versus the breakdown voltages.

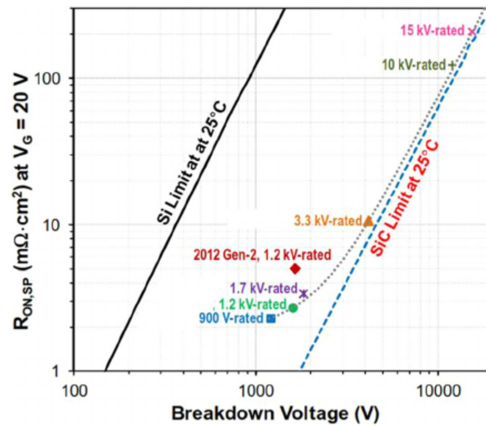

Fig. 3.4. Si and SiC comparison: specific ON-state resistance as function of breakdown voltage. Plot calculated at $T = 25$ °C and for a $V_G = 20$ V.

3.5 Trans-conductance

In forward bias, the $I - V$ characteristics for the power MOSFET resemble those of a resistor whose value can be modulated by the variable gate bias V_{GS}, in Fig. 3.5 [23] is shown this behaviour. For low V_{GS} applied to device, result that $R_{ch} >> R_{drift}$, while for high V_{GS} applied to device, result that $R_{ch} << R_{drift}$. Under these conditions, it is clear that R_{ON} can not further reduce with increasing the gate bias. Instead, increasing further the drain bias voltage (V_{DS}) the current (I_{DS}) in the power MOSFET saturates as shown in Fig. 3.6 [23].

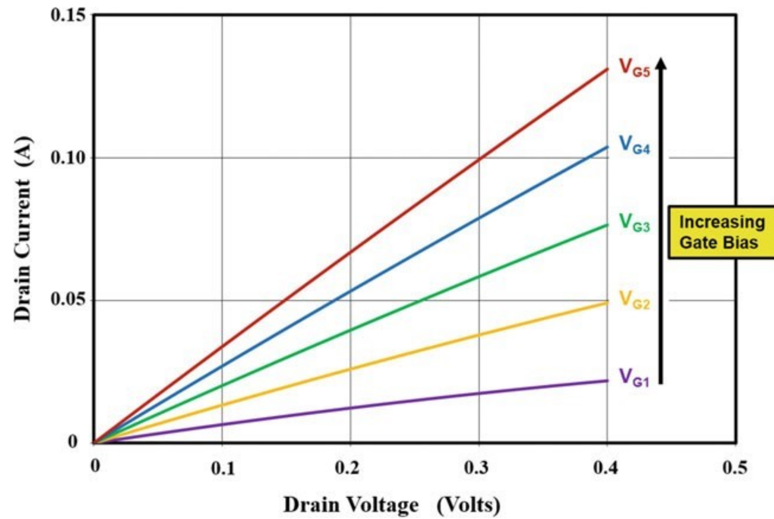

Fig. 3.5. Power MOSFET characteristics in the first quadrant at low drain bias voltages.

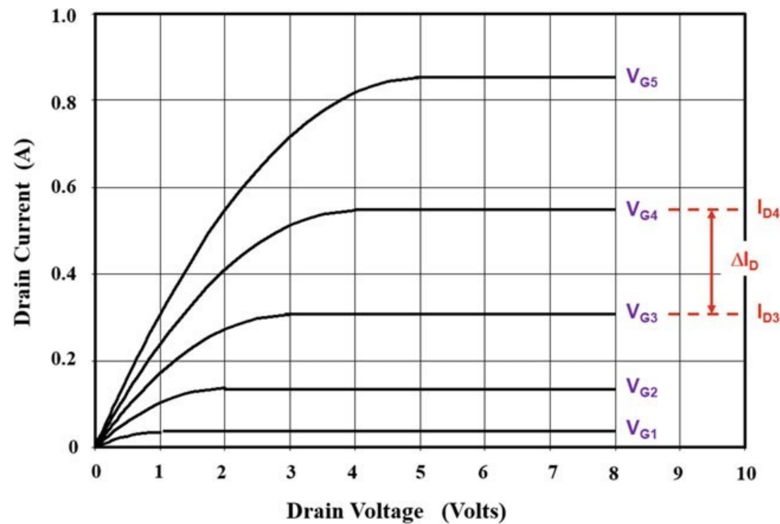

Fig. 3.6. Power MOSFET characteristics in the first quadrant at high drain bias voltages.

Thus, the V_{GS} control the saturation current $I_{D,sat}$, and this is a useful action when the device switch with inductive loads, indeed the setting of V_{GS} allows limiting the current flowing through the device during switching transients. The power MOSFET can sustain high power dissipation with very high junction temperature, but to work inside the safety area, the heating is kept below 473 K.

A useful parameter commonly used for describing the MOSFET behaviour is its trans-conductance (g_m). The trans-conductance is defined as the rate of change of the I_{DS} with incremental V_{GS}, see eq. 3.14:

$$g_m = \frac{\Delta I_D}{\Delta V_G} = \frac{(I_{D4} - I_{D3})}{V_{G4} - V_{G3}} \tag{3.14}$$

where the currents and voltages are indicated in Fig. 3.6. Thus, a high value of g_m allows to obtain a high I_{DS} with low V_{GS}, and in this condition, the switching speed of the power MOSFET improves with increasing trans-conductance.

When is applied a $V_{DS} < 0\ V$ to the MOSFET structure, the junction J1 (P-base-region/N-drift-region) becomes forward biased, in this case, current I_{DS} can now occur because the source electrode is also connected to the P-base region in the MOSFET structures to suppress the parasitic N-P-N transistor. This is referred to as current flow through the body diode of the power MOSFET. The body diode current flows when the drain bias voltage exceeds approximately 0.7 V in magnitude in the negative direction as shown in Fig.3.7 [23]. It is possible to induce larger I_{DS} current to flow at low $V_{DS} < 0\ V$ by the application of a V_{GS}. This current flow occurs through the channel of the MOSFET structure whose resistance determines the ON-state voltage drop in the third quadrant [23].

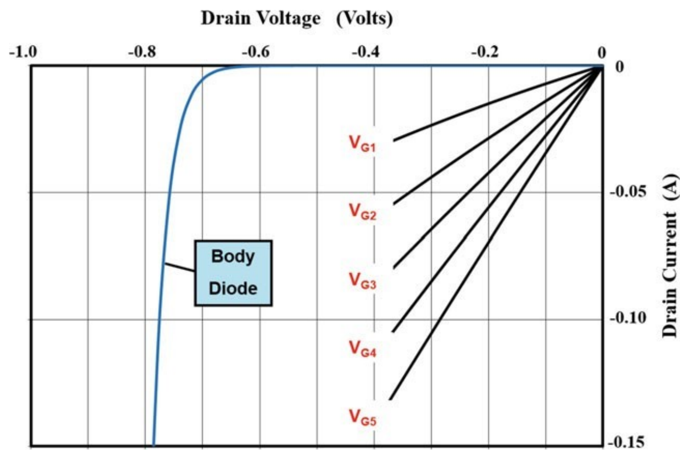

Fig. 3.7. Power MOSFET characteristics in the third quadrant at low drain bias voltages.

3.6 Ohmic contacts

An ohmic contact is a non-rectifying electrical junction, that is a junction between two conductors that present a linear current-voltage ($I - V$) curve as with Ohm's law. Instead, a junction or contact that does not present a linear $I - V$ curve is called non-ohmic. Non-ohmic contacts come in devices as (p–n junction, Schottky barrier, rectifying heterojunction, breakdown junction, etc.). Generally, the term "ohmic contact" implicitly refers to an ohmic contact of a metal to a semiconductor, where achieving ohmic behaviour is possible but requires careful technique.

The purpose of contacts is to carry electrical current into and out of the semiconductor, possibly without any parasitic resistance. Are required low resistivity Ohmic contacts, because they are crucial for high-frequency operation. Moreover, high-power and high-temperature require that the contacts must be reliable under severe conditions. SiC Ohmic contact resistances at room temperature are more often higher than contacts used for narrow bandgap semiconductors, anyway, they are enough low for most SiC applications. Lower contact resistance has been obtained with n-type 4H and 6H polytypes ($\approx 10^{-4} \div 10^{-6}\ \Omega \cdot cm^2$), and with p-type 4H and 6H polytypes ($\approx 10^{-3} \div 10^{-5}\ \Omega \cdot cm^2$) [36, 37].

A metal–semiconductor (M–S) junction is a type of junction in which a metal comes in close contact with a semiconductor material. This type of junction can either be rectifying or non-rectifying. The rectifying metal-semiconductor junction forms a Schottky barrier, making a device known as a Schottky diode, while the non-rectifying junction is called an ohmic contact. Metal-semiconductor junctions are crucial to the operation of all semiconductor devices. Usually, an ohmic contact is desired, so that electrical charge can be conducted easily between the active region of a transistor and the external circuitry. In this case, contact behaves as a resistor and the $I - V$ characteristics across the resistance follow a linear relationship. To reduce the ON-state resistance it is required that Ohmic contact would have negligible contact resistance so that it has a small voltage drop even with a high current value. The metal is characterized by the work function of the metal Φ_m (energy required to remove an electron from the *Fermi* level to the vacuum level), and the semiconductor is characterized by the work function of the semiconductor Φ_s (energy required to remove an electron from the *Fermi* level to the vacuum level). The work function of metal and semiconductor are measured with respect to the vacuum level (the energy of an electron at rest outside the material). Figure 3.8 [22] shows the thermal equilibrium energy band diagram of a metal-semiconductor Ohmic contact for n-type and p-type semiconductor. For Ohmic contact formation result: $\Phi_s(p) < \Phi_m < \Phi_s(n)$; in other

words the metal work function should be less than the n-type semiconductor work function and greater than the p-type semiconductor work function. In both cases, the *Fermi* levels are aligned between the metal and the semiconductor. The difference between metal *Fermi* levels and semiconductor *Fermi* level diminishes at the moment of forming because of the junction exchange charges at the edges of the bands.

In the energy band diagrams shown in Fig.3.8, there are no barrier blocks to halt the flow of electrons in the case of metal n-type contact and holes in the case of metal p-type contact. Hence the current can flow through the junction regardless of the polarity of the applied voltage.

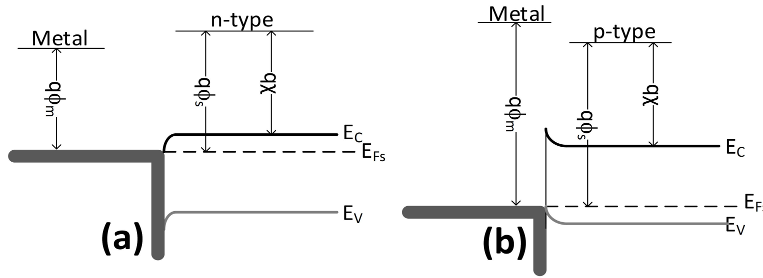

Fig. 3.8. Energy band diagram of metal-semiconductor Ohmic contact: (a) Metal and n-type semiconductor; (b) Metal and p-type semiconductor.

Contacts to power devices are made by using metal films deposited on the surface of its semiconductor layers. For these structures it is required to make ohmic contacts with n-type and p-type regions. Contacts resistance have to be as small as possible in order to minimize the ON-state voltage drop and power dissipation during current conduction. A low contact resistance is realised by using a metal-semiconductor contact with low barrier height φ_{bn} and a high doping concentration in the semiconductor to promote tunnelling current across the contact. For metal-semiconductor contacts with high doping level in the semiconductor, the contact resistance determined by the tunnelling process [22] is dependent upon the barrier height (φ_{bn}) and the doping concentration (N_D) as given by:

$$R_C = \exp\left[\frac{2\sqrt{\varepsilon_S m^*}}{h}\left(\frac{\varphi_{bn}}{\sqrt{N_D}}\right)\right] \tag{3.15}$$

where ε_S is the dielectric constant of the semiconductor, m^* is the effective mass for electrons, and h is *Planck*'s constant. Typically, specific contact resistances of less than $1 \times 10^{-5}\ \Omega - cm^2$ must be achieved in power device structures. The specific contact resistance calculated using the above formula is plotted in Fig. 3.9 [23] as a function of the doping concentration using the barrier height as a parameter.

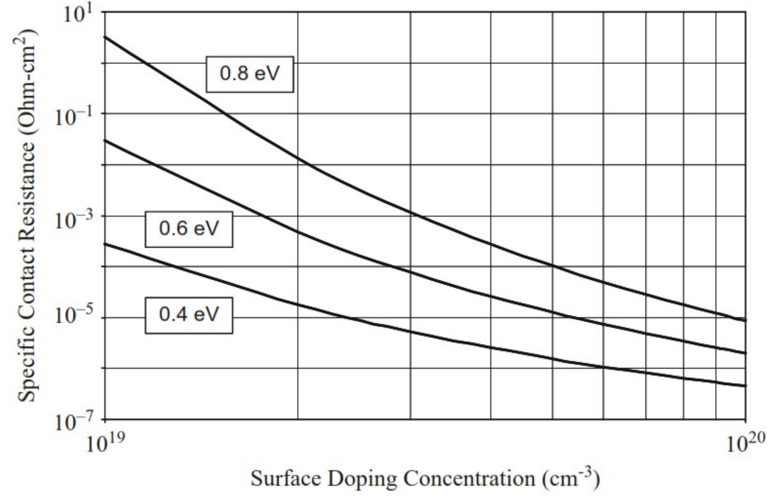

Fig. 3.9. Specific resistance at metal-semiconductor contacts.

In SiC rectifiers and power MOSFETs, the edge terminations that produce about to 100% of the ideal breakdown voltage had to be developed to maximize the performance of these devices.

3.7 MOS interface physics

In a power MOSFET, the density of free carriers and their mobility determine the channel conductivity, and the charge depends on gate bias. The free carriers transport mobility is reduced than that in the bulk of the semiconductor, this effect is due to the additional interface surface scattering phenomena. The study of the MOS interface goes through the flat band conditions, and the MOS surface charges analysis.

3.7.1 Flat band conditions

The energy band diagram for the ideal MOS structure is shown in Fig. 3.10 [23] for the case of no bias applied to the gate electrode. An ideal MOS structure is defined by the following points:

1. An insulator with infinite resistivity
2. Charge only in the metal and the semiconductor
3. Work function of the metal equal to that for the semiconductor

From the point (3) result that the *Fermi* levels for the metal (E_{FM}) and the semiconductor (E_{FS}) have the same energy. As a result, there is not any transfer of charge between the metal and the semiconductor without any gate bias; this leads to the flat band conditions shown in Fig.3.10, from which we can observe that:

$$q\phi_M = q\chi_S + \frac{E_G}{2} + q\psi_B = q\phi_B + q\chi_O \tag{3.16}$$

where, φ_M is the work function for the metal, χ_S is the electron affinity for the semiconductor, E_G is the energy bandgap for the semiconductor, ψ_B is the potential difference between the intrinsic and *Fermi* levels in the bulk of the semiconductor, ψ_B is the barrier height between the metal and the oxide, and χ_O is the electron affinity for the oxide. The *Fermi* level position in a semiconductor can be obtained by:

$$\psi_B = \left(\frac{E_i - E_{FS}}{q}\right) = \frac{kT}{q}\ln\left(\frac{p_0}{n_i}\right) \tag{3.17}$$

where E_i is the position of the intrinsic level, n_i is the intrinsic concentration, and p_0 is the hole concentration which can be assumed to be equal to the doping concentration (N_A) for Silicon. Since, a typical doping concentration for the P-base region is 1×10^{17} cm^{-3}, the *Fermi* level is positioned at 0.41 eV below the intrinsic level in the semiconductor at room temperature.

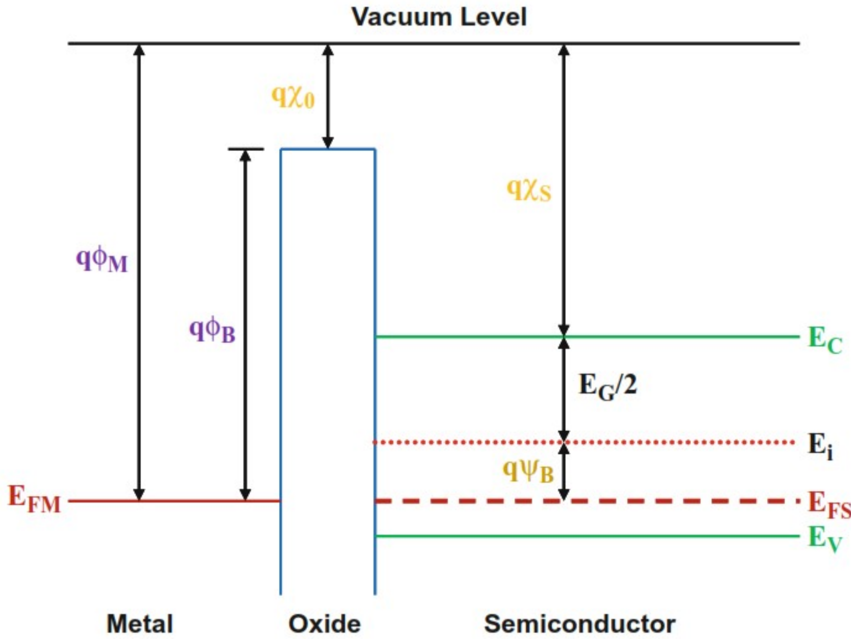

Fig. 3.10. MOS structure operating under flat band conditions.

3.7.2 MOS surface charge analysis

The channel conductivity in a power MOSFET structure is dependent by the mobile charge density created by the gate bias, and by the mobility for the carriers near the

oxide-semiconductor interface. The impact of surface scattering on the carrier mobility depending upon the module of the electric field perpendicular to the semiconductor surface, moreover, the mobility can be degraded of a factor of 2-3 times when compared with the mobility inside the bulk region. In order to compute the charge available in the MOSFET channel, it is required to calculate the distribution of potential in the MOS structure, as shown in Fig. 3.11 [23] for the case of a V_{GS} bias applied to. The potential distribution calculus $[\Psi(x)]$ can be derived by solving *Poisson*'s equation:

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_S} \tag{3.18}$$

with the charge density $\rho(x)$. The total space charge per unit area (Q_S) within the semiconductor is related to the electric field at the semiconductor surface (E_S) by *Gauss*'s law:

$$Q_S = -\varepsilon_S \cdot E_S \tag{3.19}$$

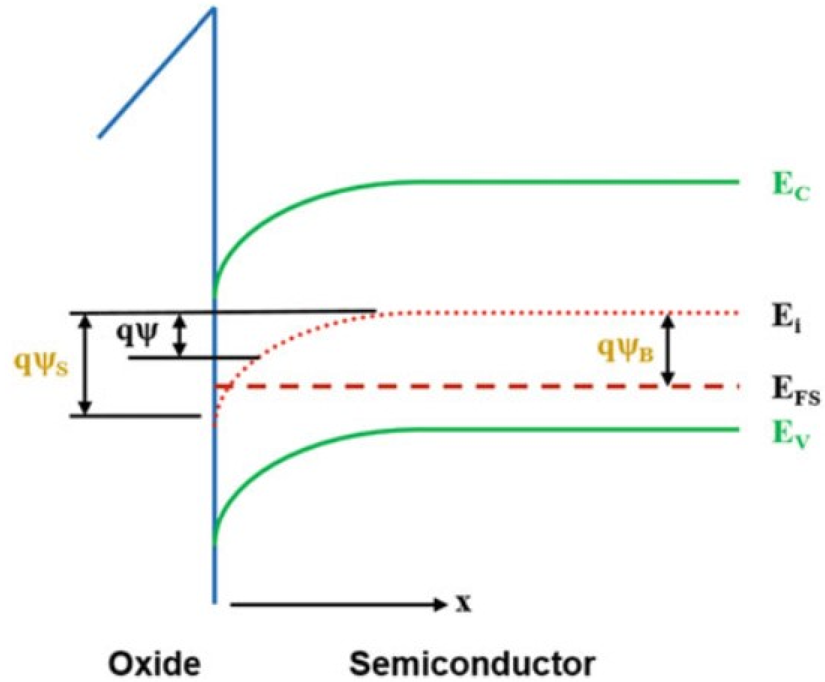

Fig. 3.11. Potential distribution within the MOS structure operating under inversion conditions.

For the evaluation of total charge in the semiconductor (p-type) shown in Fig. 3.12 [23] has been considered a doping concentration of $1 \times 10^{16}\ cm^{-3}$, at this doping concentration, the *Fermi* level is positioned at 0.206 eV from the valence band edge.

Result that $Q_S = 0\ C$ when $\psi = 0\ V$ as expected for flat band conditions. The potential, the charges and the electric field, distributions under the inversion conditions are shown in Fig. 3.13 [23]. The inversion layer charge (Q_i) is positioned too near the surface with the depletion layer charge, and it tends to extend further into the semiconductor. Under this condition, the V_{GS} results shared between the gate oxide and the semiconductor. In this case, the electric field varies linearly (thanks to its uniform doping) with distance in the semiconductor. When the MOS structure goes in a strong inversion regime, then all the variation of the gate bias are supported only across the gate oxide. Therefore, the depletion width in the semiconductor remains constant after the begin of the strong inversion process.

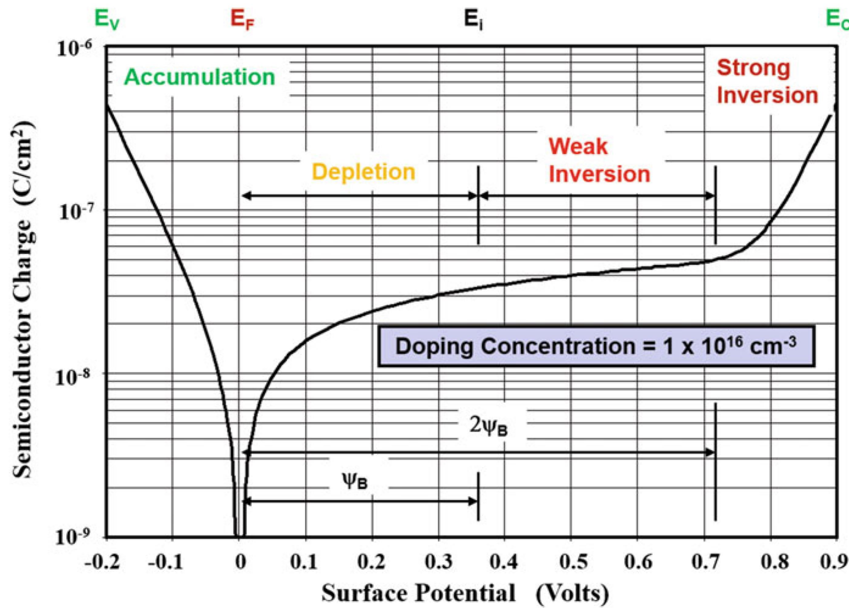

Fig. 3.12. Total charge per unit area within the semiconductor for an MOS structure.

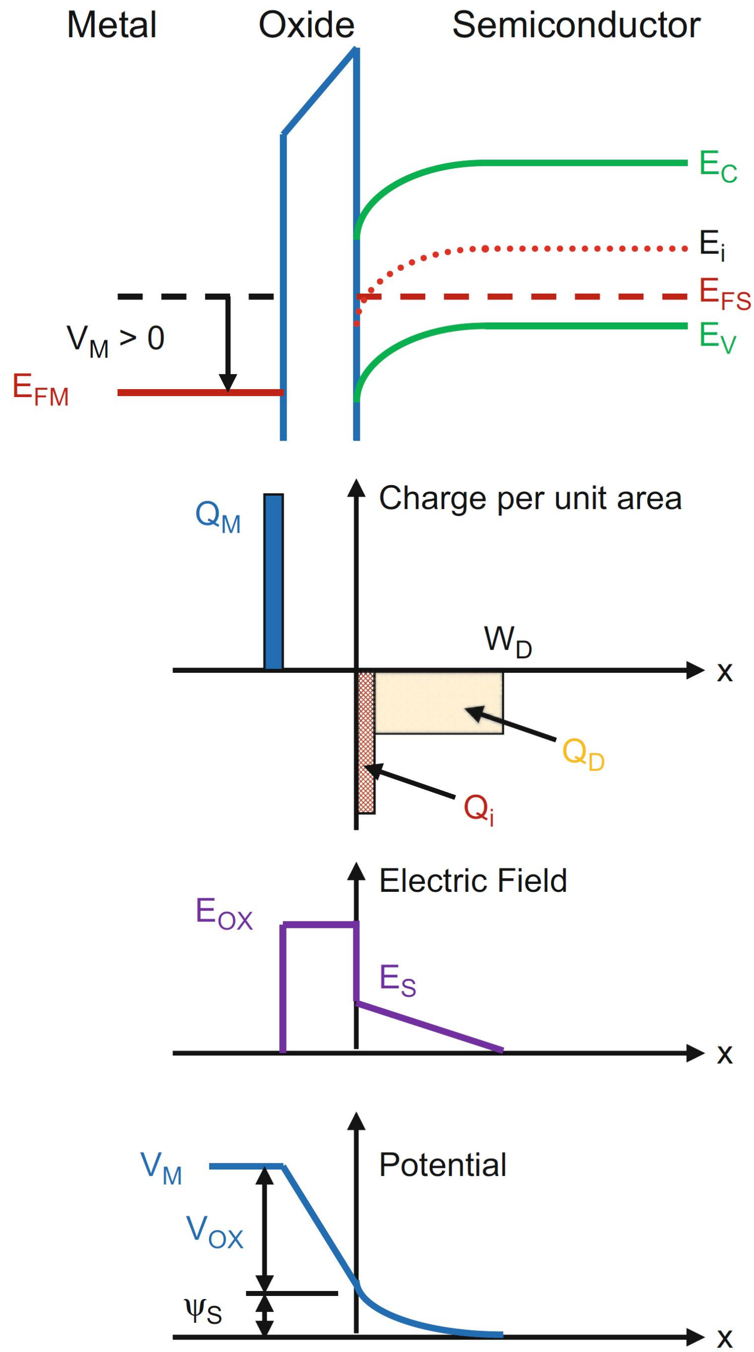

Fig. 3.13. Charge, electric field, and potential distributions within the MOS structure.

3.8 Threshold voltage

To avoid inadvertent turn-ON of device due to voltage spikes arising from noise, the threshold voltage (V_{TH}) have be maintained at $V_{TH} > 1\ V$ for most system applications. On the other hand for creating the charge in the channel is necessary to apply the voltage ($V_{GS} - V_{TH}$) where V_{GS} is the applied gate bias voltage. Thus, if the V_{TH} is too high, will be necessary to apply a higher V_{GS}. For a planar MOSFET structure, the V_{TH} can be determined by [23]:

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{3.20}$$

where N_A is the doping concentration of the P-base region, k is *Boltzmann*'s constant, and T is the absolute temperature. The positive fixed charge inside gate oxide tend to decrease the threshold voltage of amount given by :

$$\Delta V_{TH} = \frac{Q_F}{C_{OX}} \tag{3.21}$$

The threshold voltage variation for a 4H-SiC MOSFET has been determined by Baliga by means of numerical simulations as is shown in Fig. 3.14 [23] for the case of a gate oxide thickness of 500 Å.

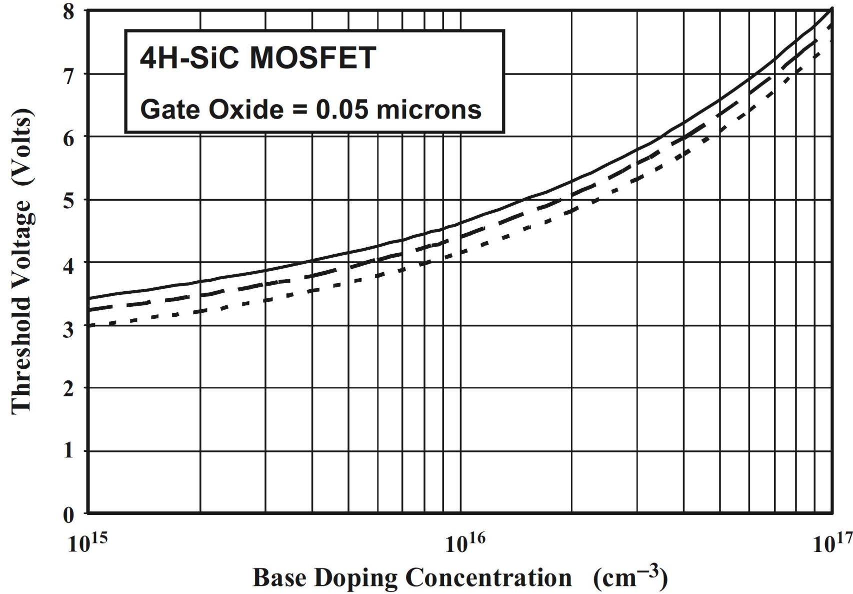

Fig. 3.14. Threshold voltage of 4H-SiC inversion-mode MOSFET structures (Solid line 300 K, dash line 400 K, dotted line 500 K).

3.9 Power MOSFETs: structure LDMOS and VDMOS

Lateral Double Diffused MOSFET (LDMOS) was the first power MOSFET structure which is still used to build output power stages in power management of integrated circuits. A lateral structure of power MOSFET is not adequate to design switches for high currents, where a vertical transistor should be used instead. The technical issues inherent to a classic lateral MOSFET design, have been mitigated by technical improvements shown in Fig.3.15 [38].

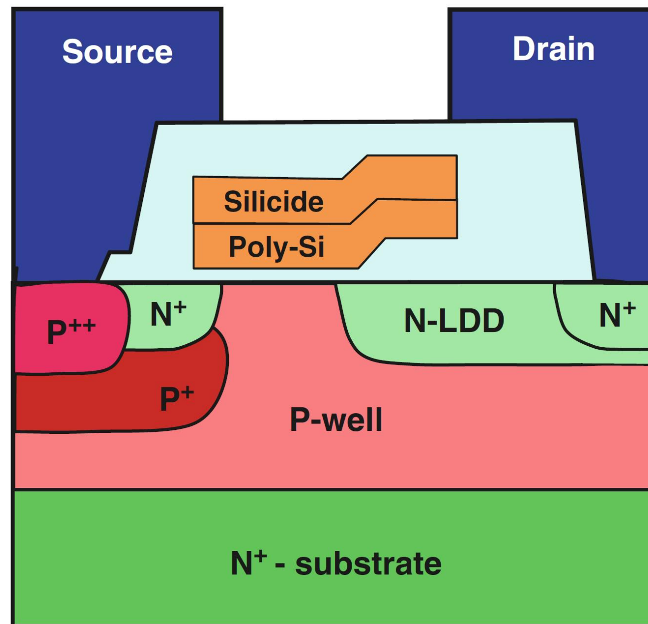

Fig. 3.15. Structure of an improved LDMOS design.

The high electric field spike happen at the corner of the gate can be reduced with a thicker oxide made by LOCOS [2] oxidation, and the resistance of the base region of the parasitic bipolar transistor can be reduced by an extra implantation to increase the dopant concentration below the source region. Unfortunately, the ON-state resistance and the internal capacitances of the LDMOS are not optimized. To improve the electrical performance of the power MOSFET, a Vertical Double Diffused MOSFET structure (VDMOS) has been introduced in the early 1980s, which basic VDMOS structure is shown in Fig. 3.16. A large area top electrode is the source terminal. The current flows from the source region N^+ to the channel under of the

[2] LOCOS, short for LOCal Oxidation of Silicon, is a microfabrication process where silicon dioxide is formed in selected areas on a silicon wafer having the SiO_2/Si interface at a lower point than the rest of the silicon surface.

lateral gate, and then into the N epitaxial layer where it is diverted to the N^+ substrate and finally reaches the drain electrode at the back of the die. The main design issue inherent to the VDMOS structure is current pinching between the two P-body regions as is shown in Fig. 3.17.

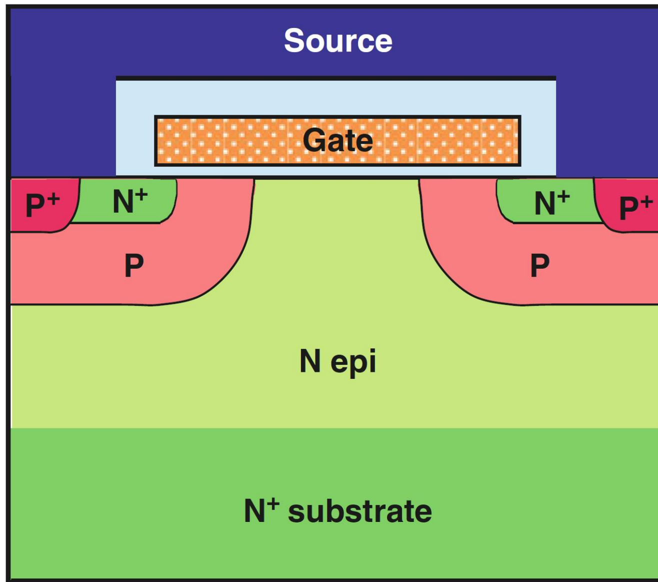

Fig. 3.16. Basic structure of a VDMOS transistor.

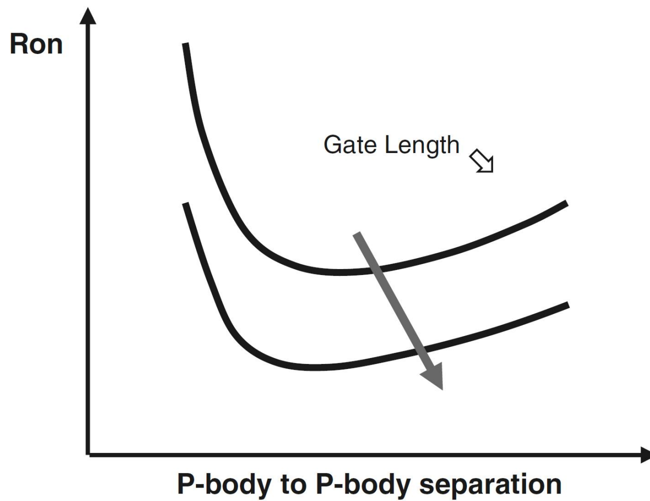

Fig. 3.17. JFET effect in a VDMOS transistor.

Current pinching called *JFET-effect* takes place if the distance between the two P-body regions is too small. This effect limits the ability to reduce the cell pitch in the design of a VDMOS structure. To reduce the cell pitch is the best way to reduce

the R_{ON} of MOSFET. Another way is to make channel shorter, but this is limited by the danger of punch-through, that occurs when the depletion induced by drain voltage penetrates the body region and reaches the source N^+ region.

This structure presents the overlap problem between the gate and the drain region among the P-body wells. The gate overlap leads to an increased C_{gd} capacitance which cannot be minimized due to the presence of the *JFET-effect*. Thus, for improving the FOM of the VDMOS design become necessary to improve the single ON-state resistance contributes.

3.10 Impact of body diode and of parasitic bipolar transistor

High voltage is supported across the junction formed between the P-base region and the N-drift region in the power n-channel MOSFET structure when a positive drain bias is applied. The same junction becomes forward biased if a negative bias is applied to the drain terminal. This P-N junction diode can, therefore, be utilized to conduct current through the power MOSFET structure in the third quadrant of operation. The equivalent circuit for the power MOSFET structure with the integral diode is shown in Fig. 3.18 [23]. The current flow path through the integral diode within the structure is shown on the cross section in the figure.

In some applications, it is desirable to utilize this current path to avoid the cost of an additional flyback diode[3].

The primary difficulty with the utilization of the integral diode in the power MOSFET structure is its poor reverse recovery characteristic due to the high lifetime in the N-drift region. In addition, the presence of the N^+ source region can lead to the turn-ON of the parasitic N-P-N bipolar transistor during the reverse recovery transient leading to destructive failure.

During the reverse recovery process, the current in the integral diode is reversed until it begins to support a positive drain bias voltage. The path for the reverse recovery current is illustrated in Fig.3.19 [23]. The entire P-base/N-drift junction collects the current which then flows into the contact to the P-base region. This current path occurs via the resistance of the P-base region. The voltage drop across the resistance forward biases the junction between the N^+ source region and the P-base region. If the voltage across this junction at point "A" exceeds the built-in potential, the

[3] A flyback diode is a diode connected across an inductor used to eliminate flyback, which is the sudden voltage spike seen across an inductive load when its supply current is suddenly reduced or interrupted. It is used in circuits in which inductive loads are controlled by switches, and in switching power supplies and inverters.

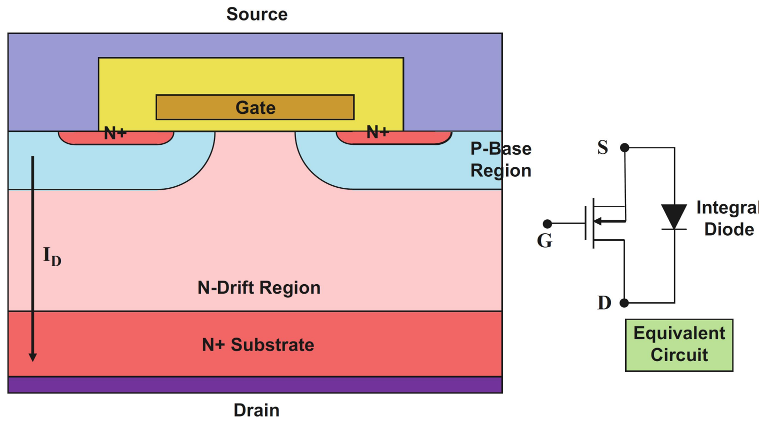

Fig. 3.18. Integral diode within the power MOSFET structure.

emitter of the parasitic bipolar transistor becomes activated. Under these conditions, the blocking voltage capability of the power MOSFET structures is degraded from the open-emitter breakdown voltage (BV_{CB0}) to the open-base breakdown voltage (BV_{CE0}). The drain blocking voltage during the reverse recovery transient can exceed the open-base breakdown voltage of the parasitic N-P-N transistor resulting in destructive failure. This problem can be overcome by the addition of the P^+ region in the structure as shown in Fig. 3.20 [23].

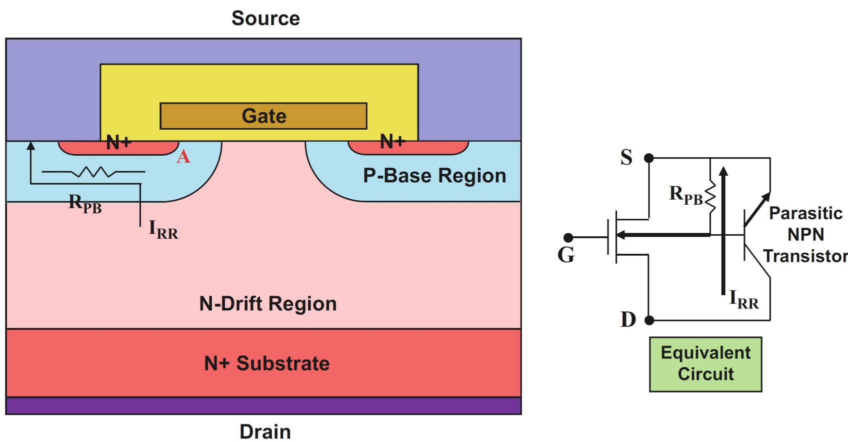

Fig. 3.19. Reverse recovery current path in the integral diode within the power MOSFET structure.

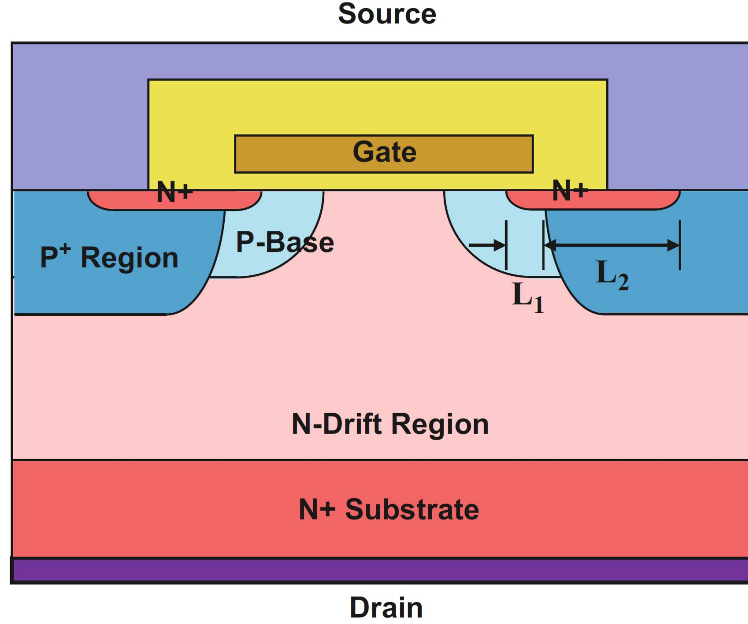

Fig. 3.20. The power VD-MOSFET structure with a deep P^+ region.

3.11 Power VD-MOSFET ON-state resistance

The R_{ON} for a power MOSFET is defined as the total resistance present between the drain and source electrodes when a $V_{GS} > 0\ V$ it is enough high to turn-ON the device. The R_{ON} limits the maximum current (I_{Dmax}) capability of the power MOSFET. The power dissipated during ON-state operation is given by:

$$P_D = V_D \cdot I_D = R_{ON} \cdot I_D^2 \tag{3.22}$$

which can also be expressed on a unit area basis:

$$\frac{P_D}{A} = P_{DA} = R_{ON,SP} \cdot J_D^2 \tag{3.23}$$

where A is the active area of the device, J_D is the ON-state drain current density, and $R_{ON,SP}$ is the specific ON-state resistance of the power MOSFET. The power dissipation per unit area is limited by the MOSFET reliability and by bearable maximum junction temperature (TJM). The increase in temperature above the ambient value (T_A) is determined by the thermal impedance of the package (R_θ). From Baliga [23] result that the maximum current density is given by:

$$J_{DM} = \sqrt{\frac{(T_{JM} - T_A)}{R_{ON,SP} \cdot R_\theta}} \tag{3.24}$$

From this expression, it is clear that the drain current density can be increased by reducing its specific ON-state resistance $R_{ON,SP}$. The power D-MOSFET structure is shown in Fig. 3.21 [23] with its internal resistance components. Moreover, the channel resistance (R_{CH}) discussed in advanced to this paragraph section, there are seven resistances that must be analysed in order to obtain the total ON-state resistance between the source and drain electrodes when the device is turned-ON. The total ON-state resistance for the power MOSFET structure is given by all the single components in series to the current path between the source and drain contacts:

$$\boxed{R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD}} \tag{3.25}$$

Every single contribution that forms the R_{ON} are considered in this paragraph. A cross section of the power VD-MOSFET structure is shown in Fig. 3.22 [23]. Here, W_{Cell} is the cell width; W_G is the width of the gate electrode; W_{PW} is the width of the polysilicon window; W_C is the width of the contact window to the N^+ source and P-base regions; and W_S is the width of the photoresist mask used during the N^+ source ion implantation. The current flow pattern in this device structure is indicated by the grey shaded area.

In *Model-A*, it is assumed that the current spreads at a 45° angle in the drift region and then becomes uniformly distributed when it enters the N^+ substrate.

In *Model-B* for current flow in the device is shown in Fig. 3.23 [23]. Here, the current is assumed to spread from the JFET region to the entire cell width when it reaches the N^+ substrate. The resistance of the drift region obtained using these models is discussed below.

3.11.1 Source contact resistance

The contact resistance is given by:

$$R_{CS} = \frac{2\rho_C}{Z\,(W_C - W_S)} \tag{3.26}$$

where Z is the cell length in the orthogonal direction to the cross section shown in Fig. 3.22. The specific contact resistance for the source regions is given by multiplying

the eq. 3.26 with the cell area ($A_{CELL} = W_{CELL} \cdot Z$) while recognizing that there are two source regions within each cross section shown in the Fig. 3.22:

$$R_{CS,SP} = \rho_C \frac{W_{CELL}}{(W_C - W_S)} \tag{3.27}$$

This expression indicates that the contact resistance tend to increase when reduces ($W_C - W_S$), i.e. when the design shrink the size of the polysilicon window. The cell width is related to the polysilicon gate width (W_G) and the polysilicon window width (W_{PW}):

$$W_{CELL} = W_G + 2\frac{W_{PW}}{2} \tag{3.28}$$

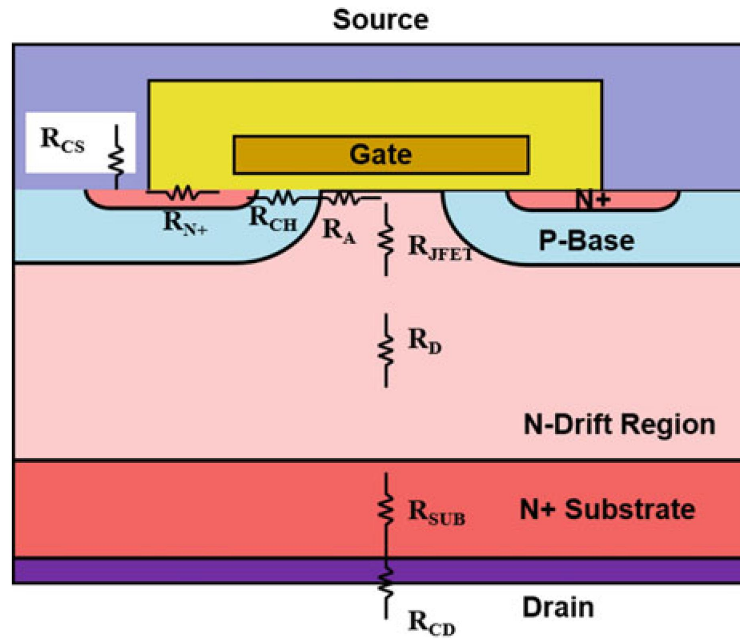

Fig. 3.21. Power D-MOSFET structure with its internal resistances.

3.11.2 Source region resistance

The resistance of the source region is given by the N^+ layer (ϱ_{SQN+}) and by its length (L_{N+}):

$$R_{N+,SP} = \frac{\rho_{SQN+} L_{N+} W_{CELL}}{2} \tag{3.29}$$

The specific resistance of the N^+ source region has a negligible contribution in the power VD-MOSFET structure.

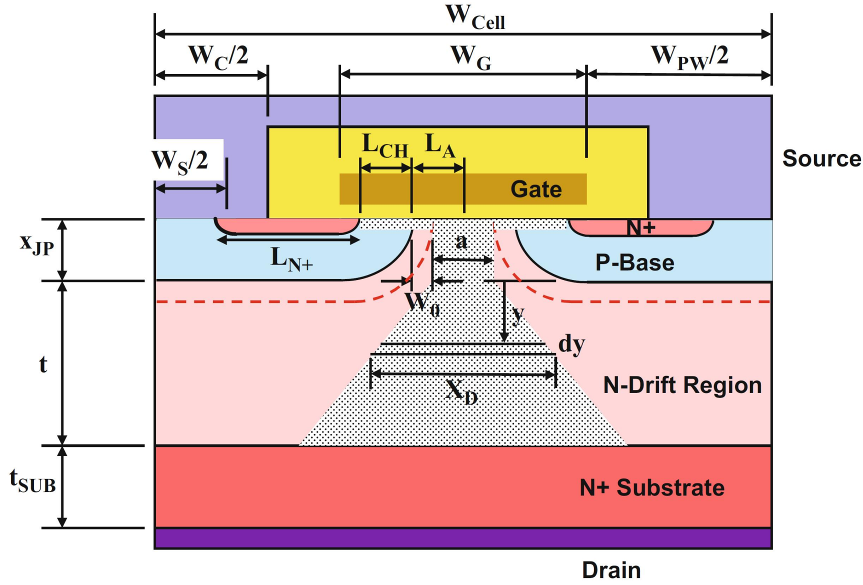

Fig. 3.22. Power D-MOSFET structure with current flow Model-A.

3.11.3 Accumulation resistance

The accumulation layer contribution is given by:

$$R_{A+,SP} = K_A \frac{(W_G - 2x_{JP}) W_{CELL}}{4\mu_{nA} C_{OX} (V_{GS} - V_{TH})} \tag{3.30}$$

The coefficient K_A take into account the current spreading from the accumulation layer into the JFET region. A typical value for this coefficient depends on the type of structure and can be numerically calculated.

3.11.4 JFET resistance

The JFET contribution is given by:

$$R_{JFET,SP} = \frac{\rho_{JFET} x_{JP} W_{CELL}}{(W_G - 2x_{JP} - 2W_0)} \tag{3.31}$$

The JFET region resistance can be reduced by increasing the gate width (W_G). However, this increases the channel and accumulation layer resistances.

3.11.5 Drift region resistance

The drift region resistance is given by:

Model-A (FIG. 3.22 [23])

$$R_{DS,SP} = \frac{\rho_D W_{CELL}}{2} \ln \left[\frac{a + 2t}{a} \right] \tag{3.32}$$

Model-B (FIG. 3.23 [23])

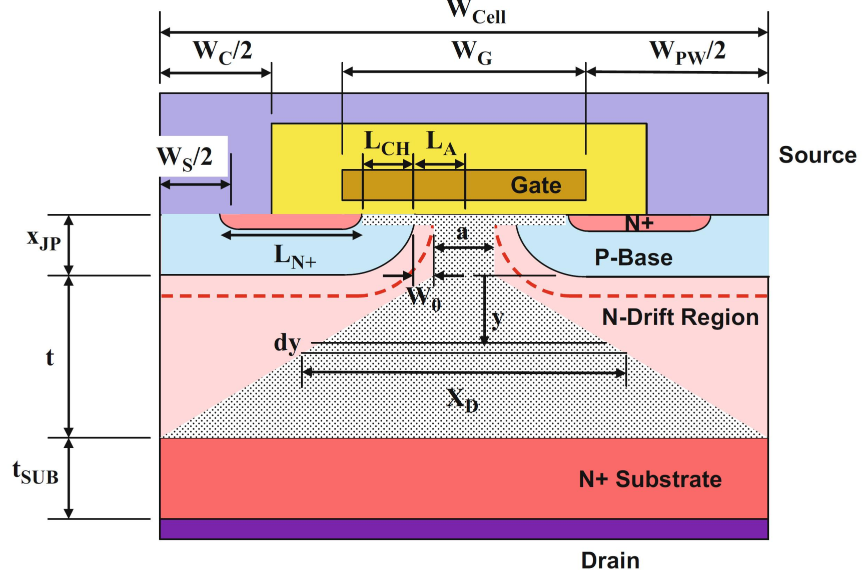

Fig. 3.23. Power D-MOSFET structure with current flow Model-B.

$$R_{DS,SP} = \frac{\rho_D t W_{CELL}}{(W_{CELL} - a)} \ln \left[\frac{W_{CELL}}{a} \right] \tag{3.33}$$

Model-C (FIG. 3.24 [23])

$$R_{DS,SP} = \frac{\rho_D W_{CELL}}{2} \ln \left[\frac{W_{CELL}}{a} \right] + \rho_D \left(t + \frac{a}{2} - \frac{W_{CELL}}{2} \right) \tag{3.34}$$

3.11.6 Substrate resistance

The substrate resistance N^+ is given by:

$$R_{SUB,SP} = \rho_{SUB} \cdot t_{SUB} \tag{3.35}$$

where ϱ_{SUB} and t_{SUB} are the resistivity and thickness of the N^+ substrate.

3.11.7 Channel resistance

For a lateral MOSFET structure has been obtained the expression:

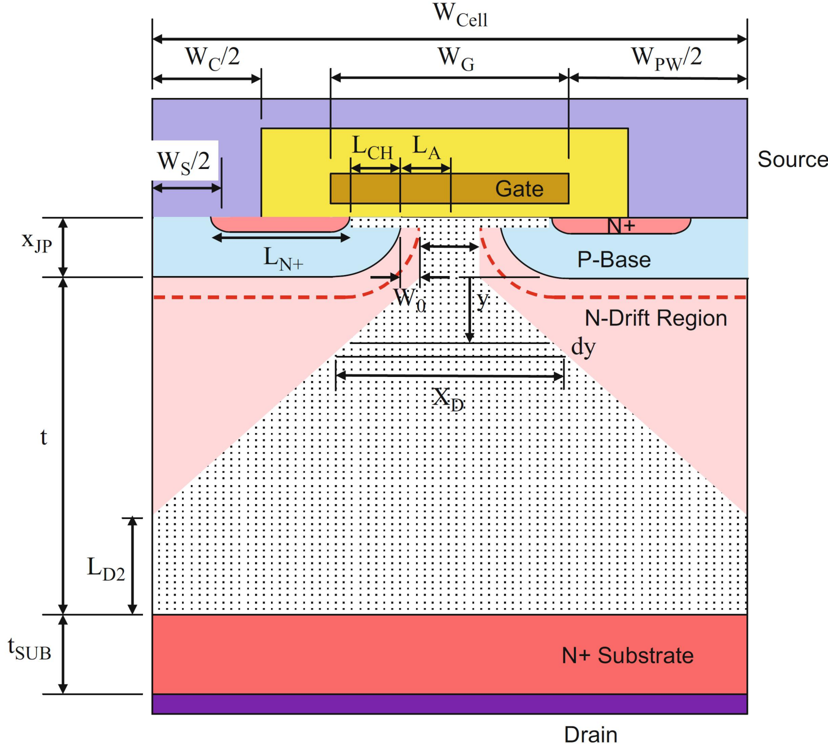

Fig. 3.24. Power VD-MOSFET structure with overlapping current distribution paths (Model-C) in drift region.

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni}C_{OX}\left(V_{GS} - V_{TH}\right)} \tag{3.36}$$

where L_{CH} is the channel length, μ_{ni} is the inversion layer mobility, C_{OX} is the specific capacitance of the gate oxide, V_{GS} is the gate bias voltage, and V_{TH} is the threshold voltage. The channel length (Fig. 3.22) is given by:

$$L_{CH} = \left(x_{JP} - x_{N+}\right) \tag{3.37}$$

The channel resistance for a vertical MOSFET is given by $R_{CH,SP} = 2{\cdot}(R_{CELL} \times A_{CELL})$ and so:

$$R_{CH,SP} = \frac{L_{CH}W_{CELL}}{2\mu_{ni}C_{OX}\left(V_{GS} - V_{TH}\right)} \tag{3.38}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}\ [F/\mu m^2]$.

This resistance can be reduced by increasing the capacitance C_{ox}, but this solution can slow down the switching speed of considered structure.

3.11.8 Drain contact resistance

The drain contact resistance is given by [39]:

$$R_{D,SP} = \frac{\rho_{Drain} W_{cell}}{2} \cdot \ln \left[\frac{a + W_{p+}}{a} \right] + \rho_{Drain} \left[t_{Drain} - \left(\frac{W_{p+}}{2} \right) \right] \tag{3.39}$$

where the width "a" of the JFET region is given by $a = (W_J - 2W_O)$, with W_O the depletion width, and $W_{p+}/2$ is the distance between the source and the end of p-base region [39].

Typically values for the contact resistivity are 1×10^{-5} or 1×10^{-6} $\Omega - cm^2$. This can be obtained by using a titanium contact layer to achieve a low barrier height, followed by a coating of nickel and silver. The nickel acts as a barrier between the titanium and the silver. The silver layer is ideal for mounting the chips to the package by using solders.

The contributions from each of the eight components of the ON-resistance are summarized in Table 3.1 together with their percentage contributions [23, 39].

Table 3.1. ON-STATE RESISTANCE COMPONENTS FOR A POWER VD-MOSFET STRUCTURE WITHIN THE 50 V AND WITH 20 μm CELL PITCH.

Resistance	**Value** $m\Omega - cm^2$	**Percentage Contribution**
Source Contact	R$_{CS,sp}$=0.05	2.2
Source	R$_{N+,sp}$=0.005	0.4
Channel	$R_{CH,sp}$=0.92	41
Accumulation	$R_{A,sp}$=0.66	29.5
JFET	$R_{JFET,sp}$=0.19	8.5
Drift	$R_{D,sp}$=0.34	15.2
Substrate	$R_{SUB,sp}$=0.06	2.7
Drain Contact	$R_{DS,sp}$=0.01	0.4
Total	$R_{T,sp}$=2.24	100

This high-value of the channel resistance may further get worse due to the presence of defects and traps in the SiC, and in particular at the interface between the gate oxide and the MOSFET's channel. For a more exhaustive study, physical models have been implemented to define interface defects and traps. Their single and conjoint effects have been evaluated on the electrical characteristics in a large range of temperatures and the results show in the next chapter.

3.12 Theory of interface defects and traps in SiC power MOSFETs

3.12.1 SiC crystal defects

SiC crystals present defects classified as the imperfection of different dimensions, they are mainly the point defects and the line defects.

Line defects can create crystallographic plane dislocations, mono-dimensional disturb and planar defects, causing stacking faults. During the semiconductor growth, the subsequent step, as cooling and device processing, can create defects in the SiC lattice. Defects can be intentionally introduced by impurity doping to increase conductivity. The introduction of deep levels, which serve as trapping centres, decreases the minority charge carrier lifetime and increases the resistivity by compensation effects.

Point defects are point-like defective volumes, limited roughly to the size of a unit cell of the crystal structure. For example, can be a substitutional impurity, vacancy, interstitial or antisite. A complete review on point defects in SiC was given by Schneider et al. [40] in 1993. The atomic substitutional impurities are atoms/molecules that can replace other atoms/molecules belonging to the crystal lattice. Vacancies occur if one atomic lattice position is left empty in the crystal. Instead, atoms not placed in an ordinary lattice site but in between are called interstitials. If they are of the same kind as the crystal lattice, they are called self-interstitials otherwise impurity interstitials. An interstitial atom together with a vacant lattice site is called "*Frenkel pair*". If in a compound semiconductor, such as SiC, can happen that a carbon atom takes a Silicon lattice site, or that Silicon is set on a carbon-place, in this case, the defect is called "antisite". Defects including two or more atoms form complex structures. A vacancy paired with an impurity atom forms a vacancy-impurity complex. An interstitial split is formed when two atoms take the lattice place of only one atom [41] and thus disturbing the lattice locally. Increasing the numbers of joining atoms, the defect can be assigned to defect clusters. When the whole atomic planes are shifted, the defect is no longer a point defect but belongs to the class of extended defects. A defect is of intrinsic origin if the defective volume is composed of the same atoms as the undisturbed crystal lattice. If foreign atoms, such as doping impurities, take part in the defect, the defect is classified as an extrinsic origin. Defects in the bandgap can be classified according to their energetic properties in the gap. Deep levels are characterized by their interaction strength with the bands, like traps or recombination centres. More detailed on this behaviour are in [42].

3.12.2 Defects: energetic properties

Defects are divided into two groups: shallow and deep levels. Depending on the size of the bandgap, indeed, a level may be regarded by its energetic location as deep in Silicon or shallow in a wide bandgap semiconductor.

Shallower levels can have a large interaction with one band, which is due to the large extension of its electron wave functions. In this case, electrons are freely bound to the impurity and thus they move as free electrons. The thermal energy at room temperature is enough high to ionize multiple-levels. Shallow levels can be used to control the *Fermi* level in the semiconductor, thus they can be intentionally introduced into the semiconductor to define the donor and acceptor concentrations, N_D and N_A, respectively, i.e. the available charge carriers needed for conductivity. Deep levels have a short steep potential (Fig. 3.25), and their electron wave functions are largely localized in the defect site.

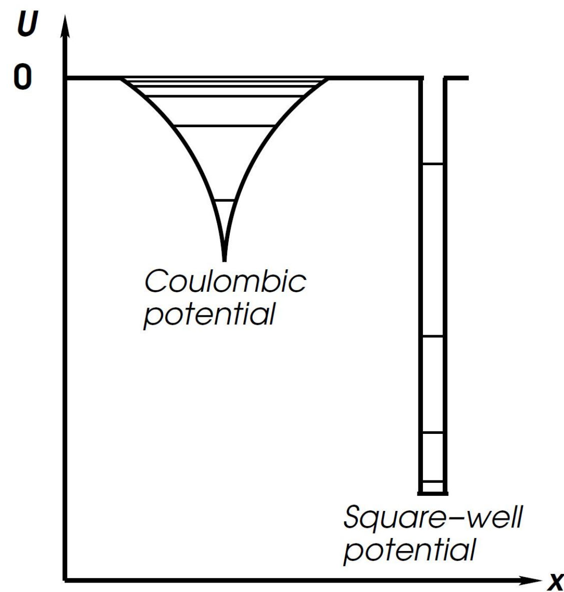

Fig. 3.25. Schematization of the one-dimensional potential for shallow and deep levels.

For not complex boundary situations, the higher charge states can be approximated by the screened *Coulomb* potential[4]. All the charge carriers can be trapped and only released if enough thermal energy will be available. The traps concentration is often only a fraction of the net doping concentration. However, in most cases, the deep level density is too small to affect the electron density in the bands.

[4] In solid-state physics, especially for metals and semiconductors, the screening effect describes the electrostatic field and *Coulomb* potential of an ion inside the solid.

3.12.3 Interaction with the bands

Usually the deep levels are classified after their primary interaction with the bands. When the electron capture rate, C_n, and the hole capture rate C_p, are tied by relation:

$C_n >> C_p$

then the defect act as an electron and is called an electron trap.

Instead, when result:

$C_n << C_p$

then the defect act as a hole and is called a hole trap.

Lastly, if result:

$C_n \approx C_p$

then the defect interacts with the same strength with both bands and is regarded as a generation-recombination centre, see Fig. 3.26.

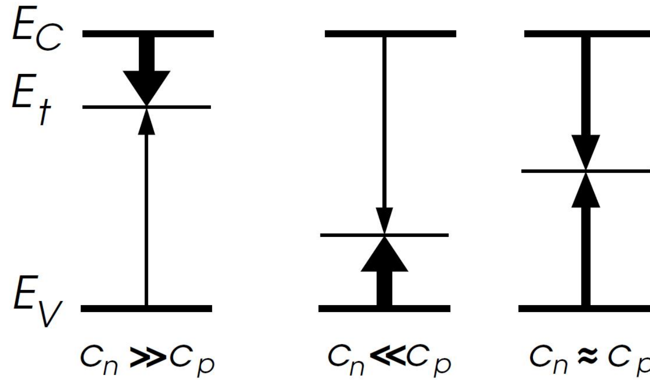

Fig. 3.26. Capture and emission characteristics of traps and recombination centres.

3.13 Traps at the interface SiC and gate oxide

Progress in the development of SiC-based devices is due mainly to the improvement of crystal quality of SiC-substrates. For the SiO_2/SiC-MOS structures, the *density of interface states* (D_{it}) at SiO_2/SiC interfaces is increased in the whole bandgap by at least two orders of magnitude [43]. This increment of D_{it} is due to from carbon atoms precipitates at the interface during the oxidation process [43], [44].

The high density of shallow states is responsible for the low channel mobility in 4H-SiC MOSFET prepared on SiC $\langle 0001 \rangle$ crystal faces. These shallow states are caused by the *Near Interface Traps* (*NITs*). Thus, traps are located in the oxide about 15 Å to 20 Å from the interface and 2.77 eV below the SiO_2 conduction band edge [45], [46].

Instead, the valence band edges of different SiC polytypes results aligned to the SiO_2 conduction band edge [47] and the 4H-SiC bandgap is larger than the bandgaps of the 6H and 15R polytypes. *NITs* are positioned inside the bandgap of the 4H-SiC polytype. *The NITs that act as acceptors, tend to reduce the channel current by Coulomb scattering*. The density of interface states D_{it} is composed of different contributions:

- Dangling Bonds (DB)
- sp^2-bonded carbon clusters of different size
- *NITs*

The quantity and distribution of "Dangling Bonds" (DB) depend upon the quality of wafer and on the technological treatments to which it has been subjected. Carbon clusters, contribute the major portion to D_{it} over the SiC bandgap. *NITs*, dominate D_{it} in 4H-SiC MOS capacitors near to the conduction band edge and are responsible for the degradation of channel mobility in 4H-SiC MOSFET. Appropriate crystal orientations and improved deposition techniques for insulating films are considered as possible solutions to reduce the density of *NITs* in 4H-SiC MOSFET.

3.14 Defects and traps: carrier mobility limitation

The relationship "diffusivity-mobility" for heavily doped semiconductors exhibit a Gaussian doping profile and band tail, it has been studied by Khan and Das in [48]. They observed that the electron distribution in n-type semiconductors and the hole distribution in p-type semiconductors take place in energy states in both the allowed band and inside band tail. In this case, electronic properties are influenced by the doping profile of donor and acceptor impurities; thus, increasing the doping will increase the carrier density in the semiconductor.

When impurity concentrations are low, local energy states are formed in the forbidden band of a semiconductor. Since the impurity atoms are enough distant, there is no interaction between them. When the numbers of carriers in the allowed bands are small, these carriers obey the *Boltzmann* statistics, which ignores the quantum indistinguishability of particles. Doping levels at which there are no interactions between impurity atoms (the carrier gas is under the *Boltzmann* statistics) is indicated as a low degree of doping and the corresponding conductors are called lightly doped. But, when the doping degree goes beyond this level, the average distance between the impurity atoms decreases and thus these atoms begin to interact together [49]. In this case, local energy levels extended out to form an impurity band. This process involves

an ionization energy reduction for impurity atoms. This behaviour depends on the structure of the impurity band and on the relative number of carriers in the allowed states. When impurity concentration tends to be further reduced, then the ionization energy tends to zero, and the impurity band merges with the conduction band (in the case of donor impurities) or with the valence band (in the case of acceptor impurities). Thus, a single allowed band is formed in a crystal.

When the impurity concentration present a very high density of carriers (heavily doped crystals) it is necessary to apply the *Fermi–Dirac* statistics. In this case, the gas of particles is defined as degenerate, and thus the semiconductor is often called "degenerate semiconductor." Doping levels used in semiconductor devices tend to increase with the progress of miniaturization. This trend can be explained considering the classic p-n junction; it contains the charge of fixed donors or acceptors. Thus, electric fields produced by this fixed charge must support the difference of potential between the n and p regions of the junction. It results that, greater will be the charge density or the doping level, and greater will be the electric fields, and the thinner the depletion layer needed to accommodate the potential difference. Thus, the increase in doping levels that promote miniaturization.

3.15 4H-SiC MOSFETs: channel mobility and technological processes for improvement of interface quality

Vertical SiC-DMOSFET is an interesting device for high-power applications that require high values of "Figure of Merit" and excellent physical and electrical properties [50, 51]. However, the device performances are sharply influenced by the quality of gate oxide, which remains one of the major worries despite the recent improvements of 4H-SiC processing technology [52, 53]. The distribution of defect density into the oxide and at the SiC interface, tends to modify the charge distribution in the channel region, and thus, and thus it will vary the threshold voltage of device [54]. The study of charge distributions trapped at the SiO_2/SiC interface and the evaluation of their effects on the electrical characteristics are essentially based on numerical simulations.

The low channel mobility is a condition that emerges when there are electrons trapped at interface states (D_{it}) near the conduction band, that are involved in a process of scattering. In particular physical conditions, the Coulomb scattering *Coulomb* scattering [5] process may occur, it may lead to the mobility degradation process.

[5] Some theoretical note is reported in the section "Mobility degradation due to scattering" 3.18

Moreover, these trapped charges at the chSiO2/SiC interface are in turn as a possible reason for V_{TH} instabilities when the device works at full load.

The interface quality of SiO_2/SiC is a crucial step in determining the MOSFET electrical characteristics. In fact, the presence of Carbon atoms during the oxidation processes leads to a higher concentration of defects at the interface in comparison to conventional Silicon technology.

From literature, a schematic overview of the trapped charges in the oxide and SiO_2/SiC interface is shown in Fig.3.27 [22]. More in detail, mobile ions can diffuse during the SiO_2 grown process and they are mainly related to atoms such as potassium (K) and sodium (Na) [23]. At the same time, trapped charges are usually distributed also deeply in the oxide, which are due to the structural imperfections [55]. Moreover, near the interface with a concentration that depends on the oxidation process, we can consider a thin film of fixed charges, that can become scattering centres that influence the device threshold voltage. Finally, the so-called interface-trapped charges in Fig.3.27 (red-cross) are related to defects which have energy levels inside the SiC bandgap.

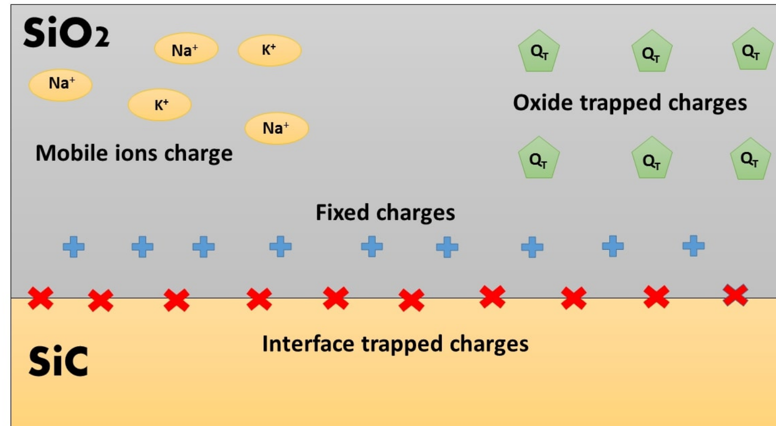

Fig. 3.27. Oxide and SiO_2/SiC interface charges.

In order to improve the channel mobility in 4H-SiC MOSFETs, different thermal treatments of the gate oxide have been explored in [56], in which it was established a correlation between the channel mobility and the type of passivation process applied to the interface. Roccaforte et al. reported a complete comparison between the Nitrogen and Phosphorous annealing processes for the gate oxides. In [57] has been studied how the MOSFET interface (SiO_2/4H-SiC) can influence the electrical properties, and thus the MOSFET behaviour. Was observed that the *nitridation process* of the

gate oxide in N_2O, tend to reduce the interface defects, and consequently we assist to an increment of mobility in the MOSFET channel as the temperature increases. This effect has been explained as due to the reduction of *Coulomb* scattering phenomena and of reduction of trapped electrons at interface. To improve the quality of interface it is possible to use a *Post-Oxidation Annealing* (POA) of the gate oxide in a Nitrogen-rich atmosphere (NO or N_2O or $POCl_3$) [57]. Roccaforte observed that the mobility of a MOSFET processed in $POCl_3$ was found to decrease with increasing of temperature. In general, mobility values in the range of 25-50 $cm^2 \times V^{-1} \cdot s^{-1}$ can be achieved using these POA treatments. Higher values of the mobility (up to 150 $cm^2 \times V^{-1} \cdot s^{-1}$) have been found when the gate oxide is annealed in Al-rich atmosphere or in $POCl_3$. Low values for the channel mobility (< 5 $cm^2 \times V^{-1} \cdot s^{-1}$) measured with thermally grown SiO_2 layers of gate oxide are attributed to the high density of interface traps (D_{it}) near the conduction band edge, which are in the order of 10^{13} $eV^{-1}cm^{-2}$. These electrically active states can originate from defects of different nature, such as clustering of Carbon atoms and/or intrinsic oxide defects in the near interface region. The presence of interface charge states leads to a reduction of electron mobility in the inversion layer, mainly due to *Coulomb* scattering effect caused by charges trapped at the interface and inside the oxide. Commercial power SiC-MOSFETs are produced using nitridation processes of the gate oxide (either in NO or N_2O). But, however their present a V_{TH} instability, indeed a positive V_{TH} shift under stress leads to into an increase of the device R_{ON}. Instead, when V_{TH} is not stable and shifts in the negative direction under stress, then a significant increase of the leakage current can occur in the OFF-state, thus leading to premature device failure [58]. Even if nitridation process could produce devices with a stable V_{TH} under stress at room temperature, exist a deep link between temperature $T > 150\ {}^{\circ}C$ and undesired V_{TH} shift. The threshold voltage instability depends on an activated mechanism involving defects present at the interface and inside the gate oxide. Thus, the V_{TH} instabilities occurring in response to the bias-temperature stress can be associated to the charging and activation of *NITs*, i.e., trapping states located inside the SiO_2 layer at a deep from few to about 100 Åaway from the physical SiO_2/SiC interface.

3.16 Carrier mobility

Carrier mobility in the device structure is mainly a function of temperature, doping concentration, local electric field and scattering mechanisms that involve surface-phonon, surface-roughness, and *Coulomb* scattering from both interface charges and ionized impurities in the bulk. In detail, for a vertical 4H-SiC MOSFET in Fig. 4.30,

we have assumed the *Caughey–Thomas* low field mobility model in the form of:

$$\mu_{n,p} = \mu_{0n,p}^{\min}\left(\frac{T}{300}\right)^{\alpha_{n,p}} + \frac{\mu_{0n,p}^{\max}\left(\frac{T}{300}\right)^{\beta_{n,p}} - \mu_{0n,p}^{\min}\left(\frac{T}{300}\right)^{\alpha_{n,p}}}{1+\left(\frac{T}{300}\right)^{\gamma_{n,p}}\left(\frac{N}{N_{n,p}^{crit}}\right)^{\delta_{n,p}}} \quad (3.40)$$

where N is the total (local) doping concentration, $\mu_{0n,p}$ terms are the carrier mobilities assumed at room temperature, is the doping concentration at which the mobility is halfway between the *max* and *min* values, and α, β, γ, and δ are process dependent coefficients, Table 3.2 . This model was experimentally validated for SiC in [59, 60].

Finally, the electron and hole impact ionization rates, $a_{n,p}$, which are needful to predict in details the avalanche device breakdown voltage, are modelled through the following empirical expression [61]:

$$\alpha_{n,p} = a_{0n,p}\exp\left(-\frac{b_{0n,p}}{E}\right) \quad (3.41)$$

where $a_{0n} = 2.5\times10^{5}\ cm^{-1}$, $a_{0p} = 3.25\times10^{6}\ cm^{-1}$, $b_{0n} = 1.84\times10^{7}\ V/cm$, and $b_{0p} = 1.71\times10^{7}\ V/cm$ are the carrier ionization coefficients measured in [62, 63]. Parameters details about the applied 4H-SiC simulation setup are reported in recent authors manuscripts [64–66]. Moreover, it is supported by experimental results in a wide range of currents and temperatures obtained with Al implanted 4H-SiC *pin* and also with Schottky diodes [67–69].

In addition, for high electric fields, the expected mobility reduction due to the carrier saturated drift velocity ($\nu_{sat} = 2\times10^{7}\ cm/s$) has been described by using:

$$\mu_{n,p}(E) = \frac{\mu_{n,p}}{\left[1+\left(E\frac{\mu_{n,p}}{\nu_{sat}}\right)^{k_{n,p}}\right]^{\frac{1}{k_{n,p}}}} \quad (3.42)$$

where E is the electric field in the direction of the current flow. Finally, mobility degradation effects in the inversion layer, where different scattering mechanisms take place due to a perpendicular electric field component ($E\perp$), have been accounted as follows:

$$\mu_{n,p}(E_{\perp}) = \mu_{n,p}\cdot\left(1+\frac{E_{\perp}}{E_{n,p}^{crit}}\right)^{2} \quad (3.43)$$

The carrier mobility model parameters adopted during the simulations are summarized in Table 3.2 [70, 71].

3.17 Bandgap narrowing

Using a 2D TCAD simulator [72], the device structure was modelled and finely meshed wherever appropriate and in particular around the p-n junctions and within the channel region, just below the SiC-SiO_2 interface, where a mesh spacing down to 25 *nm*

Table 3.2. ON-STATE RESISTANCE COMPONENTS FOR A POWER VD-MOSFET STRUCTURE WITHIN THE 50 V AND WITH 20 μm CELL PITCH.

Parameter	Unit	n-type	p-type
$\mu_{0n,p}^{\min}$	$cm^2/V \cdot s$	40.0	15.9
$\mu_{0n,p}^{\max}$	$cm^2/V \cdot s$	950	125
N^{crit}	cm^{-3}	2×10^{17}	1.76×10^{19}
E^{crit}	V/cm	1.5×10^{6}	1.50×10^{6}
α	–	-0.5	-0.50
β	–	-2.4	-2.15
γ	–	-0.76	-0.34
δ	–	0.76	0.34
κ	–	2	1

was used. The key physical models used in the simulations include the incomplete doping ionization, apparent bandgap narrowing, impact ionization, *Shockley-Read-Hall* (SRH) and *Auger* recombination processes; carrier lifetime and mobility are function of both doping concentration and temperature. Moreover, the temperature dependence of the 4H-SiC bandgap is in the form of [70]:

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta} \tag{3.44}$$

where $E_G(0)$ is the bandgap energy at $T = 0\ K$, and α, β fitting parameters. For 4H-SiC the bandgap energy $E_G(0) = 3.26\ eV$, α and β are $6.5 \times 10^{-4}\ eV/K$ [73]. Result that the dependence of the 4H-SiC MOSFET bandgap from temperature is shown in Fig. 3.28, from which observe that the bandgap decreases of about 3.86% from the room temperature up to $T = 600\ K$.

where $E_g(0)$ is the bandgap energy at $0\ K$, $\alpha = 3.3 \times 10^{-4}\ eV/K$, and $\beta = 0$ are specific material parameters. Due to the wide bandgap of 4H-SiC, not all doping atoms can be assumed as fully ionized. Using the *Fermi–Dirac* statistics, the carrier concentrations and (i.e., the number of ionized acceptors and donors, respectively) can be calculated with the following expression [74]:

$$N_{a,d}^{-+} = \left(-1 + \sqrt{1 + 4 g_{a,d} \frac{N_{a,d}}{N_{V,C}(T)} e^{\frac{\Delta E_{a,d}}{kT}}}\right) \times \left(2 g_{a,d} \frac{N_{a,d}}{N_{V,C}(T)} e^{\frac{\Delta E_{a,d}}{kT}}\right)^{-1} \tag{3.45}$$

where N_a and N_d are the substitutional p-type and n-type doping concentrations, N_V and N_C are the hole and electron density of states varying with temperature,

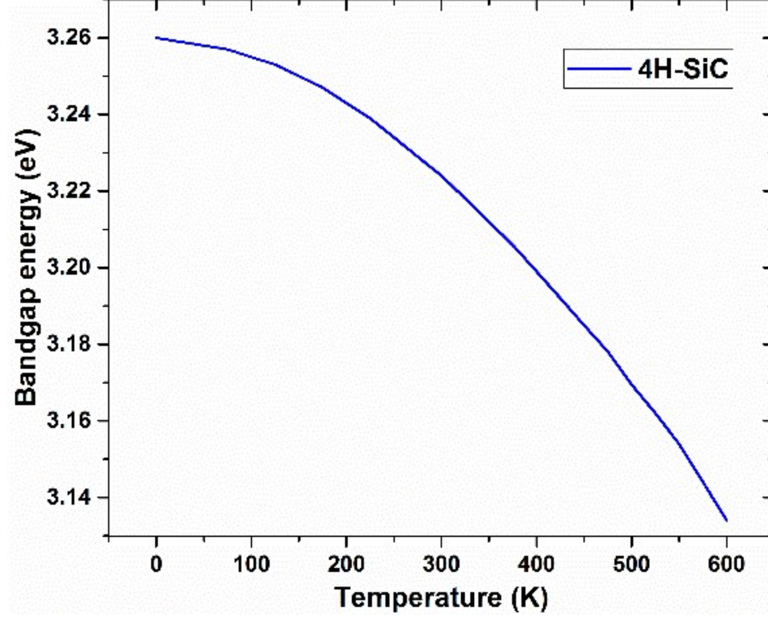

Fig. 3.28. Bandgap energy of 4H-SiC as a function of temperature.

$g_a = 4$ and $g_d = 2$ are the degeneracy factors of the valence and conduction band, and $\Delta E_a = 200\ meV$ and $\Delta E_d = 100\ meV$ are the ionization energies for acceptor and donor impurities, respectively.

An apparent bandgap narrowing effect as a function of the ionized doping in the p-type and n-type regions is also included during simulations according to the *Lindefelt's model* of the band edge displacements [25]:

$$\Delta E_G^{a,d} = A_{a,d}\left(\frac{N_{a,d}^{-+}}{10^{18}}\right)^{1/2} + B_{a,d}\left(\frac{N_{a,d}^{-+}}{10^{18}}\right)^{1/3} + C_{a,d}\left(\frac{N_{a,d}^{-+}}{10^{18}}\right)^{1/4} \tag{3.46}$$

Here, $A_{a,d}$, $B_{a,d}$, and $C_{a,d}$ are specific 4H-SiC constants, reported in Table 3.3 [74].

Table 3.3. Apparent Bandgap Narrowing Model Coefficients.

Lindefelt's Coefficients	**Value**
$A_{a,d}$	1.54×10^{-3}, 1.17×10^{-2}
$B_{a,d}$	1.30×10^{-2}, 1.50×10^{-2}
$C_{a,d}$	1.57×10^{-2}, 1.90×10^{-2}

The electron and hole lifetimes, useful to define the *SRH* recombination rate, are modelled as functions of doping by means of the relation proposed in [75].

$$\tau_{n,p} = \frac{\tau_0^{n,p}}{1 + \left(\frac{N}{N_{n,p}^{SRH}}\right)} \tag{3.47}$$

where N is the total impurity concentration for a given device region, $N_{n,p}^{SRH} = 5 \times 10^{16}\ cm^{-3}$ is a reference constant, and $\tau_{0n} = 500\ ns$ and $\tau_{0p} = 100\ ns$ are process-dependent parameters taken from [76]. As it will be confirmed by comparison with experimental data, the above assumptions provide reliable simulation results also without introducing an explicit yet reasonable state density ($D_{it} < 5 \times 10^{12}$ cm^2/eV [77]) at the SiO_2/SiC interface.

3.17.1 The average life of carriers and recombination phenomena

The lifespan of carriers within the heavily doped regions was calculated using the following empirical eq. 3.48:

$$\tau_{n,p(emitter)} = \frac{\tau_{n,p(base)}}{\left[1 + \left(\frac{N}{N_{n,p}}\right)^2\right]} \tag{3.48}$$

where N is the doping density for the highly doped emission layer (cathode or anode), and $N_{n,p}$ is a characteristic parameter for electrons and holes, respectively, dependent both on the material and on the diode manufacturing process. The value of $N_{n,p}$ used in the simulations is $7 \times 10^{16}\ cm^{-3}$. These values regarding the average life of the carriers, a function of the concentration of impurities, help to better define the *Shockley-Read-Hall* recombination model within most 4H-SiC using the following eq. 3.49:

$$R_{SRH} = \frac{pn - n_i^2}{\tau_n \left[n + n_i \exp\left(\frac{E_{trap}}{kT}\right)\right] + \tau_p \left[p + n_i \exp\left(-\frac{E_{trap}}{kT}\right)\right]} \tag{3.49}$$

where n_i is the actual intrinsic concentration of the carriers and E_{trap} is the difference between the energy level trap and the intrinsic level of *Fermi*. In addition to *SRH* recombination, the *Auger* recombination has been considered, calculated with the following model in which the C_p and C_n coefficients must be assigned by eq. 3.50:

$$R_{Auger} = (C_n n + C_p p)\left(np - n_i^2\right) \tag{3.50}$$

3.18 Mobility degradation due to scattering

There are important scattering mechanisms for SiC devices based upon the carrier-carrier scattering and which influences the characteristics of SiC high power devices at

the high current rate. The carrier-carrier contribution to the overall mobility degradation is captured in the mobility term and expressed by the model of Choo [78] which uses the *Conwell-Weisskopf* screening theory [79, 80].

$$\mu_\nu^{\mathrm{cc}} = \frac{D\left(\frac{T_L}{300K}\right)^{\frac{3}{2}}}{\sqrt{n \cdot p}} \cdot \left[\ln\left(1 + F \cdot \left(\frac{T_L}{300K}\right)^2 \cdot (p \cdot n)^{-\frac{1}{3}}\right)\right] \tag{3.51}$$

With $\nu = n, p$, where n and p are the electron and hole densities, respectively. The fitting parameter $D = 6.9 \times 10^{20}$ $[cm \cdot V \cdot s]^{-1}$ and $D = 3.045 \times 10^{20}$ $[cm \cdot V \cdot s]^{-1}$ for 4H-SiC and 6H-SiC, respectively, and $F = 7.452 \times 10^{13}$ cm^{-2} [81].

Similarly, the physical mechanisms at MOS interfaces in SiC are not well understood. However, it is necessary to account for reduced channel mobilities in real MOS devices. Surface scattering is modelled by the following empirical expression [81]:

$$\mu_\nu^{\mathrm{surf}} = \frac{\mu_\nu^{\mathrm{ref}} + \left(\mu_\nu^{low} - \mu_\nu^{\mathrm{ref}}\right) \cdot (1 - F(y))}{1 + F(y) \cdot \left(\frac{S_\nu}{S_\nu^{\mathrm{ref}}}\right)^{\gamma_\nu^2}} \tag{3.52}$$

$$\mu_\nu^{\mathrm{ref}} = \mu_{\nu,300}^{\mathrm{ref}} \cdot \left(\frac{T_L}{300K}\right)^{-\gamma_\nu^3} \tag{3.53}$$

The function $F(y)$ (depend on the surface distance Y) and describes a smooth transition between the surface and bulk, given by:

$$F(y) = \frac{2 \cdot \exp\left(-\left(\frac{y}{y^{ref}}\right)^2\right)}{1 + \exp\left(-2 \cdot \left(\frac{y}{y^{ref}}\right)^2\right)} \tag{3.54}$$

where the parameter y^{ref} describes a critical length. The pressing forces S_n and S_p are equal to the magnitude of the normal field strength at the interface if the carriers are attracted by the interface, otherwise, zero, and γ_ν^μ specifies how the undoped mobility changes due to lattice scattering.

Mobility degradation at MOS interfaces can also be modelled using a surface mobility model which incorporates an empirical model that combines mobility expressions for semiconductor-insulator interfaces and for bulk. The basic equation is given by *Matthiessen's rule*:

$$\mu_\nu^{tot} = \left(\frac{1}{\mu_\nu^b} + \frac{1}{\mu_\nu^{ac}} + \frac{1}{\mu_\nu^{sr}}\right)^{-1} \tag{3.55}$$

In this expression, μ_ν^{tot} is the total electron or hole mobility accounting for surface effects, μ_ν^{ac} is the mobility degraded by surface acoustical phonon scattering, μ_ν^{b} is the mobility in bulk, and μ_ν^{sr} denotes the mobility degraded by surface roughness scattering. The bulk mobility μ_b is computed through the empirical expression for the doping dependence of the low-field mobility is the *Caughey-Thomas* equation, Eq. 3.55. The two surface contributions can be modelled using the model of Lombardi et al. [82]:

$$\mu_\nu^{ac} = \frac{B_\nu}{E_{\perp,\nu}} + C_\nu \cdot \left(\frac{N_D + N_A}{N_\nu^{ref}}\right)^{\alpha_\nu^\mu} \cdot \left[\sqrt[3]{E_{\perp,\nu}} \cdot \left(\frac{T_L}{300K}\right)\right]^{-1} \tag{3.56}$$

$$\mu_\nu^{sr} = \frac{D_\nu}{E_{\perp,\nu}^2} \tag{3.57}$$

where B, C, D are fitting parameters, and $E_\perp$ is the component of the electric field normal to SiO_2/SiC interface.

3.19 4H-SiC MOSFET mobility model

The extremely high density of occupied interface traps in 4H-SiC MOSFETs required the development of an advanced *Coulomb* scattering mobility model for the device simulator. As the effect of *Coulomb* scattering decreases with increasing distance from the interface, the *Coulomb* mobility was required to have a depth-dependence. As the traps are screened by the mobile electrons, it was necessary to put in a screening model for the *Coulomb* scattering. In addition to the *Coulomb* scattering mobility, the bulk mobility, surface phonon mobility and surface roughness mobility together give the total low field mobility. The saturation velocity and parallel component of the electric field give the high field mobility. The total mobility is a combination of the low field mobility and the high field mobility [83].

A) Quasi-2D *Coulomb* Scattering Mobility:

To extract the quasi 2D *Coulomb* mobility, we start with a screened *Coulomb* potential:

$$V(\mathbf{r}) = \frac{e^2}{4\pi\bar{\varepsilon}} \cdot \frac{1}{\mathbf{r}} \cdot e^{-r \cdot q_{sc}} \tag{3.58}$$

where, $\bar{\varepsilon}$ is the average permittivity of SiO_2 and 4H-SiC, and q_{sc} is the screening factor.

In order to get the 2D matrix element (H_{2D}) for applying the *Fermi* Golden Rule, we first take the 3D *Fourier* Transform of the Coulomb potential eq. 3.59 and then take its 1D inverse transform eq. 3.60.

$$H_{3D} = \left\langle e^{-i\mathbf{k}\cdot\mathbf{r}} \left| V(\mathbf{r}) \right| e^{i\mathbf{k}\cdot\mathbf{r}} \right\rangle = \frac{e^2}{\bar{\varepsilon}} \cdot \frac{1}{q_{3D}^2 + q_{SC}^2} \tag{3.59}$$

$$H_{2D} = \frac{1}{2\pi} \int_{-\infty}^{\infty} H_{3D} \cdot e^{iz\cdot q_z} dq_z = \frac{e^2}{2\bar{\varepsilon}} \frac{e^{-z\cdot\sqrt{q_{2D}^2+q_{sc}^2}}}{z \cdot \sqrt{q_{2D}^2 + q_{sc}^2}} \tag{3.60}$$

where, q_{3D} and q_{2D} are the 3D and 2D scattering wave-vectors respectively. The scattering rate is obtained by applying the *Fermi* Golden Rule:

$$\Gamma_{\mathbf{k}\to\mathbf{k}'} = \frac{2\pi}{\hbar} \left(\frac{e^2}{2\bar{\varepsilon}} \cdot \frac{e^{-z\cdot\sqrt{q_{2D}^2+q_{sc}^2}}}{z \cdot \sqrt{q_{2D}^2 + q_{sc}^2}} \right) \delta\left(E_{\mathbf{k}} - E_{\mathbf{k}'}\right) \tag{3.61}$$

The scattering charges are of two types. The occupied interface traps which are located at the interface and the fixed oxide charges that are distributed inside the oxide close to the interface. In order to incorporate this distribution of fixed oxide charges, we calculate the scattering rate as a function of both, the distance of the mobile charge from the interface (z) and the distance of the fixed charges from the interface (z_i). At a distance z_i inside the oxide, the total density of charges is given as:

$$N_{2D}(z_i) = \begin{cases} N_{it} + N_f(0)\, for z_i = 0 \\ N_f(z_i)\, for z_i < 0 \end{cases} \tag{3.62}$$

where N_{it} is the occupied interface trap density, and N_f is the fixed oxide charge density. The total quasi 2D scattering rate for a $N_{2D}(z_i)$ density of scattering charges can be written from the *Fermi* Golden Rule as:

$$\frac{1}{\tau(z, z_i)} = \frac{N_{2D}(z_i)}{4\pi^2} \oint k' dk' \oint \Gamma_{\mathbf{k}\to\mathbf{k}'} (1 - \cos\theta) d\theta \tag{3.63}$$

The screened *Coulomb* scattering mobility as a function of depth is obtained from this scattering rate as:

$$\frac{1}{\mu_C(z, z_i, T_e)} = \frac{m^* e^3 N_{2D}(z_i)}{16\pi\bar{\varepsilon}^2 \hbar k_B T_e} \cdot F(z, z_i, T_e) \tag{3.64}$$

where T_e is the effective temperature of the carriers. It has an inherent exponential dependence on the distance between the mobile charge and the scattering charge centre given by the form factor:

$$F(z, z_i, T_e) = \int_{\alpha=0}^{\pi/2} \left(1 - \frac{q_{sc}^2}{\frac{8m^* k_B T_e}{\hbar^2} \sin^2\alpha + q_{sc}^2}\right) \exp \Lambda d\alpha \tag{3.65}$$

where, Λ is:

$$\Lambda = \left[-2\sqrt{\frac{8m^* k_B T_e}{\hbar^2} \sin^2\alpha + q_{sc}^2} (z - z_i)\right] \tag{3.66}$$

The screening factor in the *Coulomb* potential depends on the amount of inversion charge present and also on an average depth of the inversion layer and is given as the inverse of the *Debye* length for semiconductors:

$$q_{sc} = \sqrt{\frac{e^2 N_{inv}}{\varepsilon_{SiC} Z_{av} k_B T_e}} \tag{3.67}$$

In plasmas, the *Debye* length or radius is a measure of a charge carrier's net electrostatic effect in a fluid/gas and how far its electrostatic effect persists. A *Debye* sphere is a volume whose radius is the *Debye* length. With each *Debye* length, charges are increasingly electrically screened. Every *Debye*-length λ_D, the electric potential will decrease in magnitude by $1/e$. The corresponding *Debye* screening wave vector $k_D = 1/\lambda_D$ for particles of density n, charge q at a temperature T is given in Gaussian units by:

$$k_D^2 = \frac{4\pi n q^2}{k_B T} \tag{3.68}$$

For $T \rightarrow 0$ these quantities are known as the *Thomas-Fermi* length and the *Thomas-Fermi* wave vector. They are of interest in describing the behaviour of electrons in metals at room temperature.

Due to screening, *Coulomb* scattering reduces drastically over a short distance when a large number of mobile carriers are present. This method of treating *Coulomb* scattering [83] gives the *Coulomb* mobility for a mobile charge at any location inside the semiconductor.

The *Coulomb* scattering mobility model shows that the scattering rate is directly proportional to the density of occupied interface traps and the fixed charge density at the interface. Hence reducing the interface trap density will reduce *Coulomb* scattering and improve surface mobility. Occupied interface state density decreases with increase in temperature thereby increasing the surface mobility and causing a negative shift in threshold voltage.

B) Total Mobility

In addition to the *Coulomb* scattering mechanism described above, the scattering mechanisms included in calculating the total low field mobility are the surface phonon scattering and surface roughness scattering. The low field mobility is combined with saturation velocity dependent high field mobility by *Matheissen*'s rule, to get the total mobility.

3.19.1 *Coulomb* interaction

Modelling the intrinsically 3D *Coulomb* interaction by a 2D simulation requires some care to conserve the main physical features of the system. Screening must be accounted for first. In a non-degenerate situation, we can think of screening as an exponential decay of the effective interaction potential, according to the space-dependent screening factor:

$$q_{sc}^{-2} = \frac{\varepsilon\left(k_B T_e/e\right)}{n \cdot e} \tag{3.69}$$

where T_e is the effective temperature of the carriers and n is their concentration.

Screening is the damping of electric fields caused by the presence of mobile charge carriers. It is an important part of the behaviour of charge-carrying fluids, such as ionized gases (classical plasmas) and conduction electrons in metals. In a fluid composed of electrically charged constituent particles, each pair of particles interact through the *Coulomb* force:

$$\mathbf{F} = \frac{q_1 q_2}{4\pi\varepsilon_0 |\mathbf{r}|^2}\hat{r} \tag{3.70}$$

In reality, these long-range effects are suppressed by the flow of the fluid particles in response to electric fields. This flow reduces the effective interaction between particles to a short-range "screened" *Coulomb* interaction. For example, consider a fluid composed of electrons, where each electron possesses an electric field which repels other electrons. As a result, it is surrounded by a region in which the density of electrons is lower than usual. This region can be treated as a positively-charged "screening hole". Viewed from a large distance, this screening hole has the effect of an overlaid positive charge which cancels the electric field produced by the electron. Only at short distances, inside the hole region, can the electron's field be detected [84]. The first theoretical treatment of screening, due to *Debye* and *Hückel* (1923), dealt with a stationary point charge embedded in a fluid. This is known as electrostatic screening.

The general idea is to separate *Coulomb* interaction into two classes:

Short-range *Coulomb* interaction.

This occurs within a screening length. Since the wave packets representing the electrons can be assumed as overlapping, a simple space homogeneous theory based on *Bloch* functions can be used to estimate the scattering rate for a given electron concentration. Given the average electron density, it is possible to simulate the 3D scattering probability per unit time. Screening of the *Coulomb* perturbation potential is included in the calculation if necessary. Electron-electron scattering is applied to carriers within a screening length in the 2D simulation. The effect of short-range interaction is an exchange of energy between carriers, and the position of the particles is not changed. Therefore, the potential energy remains constant and ensemble modes are not affected.

Long-range *Coulomb* interaction.

We can assume that beyond a few screening lengths, no interaction between single carriers occurs. Carrier-carrier is ineffective on these length scales because screening attenuates exponentially the mutual force. But, the perturbation has a large effect on the entire ensemble of carriers. In other words, beyond a screening length the individual carrier no longer sees other isolated carriers but rather a plasma. The long-range interaction is thus basically an exchange of energy between a single carrier and the particle-field ensemble system. With the Atlas simulator it is possible to model the cut-off between short-range and long-range interactions by choosing a *Poisson*-mesh spacing equal to the local screening length [85].

3.20 Some consideration on high doping effects

The degeneration process of mobility, associated with the high density of carriers, can be within certain limits considered as a possible consequence of high doping. Other phenomena related to high levels of doping are the forbidden band restriction and the associated phenomenon of the band queue (band tailing). Both phenomena are the effect of high dopant concentration associated with the *Coulomb* interaction with the carriers, no longer negligible at high concentrations. The effect of concentration of a donor level is simple: a donor atom introduces, at low concentration, a discrete band energy level in the forbidden band [86], [87]. If donor concentration increases in such a way that, the average distance between neighbouring donor atoms becomes relatively low, the probability amplitudes of the electronic levels associated with neighbouring donor atoms interfere, giving rise to a sub-band placed in the forbidden band near the conduction band. This sub-band tends to merge with the conduction band because

the *Coulomb* interaction between electrons (holes) produces a change in the density profile of the states near the beginning of the conduction band (valence). The doping induced energy shifts of the lowest conduction band minimum and the uppermost valence band maximum has been calculated for both n-type and p-type 3C-SiC, 4H-SiC, 6H-SiC, and Silicon.

In non-degenerate semiconductor has been assumed that the electron or hole concentration is much lower than the effective density of states in the conduction band or the valence band, respectively. Therefore, the *Fermi* level have to be at least $3kT$ above E_V or $3kT$ below E_C:

$$E_V + 3kT < E_F < E_C - 3kT$$

In such cases, the semiconductor is referred to as a non-degenerate semiconductor. For shallow donors in n-type Silicon there is enough thermal energy to supply the energy E_D to ionize all donor impurities at room temperature and thus provide the same number of electrons in the conduction band. This condition is called complete ionization. Under a complete ionization condition, we can write the electron density n as:

$$n = N_D \tag{3.71}$$

where N_D is the donor concentration.

Figure 3.29-(a) [88] illustrates complete ionization where the donor level E_D is measured with respect to the bottom of the conduction band and equal concentrations of electrons (which are mobile) and donor ions (which are immobile) are shown.

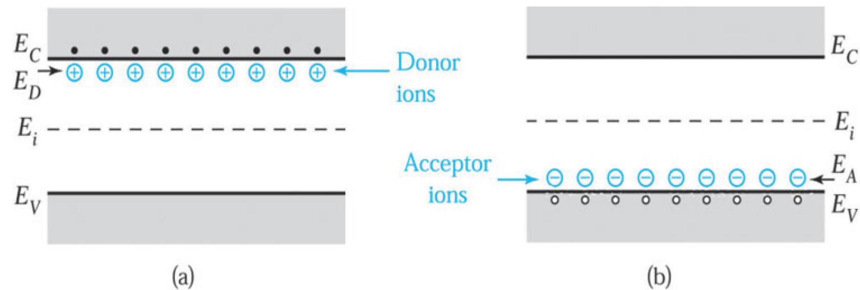

Fig. 3.29. Schematic energy band representation of extrinsic semiconductors with (a) donor ions and (b) acceptor ions.

The *Fermi* level in terms of the effective density of states N_C and the donor concentration N_D is given by [88]:

$$E_C - E_F = kT \cdot \ln\left(\frac{N_C}{N_D}\right) \tag{3.72}$$

Similarly, for shallow acceptors for p-type semiconductors as shown in Fig. 3.29-(b) [88], if there is complete ionization, the concentration of holes is given by:

$$p = N_A \tag{3.73}$$

where N_A is the acceptor concentration.

The corresponding *Fermi* level is given by [88]:

$$E_F - E_V = kT \cdot \ln\left(\frac{N_V}{N_A}\right) \tag{3.74}$$

From Eq. 3.72 we can see that the higher the donor concentration, the smaller the energy difference ($E_C - E_F$); that is, the *Fermi* level will move closer to the bottom of the conduction band. Similarly, for higher acceptor concentration, the *Fermi* level will move closer to the top of the valence band. Figure 3.30 [88] illustrates the procedure for obtaining the carrier concentrations for an n-type semiconductor [6].

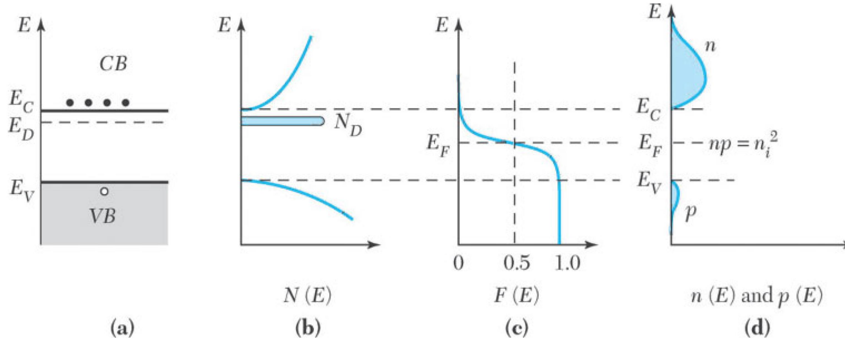

Fig. 3.30. n-Type semiconductor. (a) Schematic band diagram. (b) Density of states. (c) *Fermi* distribution function. (d) Carrier concentration.

According to the *Kane model* the density of states has an exponential tail for energies below E_C (or higher than E_V for the valence band). The trend of the band tail for the density of the electron states is of the type [89]:

$$dN_{cc} = \alpha \exp\left(\beta \cdot \frac{E - E_C}{k_B T}\right) dE \tag{3.75}$$

where α and β are appropriate constants. The same model applies to the bandwidth of the density of the states in the valence band, dN_{vc}/dE. Ultimately, therefore, the bandwidth (which is prolonged by about $k_B T$) connects the band of conduction or valence with sub-bands of donors or acceptors; the end result is for an (n-type material), shown in Fig. 3.30, is the restriction of the forbidden band.

[6] Note that $np = n_i^2$

In the case of strong doping $N > 10^{17}\ cm^{-3}$, the electron and hole related energy bands will be displaced equally each other (bandgap narrowing). This effect leads to a decrease in the energy bandgap value and consequently affects also parameters that are dependent of the bandgap. Thus, result that for small changes in the bandgap its reduction is given by [23]:

$$\Delta E_G = \frac{3q^2}{16\pi\varepsilon_S}\sqrt{\frac{q^2 N_D}{\varepsilon_S kT}} \tag{3.76}$$

where ΔE_G is the bandgap reduction due to the combined effects of impurity band formation, band tailing, and screening of minority carriers. The higher values of pn arising from bandgap narrowing are related to the smaller energy bandgap by:

$$n_{ie}^2 = n_i^2 \cdot \exp\left(\frac{q\Delta E_G}{kT}\right) \tag{3.77}$$

where the $p \cdot n$ product can be represented by an effective intrinsic carrier concentration in a manner similar to that for lightly doped semiconductors:

$$n \cdot p = n_{ie}^2 \tag{3.78}$$

The decrease of the energy gap for SiC at room temperature due to high doping concentrations as predicted by the above theory is shown in Fig. 3.31 [73].

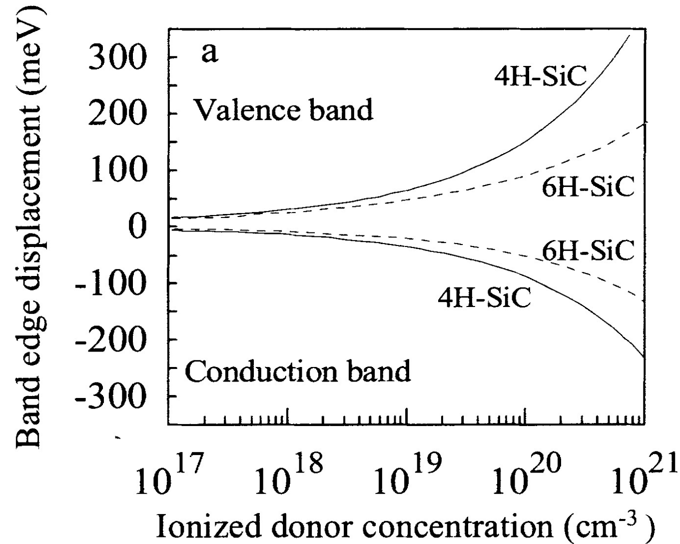

Fig. 3.31. Bandgap narrowing in SiC at high doping concentrations.

3.21 Consideration on robustness

The power semiconductor devices available on the market have intrinsic limits of performance and, during its operating life-cycle, they are subjects to deleterious wear. Robustness and reliability are two important parameters that chipmakers try to improve their products. But, before going further into these things, it is important to give a brief definition of these parameters. The robustness, also known as ruggedness, of a power device, refers to its capability to operate beyond its normal conditions and its device specifications. To evaluate the robustness of a power device means to verify that the device is capable to perform its task test with sufficient safety margins (i.e. robustness margins) between specification limits and one or more failure mechanisms in a defined application [90].

In Fig.3.32 is shown the device specifications of two generic parameters, i.e. "A" and "B", have been schematically represented with a yellow ellipse which contains the application requirements (depicted by means of a full-filled orange ellipse).

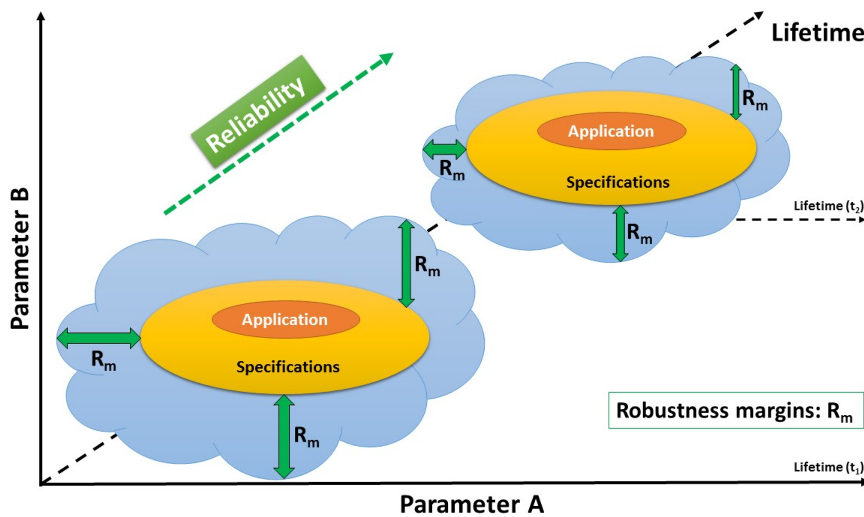

Fig. 3.32. Schematic representation of both reliability and robustness. The usage of the device determines the shrinking of its robustness margins and, consequently, a lower reliability during its lifetime.

Beyond its robustness margin (R_m), the device may fail due to a certain failure mechanism. Reliability, instead, is defined as "the probability of a device to perform a required function under given conditions for the expected lifetime" [90]. The usage of the product in its lifetime within a specified application may eventually affect both its margins of robustness and eventually, its specifications. Contrary to the definition

of robustness, the reliability is not an intrinsic property of the power device, but it is rather related to the application requirements. Thence, to validate the reliability means to verify that the device is capable to work properly inside the specified lifetime conditions.

Practically, both the reliability and the robustness of power devices are experimentally evaluated by chipmakers. In case of reliability estimations, repetitive tests help to predict the lifetime of the device by means of opportune statistical analyses, which returns important information on both failure and degradation mechanisms that helps semiconductor manufacturers to improve their products and to provide accurate product specifications, i.e. datasheets, useful for their custom applications.

Results of robustness can be represented with the diagrams of robustness, as shown in Fig.3.32 which provides a pictorial representation for two parameters, A and B, such as voltage and temperature. The light-blue area represents "the capabilities of the device" for real performance. The yellow area represents the application's specification, which the device must meet or exceed. The robustness margin is the distance between any specification and the point of failure of the device; this parameter takes into account all variations of the device's performance and of the application's environment. The failure could result in different failure modes X, Y, Z, depending on the values of the parameters "A" and "B". A robust device is a component able to maintain all characteristics when subjected to intensive use and at its limit conditions over the life-cycle without manifest any degradation and out-of-spec values.

3.22 Consideration on reliability of SiC power MOSFETs

The following section covers some aspects of SiC power MOSFETs reliability. The aspects considered here do not cover every failure mode of the SiC-MOSFETs.

- **Reliability of the gate-insulating layer**
  As oxide is used as a gate insulating layer in SiC power MOSFETs, its reliability directly affects the reliability of the device. However, by a combination of an appropriate oxide growth process and device structure, a high-quality oxide can be achieved. Chipmakers as Rohm and Cree (Wolfspeed) claimed that their oxide layer is reliable as those grown for Silicon MOSFETs [91]. The assessed lifetime for a gate-source voltage of 20 V is ten million hours (Cree/Wolfspeed). However, even with a high-quality gate insulating layer, there might still remain crystal defects that may cause initial failure.

- **Ruggedness**

  The ruggedness of SiC-MOSFETs against surge currents may partly be dependent on the ability of the gate oxide to withstand high temperatures. In [92] was shown that the location of the hot-spot during a short-circuit fault is extremely close to the gate oxide. For that reason, it is relevant to ensure that the gate oxide of SiC-MOSFETs is resistant to high temperatures.

- **Stability of the gate threshold voltage**

  When a continuous positive gate bias is applied for an extended period of time, electrons can be trapped at the interface between the layer of gate oxide and SiC body. This mechanism tends to increases the threshold voltage. Once the traps are filled, the threshold is fixed. When a continuous negative bias is applied to the gate for an extended period of time the threshold voltage drops due to trapped holes. However, in normal operation, as the gate voltage alternates between positive and negative bias, charges and discharges make it unlikely to obtain any significant changes in the threshold [93].

- **Reliability of body diodes**

  The reliability of the SiC-MOSFET is known to be affected by the degradation caused by the conduction of its body diode [94]. If the forward current is continuously applied to the body diode, a crystal defect called stacking fault could be formed due to the hole-electron recombination energy.

  These faults progressively block the current path which determines an increase of the ON-state resistance as well as an increase of the forward voltage of the body diode. An increment of the leakage current in blocking mode is also observed [95]. The increased forward losses and blocking losses affect the thermal design. Moreover, there is also a correlation between the degradation of the body diode and an increase of R_{ON}. For these reasons, for particular circuit topologies where the body diode conducts a significant current, it is important to use a device free from stacking faults.

- **Short-circuit ruggedness**

  The short-circuit capability of SiC-MOSFET devices has been widely discussed in [96]. The reported reason for failure is that the device reaches local temperatures beyond the melting point of aluminium. However, the short-circuit robustness might also depend on the manufacturer and the fabrication process of the devices. It is also reported that the failure is due to gate failure or gate weakness since the gate leakage current increases just before the failure, which is probably due

to the heat spreading in the device which may lead to the destruction of the gate oxide. Finally, the short-circuit robustness is dependent on the gate voltage and the voltage across the device during a short-circuit event. Even though short-circuit robustness of SiC devices has been widely documented, very little has been done on SiC-MOSFET protection against short-circuit failure. The degradations observed determine an increase of the ON-state resistance and of the gate leakage current.

- **Over-voltage capability**

  The failure modes of the SiC-MOSFET under avalanche conditions are due to a current failure due to the biasing of the parasitic NPN BJT transistor, localized impact ionization, or temperature failure due to thermal runaway. The voltage required to trigger the NPN BJT transistor is of 3 V for SiC-MOSFETs (0.7 V for Silicon). This voltage decreases with an increase of temperature by 2 mV/K [97]. Moreover, voltage tests have shown that the SiC-MOSFET is very rugged and is able to sustain high avalanche currents.

The reliability of SiC power devices is excellent and has continued to improve due to continuing advancements in SiC substrate quality, epitaxial growth capabilities, and device processing [98]. This has promoted the development of SiC power device and their use in different fields of application such as energy, transportation and industrial. The SiC MOSFET employs gate dielectric, polysilicon gate, Aluminium overlayer, and source ohmic contacts, similar to traditional Silicon power devices. Main critical points for reliability are the edge termination design, dielectric and wafer processing. It is fundamental for the SiC epitaxial layer to have a low defect density and appropriate doping and thickness in order to achieve the target reliability and device performance. The MOSFET area that is needed to achieve a given device resistance is determined primarily by the channel and drift resistances. The MOS channel inversion-layer mobility needs to be high, and this needs to be supported by a very reliable gate dielectric. High voltage and ON-state current produce localized heating (hot-spots) and temperature gradients at the wire bond interfaces; the devices then cool only when it switching OFF. This can then wear out and break the device due to thermo-mechanical stress.

Part II

Physical Modelling and Numerical Simulations

4

POWER VD-MOSFET in 4H-SiC: DESIGN, MODELLING and NUMERICAL CHARACTERIZATION

> Perfection is achieved, not when there is nothing more to add, but when there is nothing left to take away.
>
> Antoine de Saint-Exupery

4.1 Introduction

POWER DEVICES are required in a huge number of applications that can be classified into several categories. Among these, there is the class of devices designed to work at relatively small operating voltages, typically lower than 200 V. For these applications, Silicon power MOSFETs generally offer very good performances thanks to their low ON-state resistance and fast switching speeds. However, there are application fields where higher efficiencies and better ruggedness, compared to Silicon, would be beneficial. Examples are those cases where a power electronic circuitry is part of an apparatus with an expected long lifetime, say 20 years or more, which is moreover designed for operating in a harsh, unattended environment. Electronic circuits matched to photovoltaic modules (e.g. onboard, or on-module, DC-DC converters) belong to this category, as these modules are planned to remain operative and efficient for at least 20 years, even under hot weather conditions. Given the conversion efficiency constraints in these applications, the deployment of energy-hungry and mechanically unreliable cooling fans would be moreover unacceptable to industry [99]. Nowadays trend in photovoltaic (PV) components research considers the integration of modules with an onboard electronic circuit, a Smart Maximum Power Point Tracking (SMPPT) DC-DC converter, generally rated for voltages and currents respectively below 100 V and 10 A, providing the best match between the I-V characteristics of a single PV module and the downstream electronics [100–103]. As good

quality solar modules are generally designed to remain fully functional for 25 years in all operating conditions, the onboard electronics is expected to perform at least the same life expectations. Reaching this goal is not trivial since SMPPT converters operate in stressing and continuously changing conditions, moreover relaying on basic measures for their thermal control. The choice of suitable SMPPT topology and components is, therefore, a crucial task for designers [104–107]. In particular, the power switching devices, generally MOSFETs, must be highly efficient and rugged to meet the design targets. MOSFETs made in SiC, a semiconductor with excellent physical properties such as a high critical electric field E_{cr}, mechanical strength, and high thermal conductivity [34], have gained wide popularity in high power electronics, also for their reliability. In recent years, they have been widely used in DC-DC converters developed for different application fields [108–113]. Commercial SiC MOSFETs are currently fabricated with blocking voltages BV_{DS} in the range from 600 to 1700 V [114–116]. They provide notably good performances for which it is worth paying more, at least compared to those of their less expensive Silicon counterparts. On the other hand, for a lower BV_{DS} devices, SiC loses in part its advantages. For example, in a semiconductor p-i-n structure with given doping of the i-layer, the breakdown voltage basically scales with E_{cr}^2 [23], and therefore the lower the desired breakdown voltage, the weaker its dependence on E_{cr}. This means that in low voltage devices, only a little improvement in the blocking capabilities results from the use of SiC instead of Silicon. Therefore, as the higher blocking capabilities of SiC are usually traded off for thinner i-layers and consequent lower ON-state resistance, it follows in turn that moderate improvements can be expected for the ON-state characteristics of low voltage SiC devices. In addition, the latter present costs that, at least to date, make them not convenient to circuit designers and producers. SiC devices, however, confer robustness on circuits, also in stressing environments. This feature might be worth exploiting also in lower voltage applications, like in SMPPT, for which efficiency, miniaturization, and temperature control represent critical targets. This work is therefore addressed at predicting the characteristics of 4H-SiC MOSFETs designed for PV power switching converters, for which preliminary results on static characteristics were previously presented [99]. In particular, the design specifications refer to a transistor with a breakdown (or blocking) voltage, $BV_{DS} = 150\ V$. The attention is focused on the ON-state resistance (R_{ON}), the switch-on gate charge (Q_g), and the switching times to verify their fitness to the specific application. The device was studied by a TCAD 2D physical simulator.

4.2 A brief introduction to Silvaco ATLAS software for numerical simulations

Atlas provides general capabilities for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices. Atlas is a physically-based device simulator. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three-dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid you can simulate the transport of carriers through a structure. This means that the electrical performance of a device can now be modelled in DC, AC or transient modes of operation.

Physically-based simulation is different from empirical modelling. The goal of empirical modelling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight or predictive capabilities, or encapsulation of theoretical knowledge. Physically-based simulation has become very important for two reasons. One, it is almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult or impossible to measure. The drawbacks of physically-based simulations are that all the relevant physical models must be incorporated into a simulator. Also, numerical procedures must be implemented to solve the associated equations. These tasks have been taken care of for Atlas users. Those who use physically-based device simulation tools must specify the problem to be simulated. In Atlas, specify device simulation problems by defining:

- The physical structure to be simulated.
- The physical models to be used.
- The bias conditions for which electrical characteristics are to be simulated.

Figure 4.1 readapted from the original [72] shows the types of information that flow in and out of Atlas. Most Atlas simulations use two input files. The first input file is a text file that contains commands for Atlas to execute. The second input file is a structure file that defines the structure that will be simulated. Atlas produces three types of output files. The first type of output file is the run-time output, which gives you the progress and the error and warning messages as the simulation proceeds. The second type of output file is the log file, which stores all terminal voltages and currents from the device analysis. The third type of output file is the solution file,

which stores 2D and 3D data relating to the values of solution variables within the device at a given bias point.

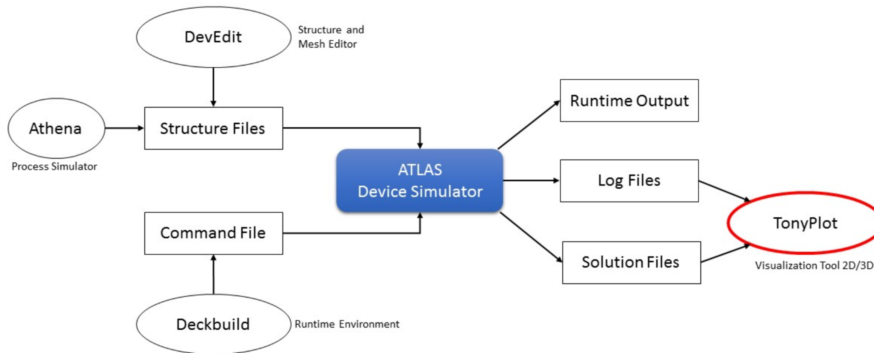

Fig. 4.1. Atlas Inputs and Outputs.

Thus, after having constructed the geometry of the device to be simulated, the code for the simulations is constructed. In our case, it is possible to implement any physical model of semiconductor physics simply by programming the input card to the simulator, and of course, supplying all the parameters of the relative equations discretized in the closed model of ATLAS.

4.3 Device structure

The schematic cross-section of the 4H-SiC MOSFET elementary half-cell considered in this study is shown in Fig. 4.2. Although simplified for simulation purposes, the proposed geometry is in principle compatible with a manufacturing process based on doping by ion implantation [77, 117, 118].

Seven regions can be identified in the designed device structure.

- Region-1 is a heavily nitrogen-doped N^+ and constitutes the drain of the MOSFET. It coincides with the 4H SiC substrate on which the drift region of the final device is grown by epitaxy. Substrates are generally produced with a thickness of 350 μm. However, before realizing the bottom contact, they are thinned down to 100–150 μm to cut the resistance and improve heat exchange. It was therefore considered a thickness $W_{sub} = 100\ \mu m$.

- Region-2 is the nitrogen-doped drift epitaxial N-layer, with thickness W_{drift}. Doping concentrations for drift regions (N_{epi}) in SiC MOSFETs are generally in the range 5×10^{15} to 10^{16} cm^{-3} [77, 117, 118]. By adapting to our $P - N_{epi} - N_{sub}^{+}$ structure the well-known formula valid for abrupt junction p-i-n devices that show breakdown in punch-through conditions [23]:

$$BV_{DS} = E_{cr} W_{drift}^{'} - \frac{qN_{epi}\left(W_{drift}^{'}\right)}{2\varepsilon_s} \tag{4.1}$$

  where E_{cr} is the critical electric field, q is the electron charge, and εs is the semiconductor dielectric constant, it follows that the lower is the desired breakdown voltage BV_{DS}, the higher can be the drift layer doping N_{epi}, with consequent advantages in terms of low ON-state resistance. Given the specified voltage ratings, the N_{epi} is set to 10^{16} cm^{-3} for the simulations.
- Region-3 is the aluminium-doped (10^{17} cm^{-3}) p-base; this region contains the actual MOS structure and the device channel, which is set to $L_{ch} = 1$ μm, just below the gate oxide.
- Region-4 is the phosphorous-doped (10^{18} cm^{-3}) source region.
- Region-5 of the MOS structure is made of Silicon oxide.
- Region-6 forms the source contact, shorting moreover the source and base regions to prevent the switch-ON of the parasitic NPN "substrate(n+)-epilayer(n)-base(p)–source(n+)" bipolar junction transistor.
- Region-7 is the gate contact.

  The geometrical parameters and doping concentrations of the different MOSFET regions are summarized in Table 4.1. The half-cell of Fig.4.2 has a length (X-direction) of 6.5 μm, while the width (Z-direction) is 1.0 μm by default. The drain contact area is therefore 6.5 μm^2, the source contact area is 1.8 μm^2 and the gate contact area is 3.4 μm^2.

The distance between the p-base regions, W_j, was set to 5.0 μm, while the W_{drift} thickness (Y direction) of 1.8 μm was chosen to meet the required MOSFET specification in terms of $BV_{DS} = 150$ V.

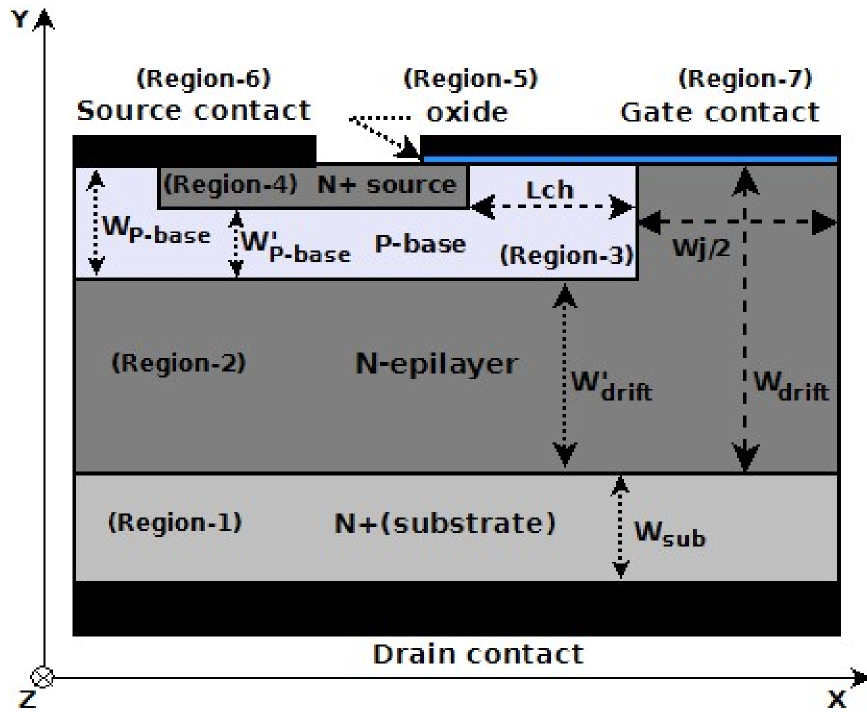

Fig. 4.2. Schematic cross-sectional view of the MOSFET half-cell. The drawing is not in scale.

Table 4.1. MOSFET Structure.

PARAMETER	**UNIT**	**VALUE**
Silicon oxide thickness	μm	0.08
Source thickness	μm	0.50
Channel length, L_{ch}	μm	1.00
Base junction depth, W_{P-base}	μm	1.30
Interspace, W'_{P-base}	μm	1.00
Distance between the base regions, W_j	μm	5.00
Epilayer junction depth, W_{drift}	μm	1.80
Base-to-substrate distance, W'_{drift}	μm	0.50
Substrate thickness, W_{sub}	μm	100.00
Device footprint area	μm^2	6.50
N^+-source doping	cm^{-3}	10^{18}
P-base doping	cm^{-3}	10^{17}
N-epilayer doping	cm^{-3}	10^{16}

4.4 Blocking voltage characteristics

A first set of simulations was performed in order to assess the dependence of BV_{DS} on the epitaxial region thickness (region-2 in Fig.4.2). With the device in the OFF-state ($V_G = 0\ V$) and grounded source, V_{DS} was gradually raised up to the occurrence of a critical electric field $E_{cr} = 1.9 \times 10^6\ V/cm$ somewhere along the border of the P-base/N-epilayer junction. Under these bias conditions, no channel is formed under the gate at the surface of the P-base region, and the P-base/W$_{drift}$ junction is reverse-biased to sustain the positive drain voltages. However, despite the short-circuiting of the N^+ source and P-base region, the drain leakage current I_{leak}, which remains below any practically detectable value ($J_D < 10^{17}\ \mu A/\mu m^2$) until E_{cr} is under 1.9×10^6 V/cm, suddenly rises up to 70 $\mu A/\mu m^2$ as soon as the depletion layer in the P base punches through the source. The electric field and drain current behaviours are shown in Fig. 4.3 as a function of the drain voltage for two devices with different W_{drift} thicknesses, namely $W_{drift,1} = 5.0\ \mu m$, and $W_{drift,2} = 1.8\ \mu m$. In particular, the $W_{drift,2} = 1.8\ \mu m$ device was identified as the minimum thickness able to support the $BV_{DS} = 150\ V$. In Table 4.1 are reported the main parameters for designed MOSFET. More detail about Eq. 4.1 are reported in [119].

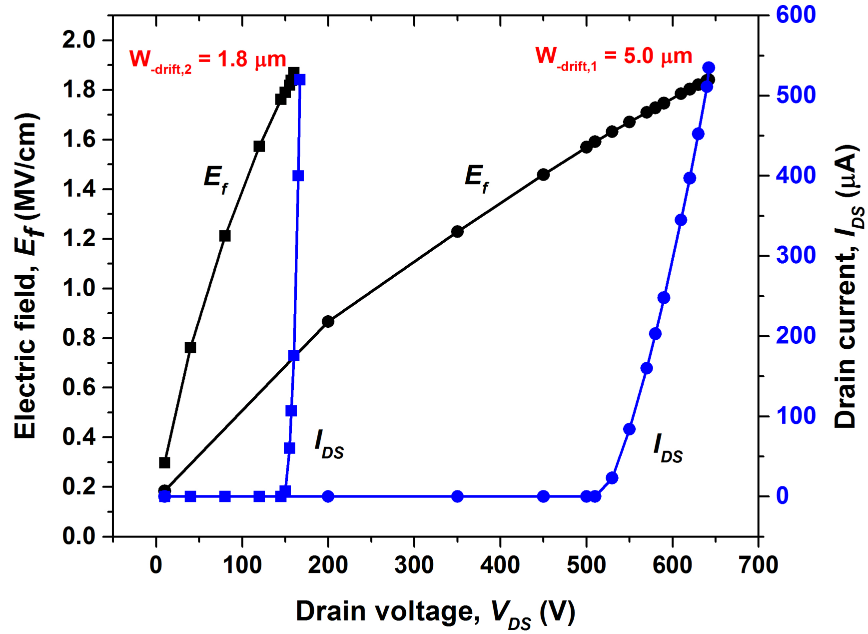

Fig. 4.3. Electric field (black curve) and drain current (blue curve) as a function of the drain bias for two devices with different W_{drift}. The reported electric field is the highest measured along the border of the P-base/N-epilayer junction (see Fig. 4.2).

A detailed analysis of the MOSFET BV_{DS} behaviour vs. W_{drift} is illustrated in Fig.4.4.

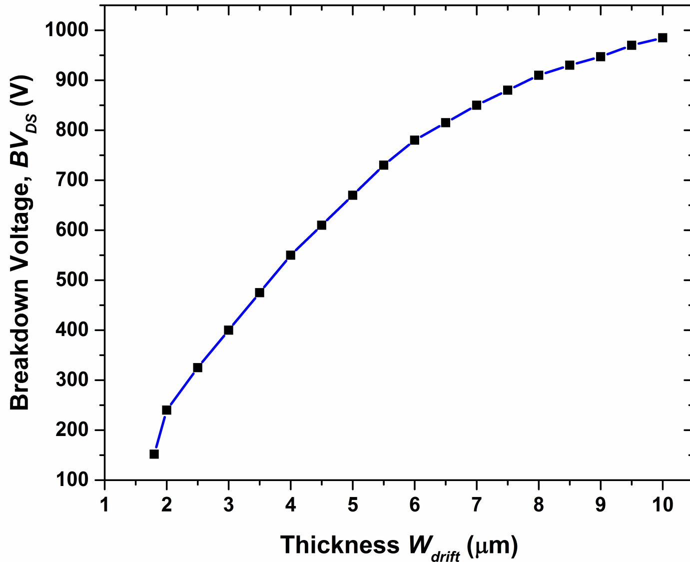

Fig. 4.4. MOSFET breakdown voltage as a function of W_{drift}.

4.5 ON-state analysis

The current density-voltage ($J_D - V_{DS}$) output characteristics for the designed device with an epilayer thickness of $W_{drift} = 1.8\ \mu m$ was evaluated within the triode region, are shown in Fig. 4.5 for $V_{GS} = 7 \div 20\ V$; the geometrical and electrical parameters of the device are those listed in Table 4.1.

The existence of contact resistances was also considered for these device. Indeed, assuming for both the p-type and n-type contacts a specific contact resistance of $R_{contact} \approx 10^{-6}\ \Omega \times cm^2$ [120, 121], result that the device has a footprint $= 1\ \mu m^2$, with the following contacts resistance of $R_G = 176\ \Omega$, $R_S = 325\ \Omega$, and $R_D = 100\ \Omega$.

The device turns-ON for a $V_{GS} \approx 8\ V$, which we can assume to be its threshold voltage V_{TH}. At this regime, the resistive path established for electrons flowing from the source contact to drain is characterized by an R_{ON} resistance determined by various terms, namely[1]:

[1] In section on physical model the equation of ON-state resistance has been defined with uppercase-subscripts for each component. A part this variation of text, the single component are the same. I left this apparent difference only to respect the original sources

$$R_{ON} = R_{n+} + R_{ch} + R_a + R_j + R_d + R_b \quad (4.2)$$

where:

- R_{n+} is the source resistance.
- R_{ch} is the channel resistance.
- R_a is the resistance of the accumulation region relative to the distance $W_j/2$ (see Fig. 4.2).
- R_j is the resistance of the depletion layer between the P-base and the N-epilayer region.
- R_d is the resistance of the drift region.
- R_b is the drain resistance.

They are thus classified:

- R_{n+} and R_b can be considered negligible because they are localized in heavily doped regions.
- R_{ch} and R_a mainly depend on the gate bias level.
- R_j and R_d are determined by the geometry and doping level of the W_{drift} region.

Assuming an operating point in the triode region. For $V_{GS} = 16\ V$ and $V_{DS} = 1\ V$ result $J_D \approx 10\ \mu A/\mu m^2$, at this point corresponds to an $R_{ON} = 100\ k\Omega \times \mu m^2$. Thus, has been calculated the R_{ON} for different V_{DS} as a function of V_{GS}, Fig. 4.6.

Instead, the Fig. 4.7 shows the R_{ON} behaviour vs. V_{GS} at $V_{DS} = 1V$ for four different values of thickness $W_j/2$ (see Fig. 4.2). From this plot it is clear that a $W_j/2 = 2.5\ \mu m$ represents a good trade-off for the $V_{GS} \geq 16\ V$.

Further simulation has been done to evaluate the channel length impact on the electrical characteristics. Was observed that changing the channel length as $L_{ch} = 1 \pm 0.2\ \mu m$ results that this parameter has a limited impact on the device ON-state current capabilities, more precisely in full ON-state, and taking as reference $L_{ch} = 1\ \mu m$ results the variation reported in Table 4.2.

Table 4.2. MOSFET ON-STATE RESISTANCE VS. CHANNEL LENGTH.

$\mathbf{R_{ON}}$	$\mathbf{L_{ch}}$	$\Delta\ \mathbf{R_{ON}}\%$
R_{ON}	1.0 μm	ref. value
R_{ON}	0.8 μm	≈-5%
R_{ON}	1.2 μm	≈+5%

From the Table 4.2, result that R_{ON} approximately decreases (increases) by a factor of 5% for the channel length variation of $\pm 0.2\ \mu m$.

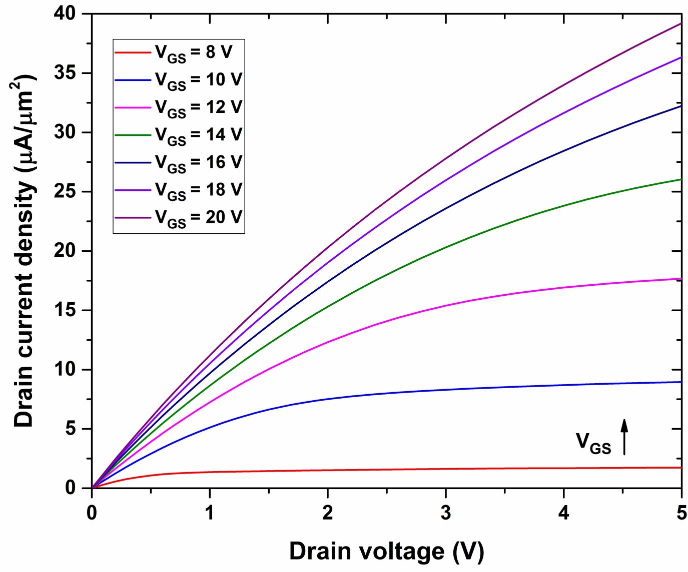

Fig. 4.5. Forward $J_D - V_{DS}$ characteristics.

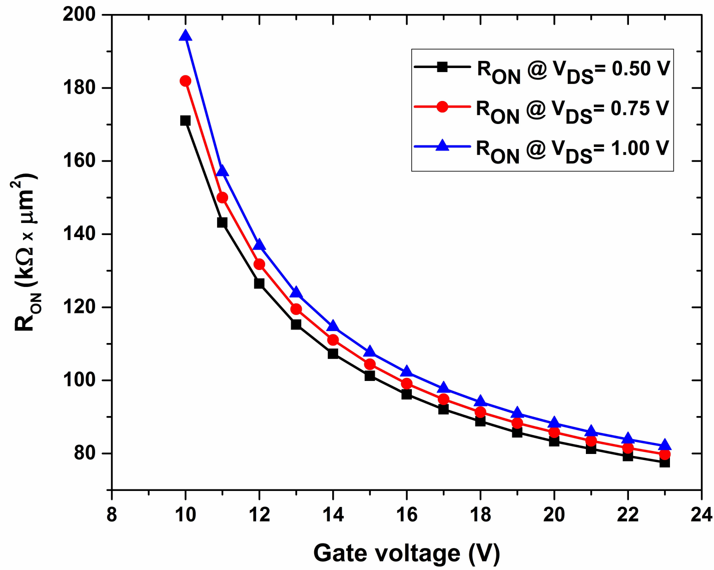

Fig. 4.6. R_{ON} as a function of V_{GS} at different drain voltage levels.

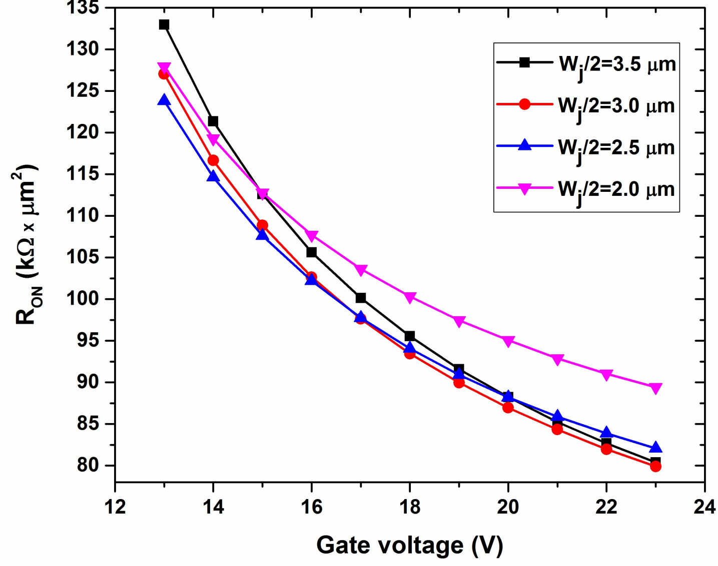

Fig. 4.7. R_{ON} as a function of V_{GS} for different values of $Wj/2$ at $V_{DS} = 1\ V$.

4.6 Simulation setup and comparison with experimental data

The prediction capabilities of the simulation setup described above were tested by comparison with experimental data. In particular, simulations of a commercial class 900 V SiC MOSFET [115] were performed, starting from the same device topology of Fig. 4.2. In order to circumvent the lack of information about geometry and doping levels, similarly to [122] we assumed the following parameters: $W_{drift} = 10\ \mu m$; $N_{drift} = 3 \times 10^{15}\ cm^{-3}$, guarantee the assumed $BV_{DS} \approx 900\ V$.

For a complete comparison with the choice commercial device [115], it has been decapsulated and thus measured its footprint. We have got an area of 2.1 mm^2, from which a 50 μm wide ring for the junction termination should be subtracted, giving an actual area of ($\approx$ 1.9 mm^2). The measured R_{ON} of the commercial device as a function of V_{DS}, for $V_{GS} = 15\ V$, is shown in Fig. 4.9 together with that calculated by numerical simulations. The plotted values has been calculated for $V_{GS} = 15\ V$. Also for commercial device has been considered the same value for the specific contact resistance ($10^{-6}\ \Omega\times\ cm^2$). However, has been performed simulations to evaluate the impact of contact resistance (seen above) on the electric performance.

Considering these last results, it is clear that simulation results appear in good agreement with the experimental data Fig. 4.9, and that the contact resistance has not a heavy impact on the electrical characteristics thanks to the heavy doped junctions Fig. 4.8 .

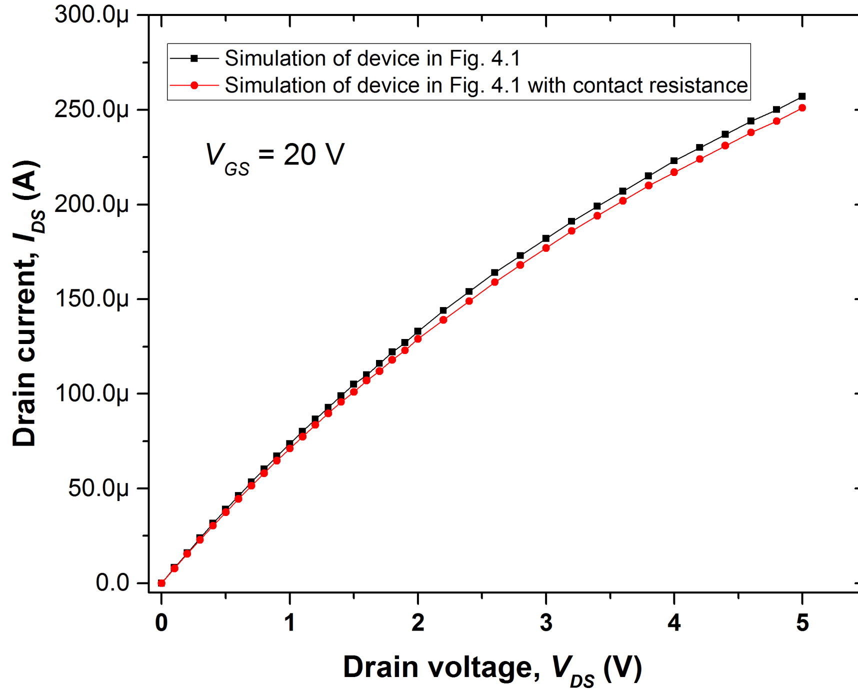

Fig. 4.8. Contact resistance weight on forward characteristics; $R_G = 176\ \Omega$, $R_S = 325\ \Omega$, and $R_D = 100\ \Omega$.

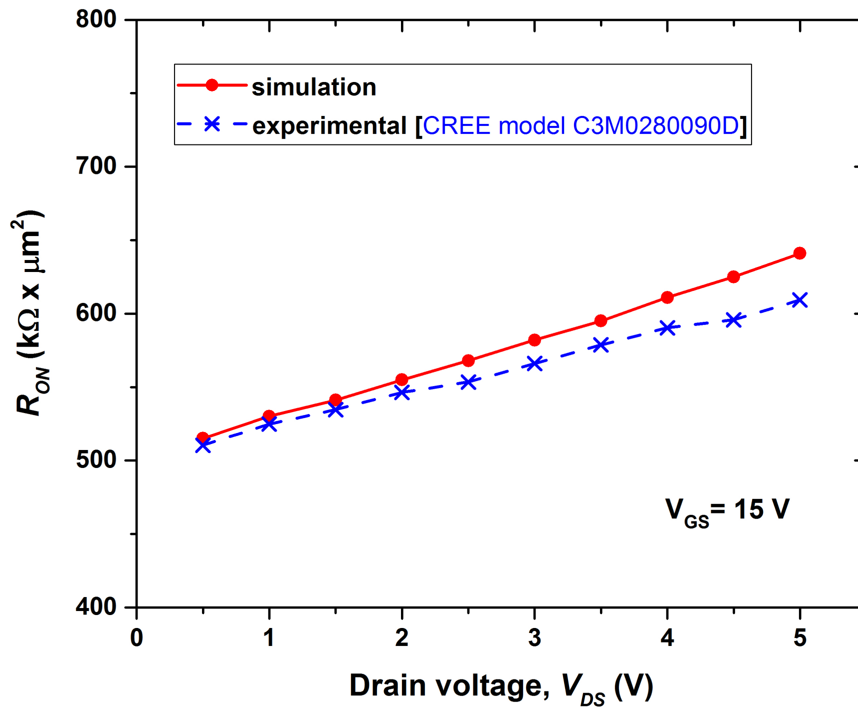

Fig. 4.9. Comparison between the R_{ON} of a commercial device and that calculated by numerical simulations as a function of V_{DS} for $V_{GS} = 15\ V$.

4.7 Transient analysis and switching times

In MOSFETs for high-performance switching applications (e.g. for DC-DC converters for solar power optimizers with conversion efficiencies higher than 98%) the static power dissipation, due to R_{ON}, is at least as important as the dynamic power dissipation during turn-ON and turn-OFF transients, the latter being governed in turn by the charge and discharge times of stray capacitances existing within the device. A common quality factor considered for a power MOSFET is, therefore, the gate charge:

$$Q_g = \int i_g \times dt$$

that must be transferred to (removed from) the gate capacitor in order to fully turn-ON (turn-OFF) the switch. The gate capacitance C_g is given by:

$$C_g = C_{gs} + C_{gd}$$

where C_{gs} is the gate-source capacitance and C_{gd} the gate-drain capacitance.

The capacitance C_g, and therefore Q_g, can be reduced by lowering the doping of the drift region (N_{epi}), but this has a negative impact on R_{ON}, so the best C_g value comes from a tradeoff between these two parameters. For this reason, a frequently used *Figure of Merit*[2] for power MOSFETs for a given BV_{DS} [123]:

$$FOM = R_{ON} \times Q_g \tag{4.3}$$

which should be as low as possible.

Transient simulations were therefore performed to estimate these quality parameters. When transient simulation is performed, the carrier continuity equations are integrated in the time domain. The reference circuit is shown in Fig. 4.10. It includes the device object of this study, with the characteristics of Fig. 4.5, and a lumped element for the load. The power source voltage, V_{DD}, and the load resistor, R_L, were chosen to have the MOSFET operate in deep triode region at $V_{DS} = 1\ V$, $J_D \approx 10$ $\mu A/\mu m^2$ (see Fig. 4.5) when a gate pulse $V_{GS} = 16\ V$ is applied.

During the transient simulation has been considered also the contact resistances, and simulations were run with and without a lumped gate driving resistance $R_{G,ext}$, to measure both the theoretical ($R_{G,ext} = 0\ \Omega$) and realistic ($R_{G,ext} > 0\ \Omega$) characteristic switching times of the device. That in Fig. 4.10 is the simplest circuit through which the device basic switching parameters can be calculated. The device was driven by voltage pulses with several amplitudes ($V_{GS} = 10 \div 23\ V$, in steps of $1\ V$), with switching times of 100 ps.

[2] For a brief overview, see Appendix C.

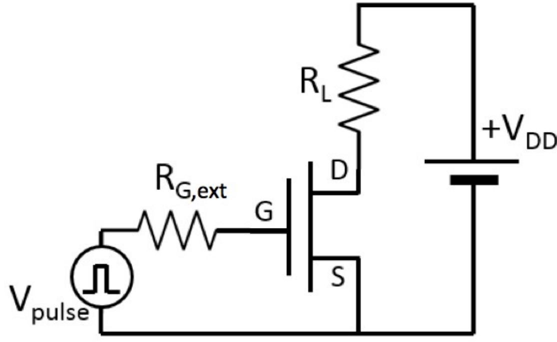

Fig. 4.10. Circuit for the MOSFET transient analysis: the MOSFET has a 1 μm^2 footprint, $R_L = 7.5\ M\Omega$, $R_{G,ext} = 0\ \Omega$ (or $R_{G,ext} = 200\ k\Omega$), and $V_{DD} = 75\ V$.

For a gate control was applied a pulse of 16 V applied at the time $t = 5\ ns$.

The evolution of the drain node voltage, from cut-off ($V_{DS} = 75\ V$) to full power ($V_{DS} \approx 1\ V$), is shown in Fig. 4.11 together with the drain current density.

The calculated 90% $\Rightarrow$ 10% fall times and 10% $\Rightarrow$ 90% rise times (i.e., t_f and t_r, respectively) of V_{DS} and J_D, for $R_{G,ext} = 0\ \Omega$ are listed in Table 4.3. The same Table also reports, in parenthesis, the switching times calculated for $R_{G,ext} = 200\ k\Omega$, corresponding to a gate drive resistance of 2 Ω if the device were upscaled to handle an $I_D = 10\ A$.

Table 4.3. MOSFET Switching Times.

Parameter	$\mathbf{t_f}$(ns)	$\mathbf{t_r}$(ns)
V_{DS} (V)	0.27 (0.54)	1.45 (2.10)
J_D ($\mu A/\mu m^2$)	1.48 (2.10)	0.25 (0.49)

The short values of switching times, clearly smaller than those of state-of-the-art commercial Si-MOSFETs of the same BV_{DS} class, imply advantages in terms of containment of dynamic power dissipation. The device performances are compared in Table 4.4 to those of state-of-the-art Si-MOSFET, including super-junction (SJ) devices.

Device [124], rated for $BV_{DS} = 100\ V$ shows a slightly smaller specific R_{ON} and notably higher switching times, while [125], rated for 150 V, has a considerably higher specific R_{ON}. Commercially available SJ devices, which are always rated for $BV_{DS} > 500\ V$ [126, 127], also behave slightly poorer.

From transient simulation has been extracted value of gate charge Q_g:

$$Q_g = \int_{tr}^{tf} i_g \left(V_{gs}\right)$$

and the result is shown in Fig. 4.12, which reports also the R_{ON} curve calculated in the range $V_{GS} = 10$ V - 23 V. Thus, the calculated figure of merit is:

$$FOM = R_{ON} \times Q_g = 0.48 \times 10^9\ \Omega \times C$$

which is smaller than that of other SiC MOSFETs designed for higher BV_{DS} [128] and comparable to that of [123] ($0.48 \times 10^9\ \Omega \times C$).

Table 4.4. Static and Dynamic Characteristics of State-of-the-art-MOSFETs.

This study	150	0.27 0.54	1.45 2.1	8.7	$A = 1.0\ mm^2$ $V_{GS} = 20\ V$ $I_D = 10\ A$	$V_{DD} = 75\ V$ $V_{GS} = 16\ V$ $I_D = 10\ A$ $R_{G,ext} = 0\ \Omega$ $R_{G,ext} = 2.0\ \Omega$
[124]	100	3.9	4.6	6.7	$A = 4.5\ mm^2$ $V_{GS} = 10\ V$ $I_D = 20\ A$	$V_{DD} = 50\ V$ $V_{GS} = 10\ V$ $I_D = 10\ A$ $R_{G,ext} = 1.6\ \Omega$
[125]	150	14	35	21.6	$A = 30\ mm^2$ $V_{GS} = 10\ V$ $I_D = 100\ A$	$V_{DD} = 75\ V$ $V_{GS} = 10\ V$ $I_D = 100\ A$ $R_{G,ext} = 1.6\ \Omega$
[126] (SJ)	600	4.5	8	80 [127]	$V_{GS} = 10\ V$ $I_D = 9.70\ A$	$V_{DD} = 400\ V$ $V_{GS} = 13\ V$ $I_D = 9.70\ A$ $R_{G,ext} = 5.3\ \Omega$
[129] (SJ)	225	-	-	14	$V_{GS} = 14\ V$ $J_D = 2\ A/mm^2$	-
[130] (SJ)	200	340	180	45	$V_{GS} = 10\ V$ $I_D = 20\ A$	$V_{DD} = 120\ V$ $V_{GS} = 10\ V$ $I_D = 7\ A$ $R_{G,ext} = 4.7\ \Omega$
[131] (SJ)	220	-	-	15	$V_{GS} = 10\ V$	

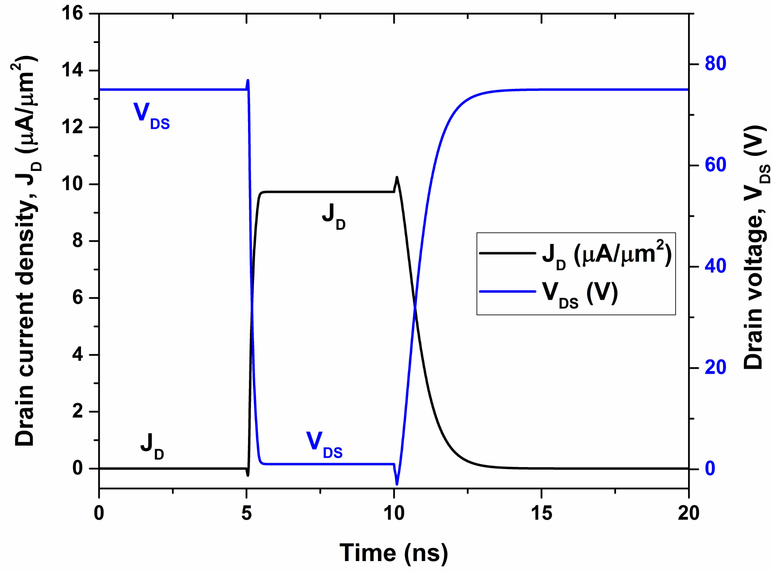

Fig. 4.11. MOSFET transient analysis (OFF-ON-OFF) at room temperature ($R_{g,ext} = 0$ Ω). The gate control pulse is applied at $t = 5$ ns and it switches from zero to 16 V in 100 ps. $V_{DD} = 75$ V.

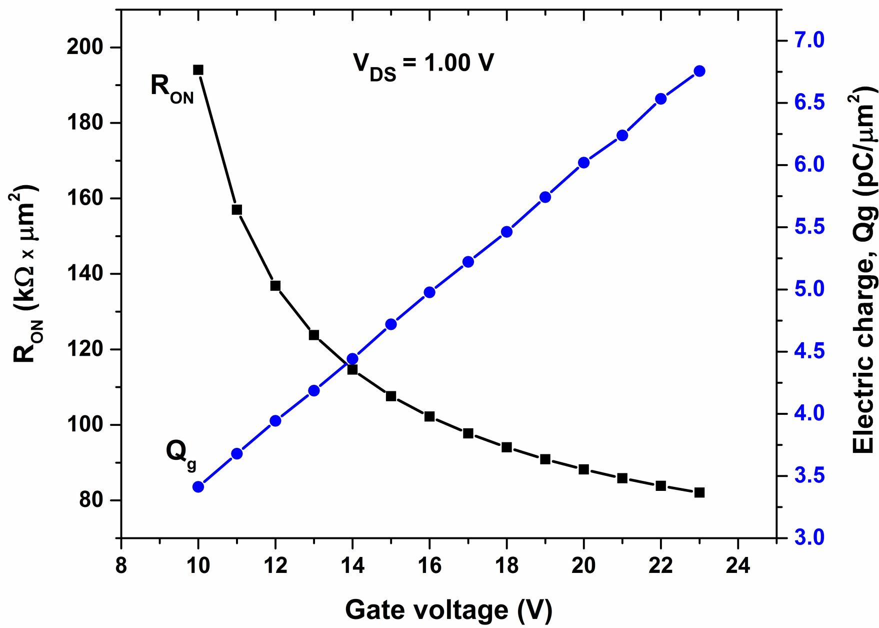

Fig. 4.12. R_{ON} and Q_g behaviours as a function of V_{GS}. For a structure with $Wj/2 = 2.5$ μm; $W_{drift} = 1.8$ μm.

4.8 ON-state resistance: dependence from temperature and bias voltage

The main physical phenomena which determine the dependence of the drain current from the temperature in the power MOSFET, as well as the physical models and the main parameters used during the simulations are referred to below.

For the device shown in Fig.4.2, the electrical characteristics were evaluated for different values of the bias voltage and in a temperature range between 300 K to 500 K, in steps of 50 K. From the followings figures it is clear that the ON-state resistance (calculated at $V_{DS} = 1\ V$) increase with the temperature, and of course, it decrease when increase the bias voltage, as is shown in Figs.4.14,4.13. The worst case occurs when the device operates at low bias voltage and at high temperature. This is an important warning that designers must take into account during the design phases. The drain current undergoes a reduction with increasing temperature, a phenomenon that is mainly due to the reduction of the carriers mobility.

As can be seen, the increase in temperature always produces an increase in the R_{ON} resistance, with a trend approximately linear.

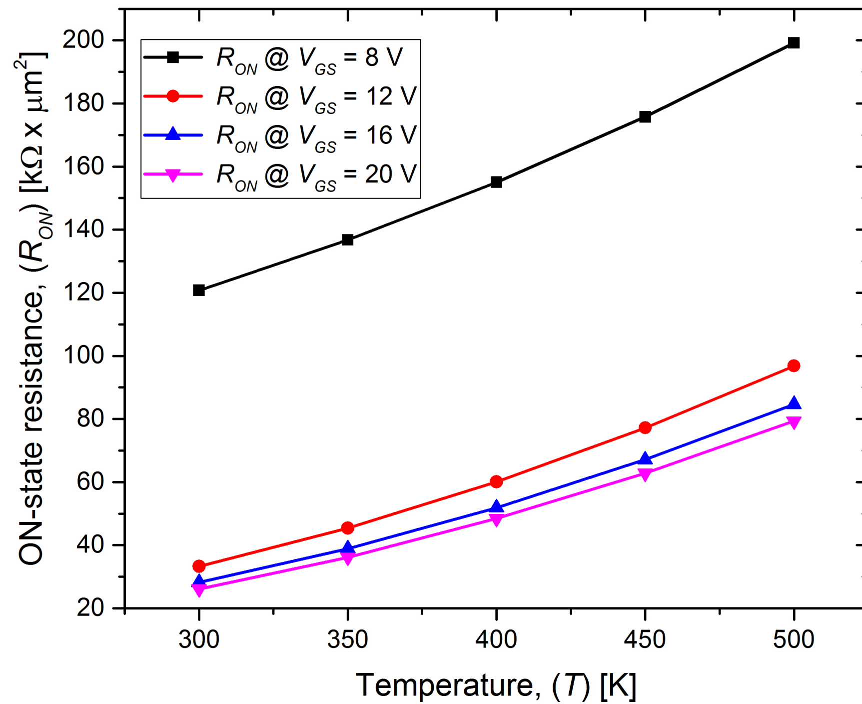

Fig. 4.13. ON-state resistance versus the absolute temperature. Plots obtained at different bias voltages.

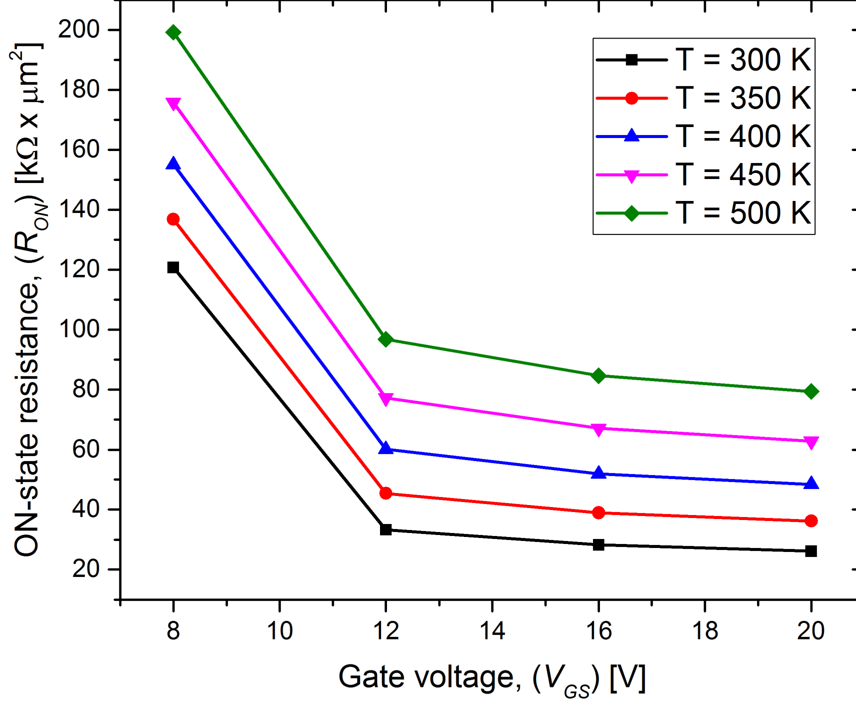

Fig. 4.14. ON-state resistance versus the bias voltages. Plots obtained at different bias absolute temperatures.

In the range of temperature (300 K - 500 K) the Fig.4.15 shows the percentage variation of the ON-state resistance versus the gate voltage. At low bias voltages, there is a variation of R_{ON} of about 40%. This variation increases up to $V_{GS} = 12$ V. For further increasing of the bias voltage up to 20 V, there is a very negligible percentage increase that is settled to around 65%. There is a percentage variation of R_{ON} of about 30% for the bias voltage between 8 V and 20 V.

To evaluate the impact of temperature on the performance of MOSFET under observation, the trends of drain currents were plotted as a function of the bias voltage of the device inside the considered range of temperatures, Fig. 4.16. The device presents a footprint area $A = 6.5\ \mu m \times 1.0\ \mu m = 6.5\ \mu m^2$. We can observe that at $V_{GS} = 8\ V$ the maximum drain current variation is given by:

$\Delta_{(V_{GS}=8V)}(I_{DS,300} - I_{DS,500}) = 3.26\ \mu A$.

Instead, at $V_{GS} = 20\ V$ result:

$\Delta_{(V_{GS}=20V)}(I_{DS,300} - I_{DS,500}) = 25.71\ \mu A$.

Therefore, the percentage variations of drain current can be calculated as:

$$\Delta_1 = \frac{\Delta_{(V_{GS=8V})}\left(I_{DS,300} - I_{DS,500}\right)}{I_{DS,300}} \times 100 = \frac{8.28 - 5.02}{8.28} \times 100 = 39.37\%$$

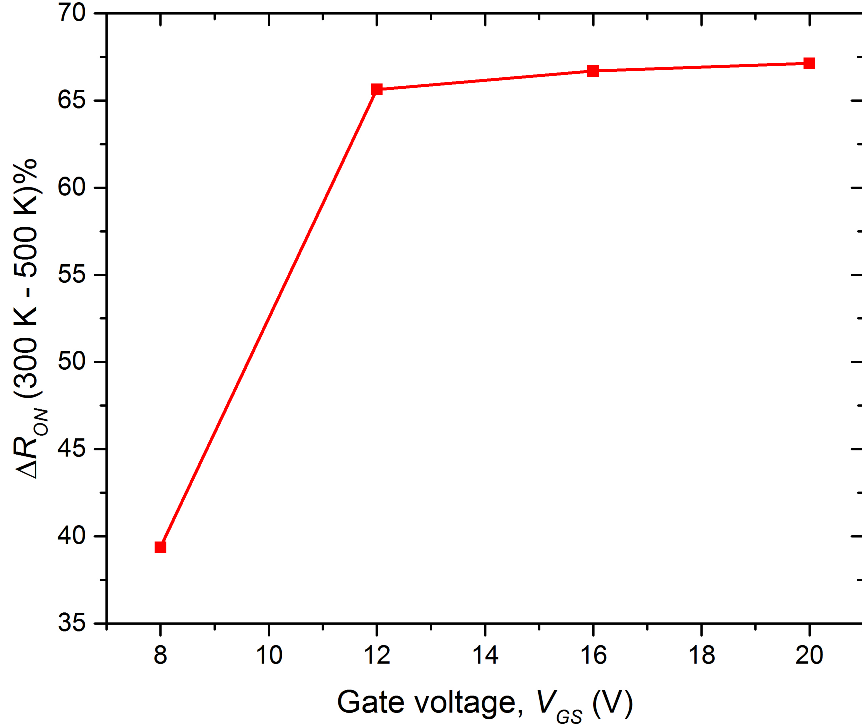

Fig. 4.15. Percentage variation of the ON-state resistance versus the bias voltage.

$$\Delta_2 = \frac{\Delta_{(V_{GS=20V})}\left(I_{DS,300} - I_{DS,500}\right)}{I_{DS,300}} \times 100 = \frac{38.31 - 12.60}{38.31} \times 100 = 67.11\%$$

Thus, the impact of temperature on the MOSFET performance becomes more consistent with higher bias voltages, this is due to the already seen increase in the ON-state resistance with the temperature.

Other developments of low voltage MOSFETs in terms of R_{ON} minimization are focused mainly on the following two points:

1. Increment of channel density (smaller cell pitch implies a smaller specific R_{ON}).
2. Reduction of substrate contribution by use of highly doped, thin substrates.

Otherwise, the design of MOSFETs for voltages $V_{GS} < 20\ V$ is taking advantage of shorter channel length, thinner oxide (high g_m), and low V_{TH}. As shown schematically in Fig.4.17 [99](R_{ON} vs. V_{GS} for two technologies with different V_{TH} and g_m), lower V_{TH} reduces R_{ON} at low V_{GS}, and higher transconductance (g_m) leads to a faster drop of R_{ON} for V_{GS} higher than V_{TH}. Thus, low R_{ON} is all what matters for load switch applications.

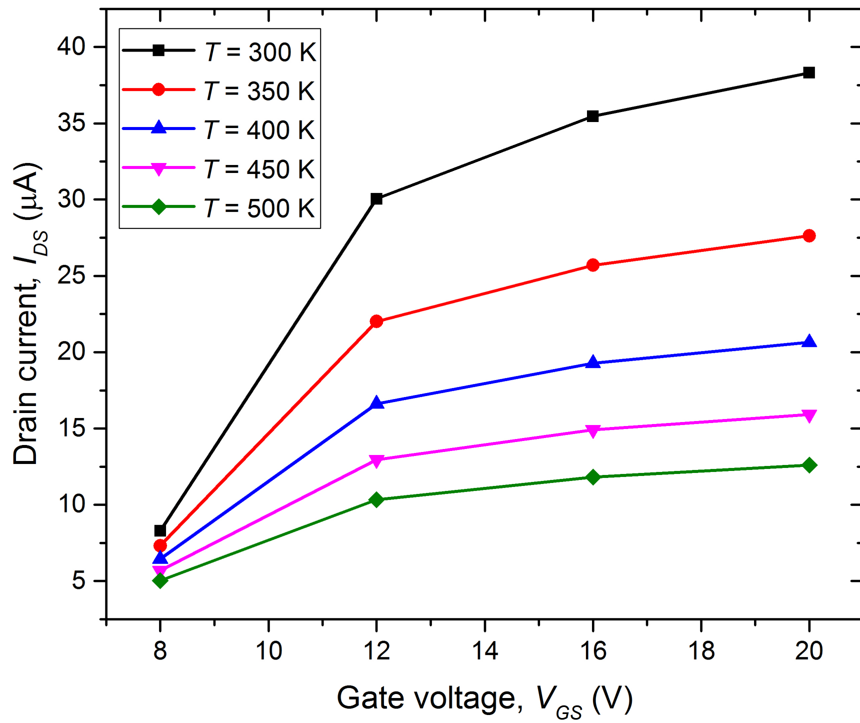

Fig. 4.16. Drain current trend and dependence by temperature.

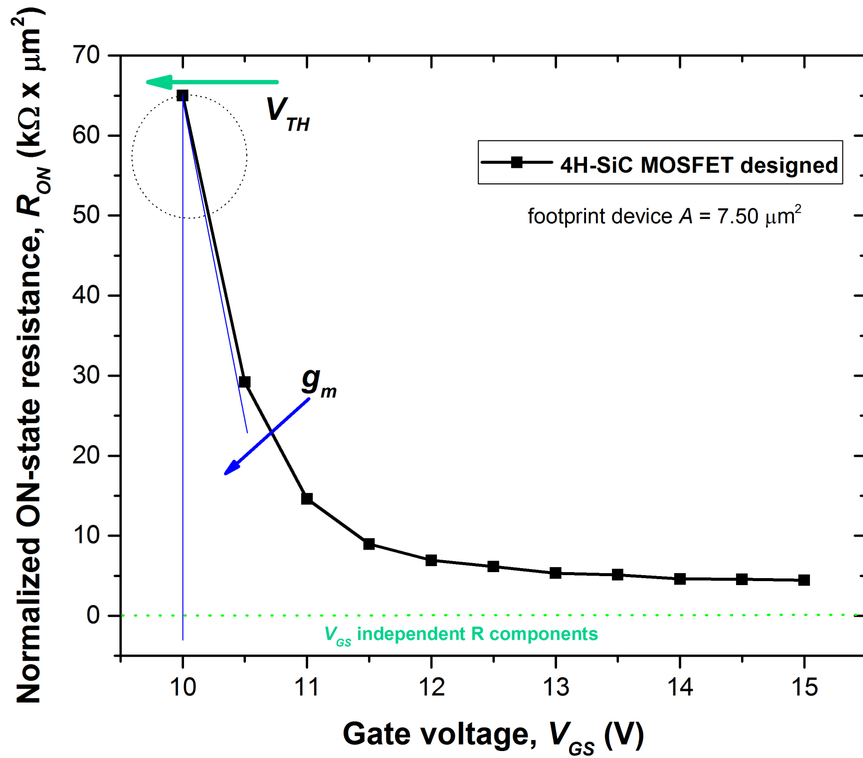

Fig. 4.17. ON-state resistance (normalized to footprint area) versus gate voltage.

4.9 Study of SPICE models of the designed MOSFET and comparison with the numerical model developed with Silvaco ATLAS

Research and industry have much software for circuit simulation and for the extraction of SPICE parameters of a device sized for a specific application. Among these the most used are:

- FineSim (Synopsys)
- HSPICE (Synopsys)
- PSpice (Cadence)
- Eldo (Mentor Graphics)
- Multisim (Electronics Workbench)
- LTspice (Linear Technology Corporation)

Each software adopts different algorithms; some of them are proprietary, others of the Open-Source type. The choice of the SPICE model to be adopted is based on the type of simulations and expected results, for which there are several SPICE models to simulate the MOSFETs, and the choice of the most appropriate one is based on the particular electrical parameters to be obtained and on the properties to model.

The SPICE models of level 1, 2 and 3 are the most used for the simulation of devices with a channel length of the order of tenths of a micron. If we want to take into account even the most advanced parameters, in terms of both physical parameters and numerical precision or technological processes, we can adopt a BSIM model (Berkeley Short-Channel IGFET Model). It is mainly used in the variants BSIM1, BSIM3, BSIM4, BSIM6, etc, which allow scaling the model parameters according to the geometry of the MOSFET [132]. These models are, however, suitable for planar submicrometric devices and, therefore, will not be taken into account for our vertical power MOSFET. Returning to the basic models, below, we summarize the main features:

- Level-1: The first level is not particularly fine and detailed, it allows to quickly obtain fairly accurate results for digital simulations or switching, but not for analogue applications.
- Level-2: The second level is particularly suitable for modelling effects of electric charges in bulk regions on the current I_{DS}; this makes this model useful for analogue circuits with very low electric currents, typically I_{DS} from 1 μA up to about 1 nA.

- Level-3: The third level allows realizing simulations that converge better and faster to the results compared to those obtained with the Level-2 model and, for this reason, it is also one of the most used models.

The SPICE parameters were extracted from the designed and simulated device; this phase required an accurate evaluation of the simulation models to be used [133]. The first phase of the SPICE modelling allowed to obtain a first approximation model using the Level-3 SPICE algorithm. The latter phase is a semi-empirical model developed in 1980, whose algorithm requires parameters that can be determined by experimental characterizations and/or numerical simulations. This model calculates the overlap capacities (C_{GDO}, C_{GSO}, C_{GBO}) for the evaluation of the current-voltage characteristics of the active MOSFET region (see 4.18).

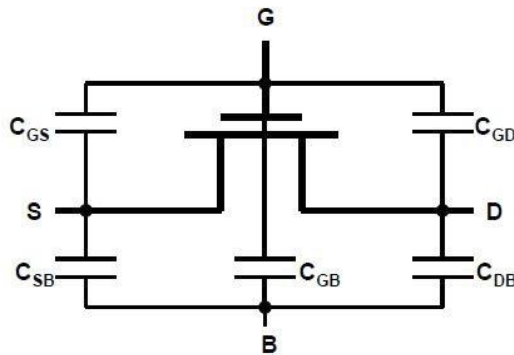

Fig. 4.18. Parasite capacitance of the MOSFET.

The model adopted considers the overlap capacity associated with the gate oxide, as a distributed capacity between the gate, source, drain and the bulk region. The MOSFET parameters for models of Level-1, Level-2 and Level-3 are divided into three categories:

- Absolute parameters of the device.
- Scalable and process parameters of the device.
- Geometric parameters.

A SPICE model reconstructs the electrical behaviour of a device through its representation in the form of electrical networks consisting of fundamental circuit elements, such as generators (voltage or current), resistors, capacitors and, rarely, inductors. Depending on the type of device, the description of the model can be defined either through the parameters obtained from the datasheet and/or from numerical simulations or through a netlist of descriptive sub-circuits. The Cadence Model Editor

converts information from the datasheets or numerical simulations in the parameters for the PSpice model simulator, with a structure of type ".model" Fig. 4.19 shows the schematic circuit of a MOSFET model of Level-3 type, used by the Model Editor for the extraction of the primary parameters PSpice. Unfortunately, some parameters of the results were not enough satisfactory, due to the particular cell structure of the device under study. Almost all the major SPICE tools available are based on the BSIM models (Berkeley Short-channel IGFET Model), this algorithm has not yet available a library for the correct extraction of parameters from a Vertical-DMOSFET (VDMOS). Thus, has been extracted these particular SPICE parameters with a specific Cadence library based on model BSIM Level-1, which allowed to simulate properly also the VDMOS structures. More details are contained in [133].

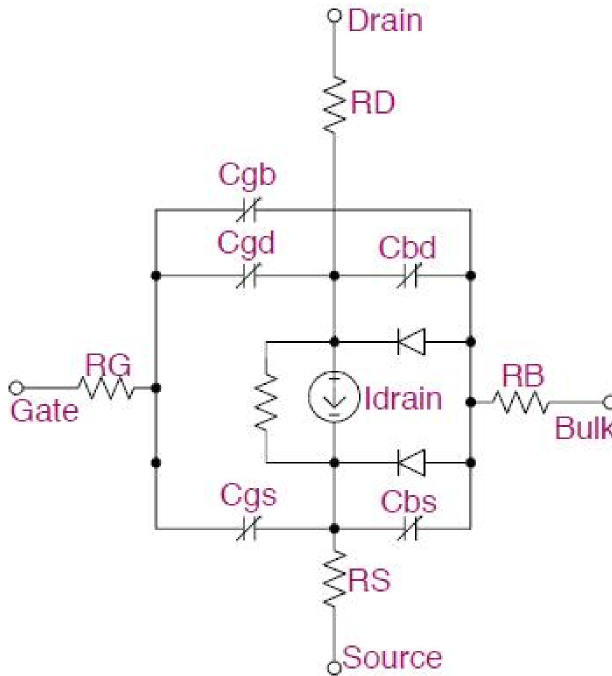

Fig. 4.19. SPICE schematization of the MOSFET Level-3.

4.10 LTSpice VDMOS model

The vertical double-diffusion MOSFET (VDMOS) behaves qualitatively different from those of planar MOSFETs. In particular, the drain-source diode of a VDMOS transistor is connected differently to the external terminals with respect to the diode of a monolithic MOSFET and the non-linear behaviour of the gate-drain capacitance

C_{GD} cannot be modelled easily, since the C_{GD} changes abruptly for gate-drain voltages close to zero. When the gate voltage is negative, the C_{GD} assumes the capacitance value of a capacitor in which the gate constitutes one of the electrodes while the other electrode is the drain contact placed on the back of the device. Obviously, given the high thickness of the drift region, the C_{GD} assumes, in this case, a very low value. On the other hand, when V_{GS} is positive, the drift region is conducting and the C_{GD} capacity becomes that of the capacitor having the gate oxide as a dielectric, which is very thin, so the C_{GD} grows enormously [134]. Among the various SPICE models dedicated to vertical MOSFETs, one of the most efficient, also from a computational point of view, is the VDMOS model developed by Linear Technologies for its LTspice circuit simulation software. The model is inspired in practice by the Level-1 model, integrated with some modifications. The parameters L (channel length) and W (channel width) are set equal to 1 so that the transconductance can be fixed directly, for each simulation; the gate-source capacity (C_{GS}) is assumed to be constant, which is an acceptable approximation in the hypothesis in which V_{GS} never assumes negative values; the gate-drain capacity (C_{GD}) follows the empirically determined approximation, shown below:

- For $V_{GD}> 0$, C_{GD} changes as the hyperbolic tangent of V_{GD}.
- For $V_{GD} <0$, the C_{GD} changes as the arctangent of V_{GD}.

For the calculation of the C_{GD} it is necessary to provide two parameters, C_{GDmax} and C_{GDmin}. Finally, the C_{DS} drain-source capacity is modelled as that of the diode present between the drain and source contacts, excluding the drain and source resistors (R_D and R_S). Fig. 4.20(a) shows the circuit model of a VDMOS, while in Fig. 4.20(b) the empirical trend of C_{GD} is shown when V_{GD} changes [135].

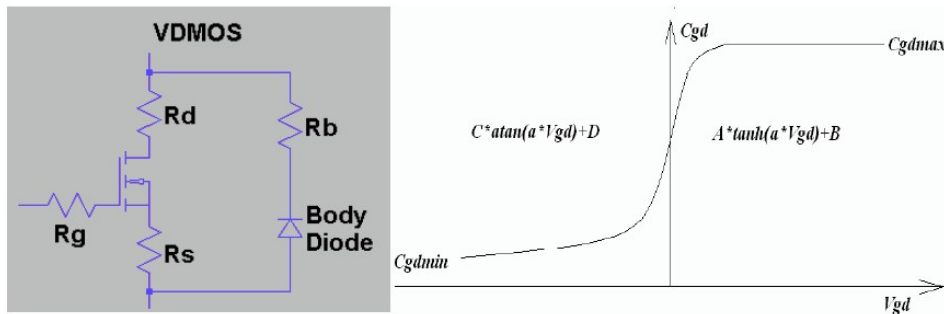

Fig. 4.20. a) Circuit model of the VDMOS implemented in the LTspice simulator; b) Empirical trend of C_{GD} as the V_{GD} changes and its mathematical model.

4.11 Extraction of the model parameters

In order to develop the SPICE model, the Model Editor software requires some parameters supplied by the user. In particular, it requires experimental values or values calculated previously through numerical simulations, which in our case come from the output simulations with Silvaco Atlas. The specific model of the MOSFET estimates the transfer curves and the threshold voltage of the device. In our model, many parameters have been calculated separately, as the Silvaco Atlas simulation software does not allow to export a list of SPICE parameters to be used with a PSpice model. The Model Editor presents a series of calculation sheets, each one dedicated to the calculation of a particular feature. The parameters calculated through the following parameters are described below: transconductance, $R_{DS,ON}$, and individual components of the gate capacity.

4.11.1 Transconductance

Referring to the I-V trans-characteristic, it is possible to define for a n-channel MOSFET a fundamental differential parameter which is called transconductance; this parameter for the saturation region is defined analytically by means of the eq. 4.4:

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_Q = K_n^{'} \frac{W}{L} \left(V_{GS} - V_{TN} \right) = \frac{2I_D}{V_{GS} - V_{TN}} \tag{4.4}$$

With

$$K_n^{'} = \begin{cases} K_n \frac{L}{W} \\ \mu_n C_{ox}^{''} \end{cases}$$

where:

- K_n and $K_n^{'}$ are called transconductance parameters and both have units of A/V^2.
- $C_{ox}^{"} = \varepsilon_{ox}/T_{ox}$ is the capacitance per unit area (F/cm^2).
- $\varepsilon_{ox}(Si) = 3.9 \cdot \varepsilon_o$ is the oxide permittivity (F/cm).
- $\varepsilon_o = 8.854 \times 10^{-14}$ (F/cm).
- T_{ox} is the oxide thickness (cm).

The calculation of transconductance requires a series of values of the current I_{DS} and bias voltage V_{GS}. The Table 4.5 shows the value calculated by the characteristics in DC and subsequently supplied from Model Editor. Some ambiguity can sometimes arise on some parameters used by the various manufacturers since there is not a precise standard. In particular, the transconductance g_m can also be indicated with g_{FS}. The

transconductance is a measure of the sensitivity of the drain current to the changes of bias voltage. This parameter is normally indicated for a value of V_{GS} which supplies a drain current equal to about half of the maximum nominal current value and for a V_{DS} that ensures operation in the constant current region [26]. When the working point "Q" has been set on the trans-characteristic, that is the three values (V_{DS}, V_{GS}, I_{DS}), and once the characteristic in the neighbourhood of that point has been linearized, the transconductance measures the slope of the trans-characteristics at the work point considered. It is obvious that, depending on the region of operation of the device, there will be different values of g_m. The transconductance is influenced by the gate width, which increases proportionally to the active area. The channel length also affects transconductance, in fact, the reduced length of the channel is advantageous for both trans-conductance (g_{FS}) and channel resistance (R_{ch}). The lower limit of this length is imposed by the Double Diffusion process. Finally, reducing the oxide thickness, T_{OX}, the transconductance value is increased, because $g_m \propto 1/T_{OX}$.

Table 4.5. Calculated transconductance values for the SPICE Level-3 model.

V_{GS} (V)	g_{FS} ($\mu A/V$)
10	3.35
11	3.76
12	3.95
13	4.03
14	4.05
15	4.02
16	3.97
17	3.91
18	3.93
19	3.76
20	3.68
21	3.60
22	3.52
23	3.44

4.11.2 Gate capacitance

Since the Model Editor also requires the values of the parasitic capacitances of the C_{GSO} and C_{GDO} gates, the calculation of the above capacities has been implemented in the simulation code of Silvaco Atlas. The calculation procedure provided for sim-

ulations in AC, applying a small variable signal at the frequency of 1 MHz on each terminal. For our device we have obtained the following capacity values, then used in the Model Editor for the extraction of the SPICE model:

- $C_{GSO} = 3.98 \times 10^{-11}\ F/m$
- $C_{GDO} = 3.98 \times 10^{-11}\ F/m$

The calculation of the C_{GSO} and C_{GDO} gate capacitances together with the resistance values associated with the single MOSFET contacts have allowed closing the control and correction chain of the SPICE parameters extraction algorithm.

4.11.3 ON-state resistance

The Level-3 model estimates the value of the ON-state resistance through the R_{DS} of the device, this model evaluates mainly three contributions [128]:

- Channel resistance, R_{ch}.
- Series resistance to each of the source and drain terminals, R_S and R_D.

This model makes continuous feedback with the R_D until obtaining the correct resistance value. However, it is important that the R_{DS} is calculated at an I_{DS} value that does not exceed the absolute maximum value of the direct current (algorithm setting). The Model Editor requested the values of I_{DS} and R_{ON} for a $V_{GS} = 16\ V$, obtaining for $V_{DS} = 0.5\ V$ the $R_{ON} = 14.792\ k\Omega \times \mu m$.

4.11.4 Turn-ON charge

The value of gate charge Q_{GS} associated with the gate-source terminals ranges from zero to the value required to support the maximum load current at the highest value of the V_{GS} voltage.

The Q_{GD} charge associated with the capacity on the C_{GD} gate-drain terminals, switches the load current to the V_{DD} voltage, while the Q_{GS} charge represents the charge that initiates the switching (start switching). The gate capacitances in the SPICE model of the MOSFET are dependent on the point of operation in DC and are active in the AC phase, mainly during the switching transitions; moreover, these capacities are not calculated during the DC analysis. The different SPICE models can select the gate capacities to be evaluated and use the most appropriate calculation model. Furthermore, we recall that the SPICE Level-3 model operates with the overlap extracted capacities, C_{GDO} (gate-drain), C_{GSO} (gate-source) and C_{GBO} (gate-bulk), whose values are derived from the extraction model itself. They depend on the type of

material used and on the surface state of the semiconductor. These characteristics also influence the value of the voltage applied to the gate. For a classic planar MOSFET model, implemented in Level-3, the three surface states are:

- Accumulation.
- Emptying.
- Inversion.

When the device works in the accumulation state, an accumulation layer of charges is formed that behaves like a capacitor armature, while the high concentration of holes in a substrate P (N-type device) forms the second armour of the capacitor. The gate capacity is evaluated roughly as [99]:

$$C_G = \frac{(\varepsilon_{SiC} \cdot \varepsilon_0)}{T_{OX}} \tag{4.5}$$

Finally, the values C_{GSO} and C_{GDO} are multiplied by the channel thickness of the MOSFET in order to present the appropriate capacitance values. The circuit in Fig.4.21 shows the type of circuit considered in the Level-3 [136]. The different SPICE models use distinct algorithms to extract the aforementioned capacities, which give quite similar results. What differentiates them is mainly the calculation speed of execution, based on the algorithm used and the number of iterations that are calculated; the latter are evaluated based on the required numerical accuracy. Obviously, the different SPICE models of the Level-1 series, Level-2, Level-3 and BSIM use different discretized formulas for calculating capacities. A very precise calculation is usually performed only on the final device, this because the total computing time increases considerably [76].

Figure 4.22 [137] shows a qualitative diagram of the division of the gate charge. The SPICE Level-3 model uses n-iteration calculation and control parameters, where "n" is usually a very complex parameter that takes into account the convergence and optimization of several design and sizing variables. This model is derived from empirical relationships between experimental data and existing theoretical models; compared to the Level-2 model, it includes the effect DIBL (Drain-Induced Barrier Lowering) and the effects of the degradation of mobility. The Level-3 models are applicable to devices with a long channel, thus approximately up to 2 μm.

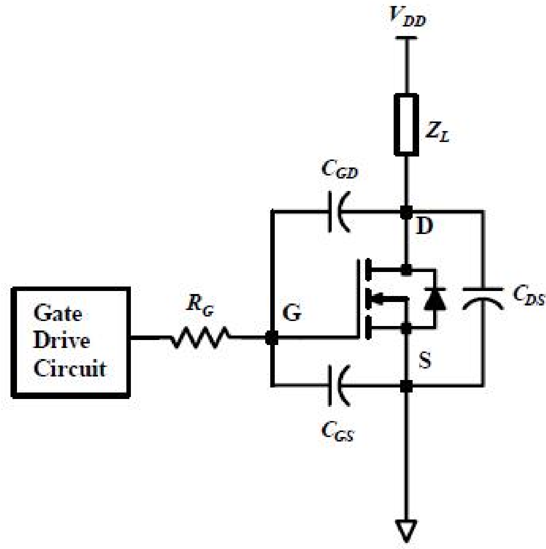

Fig. 4.21. SPICE circuit model for a power MOSFET.

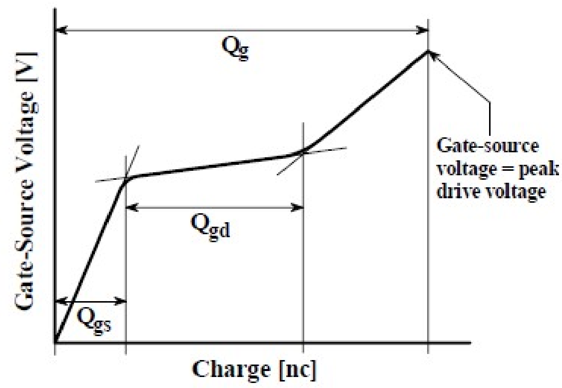

Fig. 4.22. Evolution of the V_{GS} as a function of the gate charge.

4.12 Comparison between SPICE model and numerical model

4.12.1 PSPice model

The Level-3 model of the obtained 4H-SiC MOSFET is defined by the parameters shown below in table reported as Fig.4.23. For completeness, has been listed as first the physical parameters of the materials and of the technological processes used:

LAYOUT PARAMETERS	**VALUE**	**UNIT**
L	1	μm
W	1.54E-5	μm
Drain/Source Area	3.08E+5	μm^2
Perimeter of Drain/Source	44	μm
# squares between Contact and Channel	0.001	
# squares between LDD/N+ and Channel	0.001	
PROCESS PARAMETERS	1=YES/2=NO	
Aluminum gate	1	
n+ Poly gate	0	
p+ Poly gate	0	
N well (pMOSFET)	0	
P well (nMOSFET)	1	
Vth adjust Dose (+ for Boron, - for Phos)	0	cm^{-2}
Gate Oxide Thickness	800	Å
NSS	3E+11	cm^{-2}
Starting Wafer Resistivity	10	Ω-cm
Well Dose	2E+13; 2E+12	cm^{-2}
Well Drive Time	10	min
Well Drive Temperature	1100	°C
LDD D/S Dose	2.50E+13	cm^{-2}
LDD D/S Drive Time	10	min
LDD D/S Drive Temperature	1000	°C
Field Oxide Thickness	6000	Å
Minority Carrier Lifetime in the well	1	μs
D/S Dose (N+ or P+)	2E15	cm^{-2}
D/S SILISIDE (1=YES, 0=NO)	0	

Fig. 4.23. Level-3: Parameters of MOSFET.

In the table shows in Fig.4.24 have reported the calculated parameters, specific for the studied MOSFET.

Figure 4.25 shows the characteristics of our device compared with those of the MOSFET designed using the Atlas-SILVACO numerical simulator.

A not particularly good agreement is observed, especially at the average gate bias, with the drain current values that differ from 40% or more.

The observed deviation results in an inaccurate calculation of the differential transconductance of the device, in a region in which it could operate during the

Level	3	UNIT
TPG	0	
TOX	8E-8	m
LD	1.85E-7	m
WD	3.00E-7	m
UO	777	cm^2/Vs
VTO	8.77	V
THETA	0.900	1/V
RS	1.35	Ω
RD	1.35	Ω
DELTA	1.37	
NSUB	1.22E+17	cm^{-3}
XJ	1.15E-7	m
VMAX	5.47E+7	m/s
ETA	0.179	
KAPPA	0.142	1/V
NFS	3.00E+11	cm^{-2}
CGSO	3.98E-11	F/m
CGDO	3.98E-11	F/m
CGBO	5.75E-10	F/m
PB	1.98	V
XQC	0.40	

Fig. 4.24. Calculated Parameters.

switching phases. It is believed that this result is due to the particular formulation of the Level-3 model, which remains however particularly suitable for the calculation of planar MOSFET currents, in which the drain and source regions are almost symmetrical.

4.13 SPICE simulations: final consideration

Has been compared the numerical simulation model obtained with ATLAS (Silvaco) and the electric model SPICE obtained with LTSpice (Cadence). The 4H-SiC MOSFET model based on the VDMOS model inside the LTSpice simulator is defined by the following statement:

.model MOSFET-ENEA VDMOS (Rg=0.1 Vto=5.9 Rd=1m Rs=72m Rb=1.1m Kp=1.0 Lambda=0.1 A=0.3 M=0.35 Is=8.1p Vj=2.5 N=1.077 Ron=0 Qg=7n TT=90n mtriode=2.2 phi=1 ksubthres=0.5)

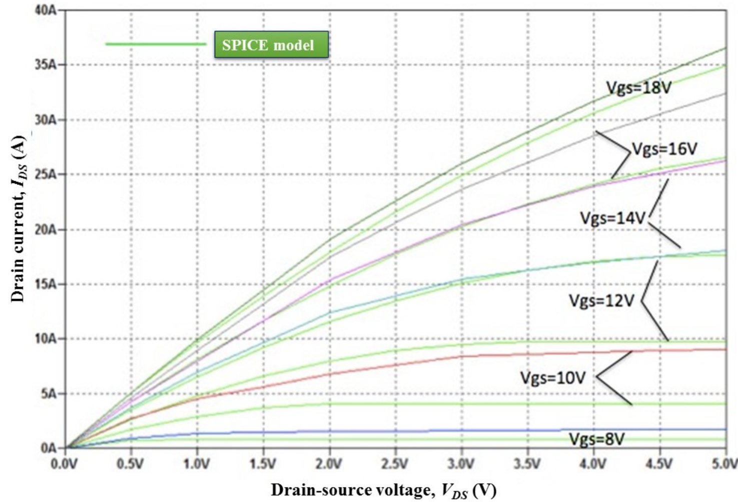

Fig. 4.25. Comparison between the characteristics of the designed MOSFET obtained from the PSpice circuit model (light green) and from the finite element simulator Atlas-SILVACO (various colours).

The following (Fig. 4.26) shows the characteristics of the aforementioned device compared with those of the MOSFET designed using the Silvaco ATLAS numerical simulator. A satisfactory agreement is observed between the curves shown, the values of which deviate at a maximum of 10%, however, in regions presumably far from those of actual use of the device if excessive power dissipation is to be avoided.

4.13.1 Simulations in transient

Finally, simulations of the LTSpice model of the MOSFET in switching mode were carried out. To perform these simulations has been used the circuit shown in Fig.4.27.

To carry out the transient analysis and calculate the relative switching times, we used the circuit of Fig. 4.27, whose parameters were calculated considering the device of the Infineon IPB072N15N3G in which the operating conditions are given in the datasheet. Since this device and our MOSFET have the same $BVds$, we set the same value of the Vdd. Thus, the SPICE simulations were carried out by imposing a $Vdd = 75\ V$. Regarding the R_L load resistor, from the same datasheet emerges that its resistance is fixed by Infineon to the value: $V_{DD}/I_{max} = 75/100 = 0.75$ Ω, value also used during our simulations. It is emphasized that, in order to ensure uniformity of operating conditions with the numerical simulations and those of the Infineon MOSFET, it was necessary to scale the dimensions of the SPICE model for the 4H-SiC MOSFET.

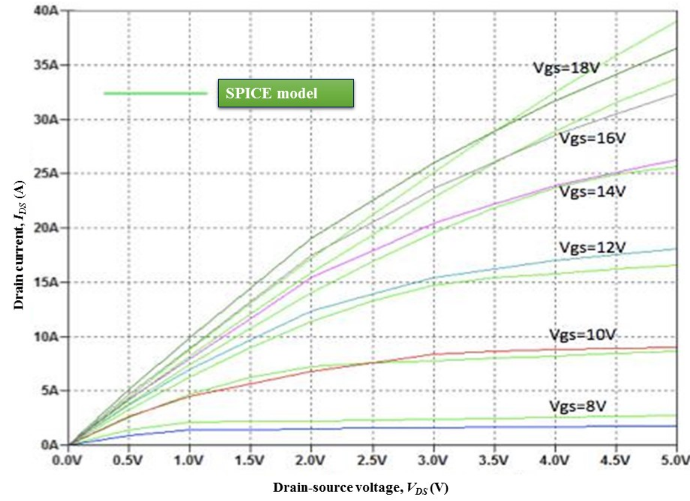

Fig. 4.26. Comparison between the characteristics of the MOSFET object of the study obtained from the VDMOS LTSpice circuit model (light-green) and the Silvaco ATLAS finite element simulator (various colors).

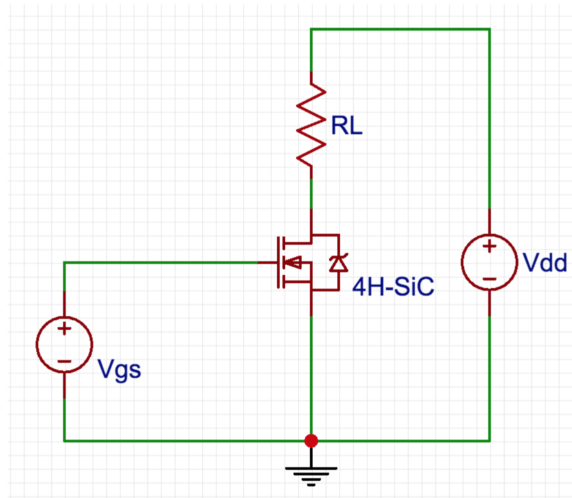

Fig. 4.27. Bias circuit applied to the 4H-SiC MOSFET for the SPICE simulation of the turn-on phase.

In fact, while the Infineon device is completely switched ON and capable of conducting $I_{DS} = 100\ A$ with $V_{DS} = 0.5\ V$, the MOSFET presented in the previous paragraphs is sized for $I_D = 4\ A$ to the same V_{DS}. This requires an area scaling of a factor of 25, with a consequent reduction in scale of the parasitic resistances (especially that of source) and an increase of the parasitic capacity. The model used is ultimately described by the following parameters.

.model MOSFET-ENEA VDMOS (W=2.1; Cgs=500p; Cgdmin=800p; Cgdmax =8000p; Rg=0.1; Vto=5.9; Rd=2m; Rs=2m; Rb=1.1m; Kp=1.0; Lambda=0.1; A=0.3; M=0.35; Is=8.1p; Vj=2.5; N=1.077; Ron=0; Qg=7n; TT=90n; mtriode=2.2; phi=1; ksubthres=0.5)

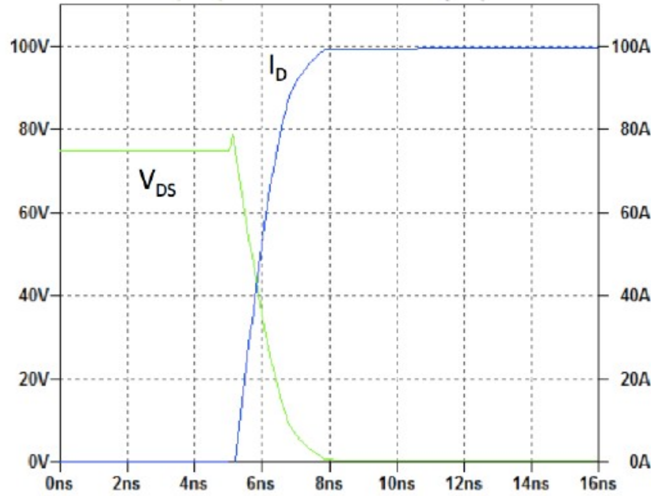

Fig. 4.28. Evolution of the drain current and drain-source voltage calculated with the SPICE simulations obtained with the model developed in this study.

A voltage step $V_{GS} = 16\ V$ has been considered with a rise time of 0.1 ns. Figure 4.28 shows the evolution of the drain node potential and the drain current, from the switch-OFF condition of the MOSFET ($V_{DS} = 75\ V$, $I_D = 0\ A$) to the complete switch-ON condition ($V_{DS} = 0.4\ V$, $I_D = 100\ A$).

The gate forcing is applied at time $t = 5\ ns$. For comparison, the following Fig. 4.29 shows the evolution obtained with the numerical simulations. [3].

The requirements for power optimizers used in photovoltaic modules, generally rated for a maximum voltage of 100 V, include high efficiency, for a fast return of investments, and 20 years or longer life span, under any weather conditions. Both these requirements could be addressed in principle by deploying the fast and rugged SiC-based switches, if only they were available for this voltage range. The performances of a 4H-SiC MOSFET with short drift layer, suiting 100-V-class switching converters, have been predicted by numerical simulations. The device features a 1.8 μm-thick epilayer, with a breakdown voltage of 150 V and an ON-state resistance in the order of 0.9 $m\Omega \times cm^2$, which is comparable to that of commercial Si MOSFET rated for the same voltage range. The switching analysis, performed considering a resistive load

[3] Report ENEA-2016

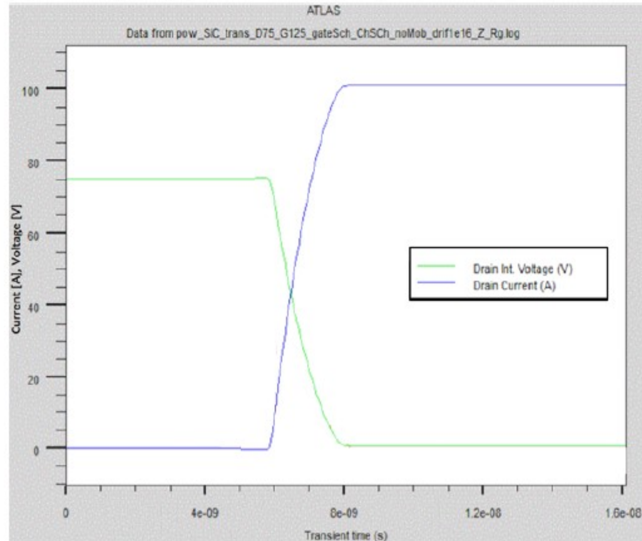

Fig. 4.29. Evolution of the drain current and drain-source voltage calculated with the numerical physical simulations.

at a drain current density close to 10 $\mu A/\mu m^2$, shows that the rise and fall times for V_{DS} are 1.45 ns and 0.27 ns, respectively.

A small figure of merit of $FOM = 0.48 \times 10^9\ \Omega \times C$ was also calculated in the best operating conditions of $V_{GS} = 16\ V$, $V_{DS} = 1\ V$, and $J_D = 10\ \mu A/\mu m^2$.

In conclusion, the characteristic parameters of the 4H-SiC MOSFET were obtained for two different SPICE-type circuit models: the Level-3 model and the VDMOS model. With the parameters obtained, both models are able to reproduce the characteristics of the device in the region of interest for switching applications, even if the VDMOS model, which is integrated inside the LTspice simulator of Linear Technologies, presents characteristics closer to those obtained with the numerical physical simulations of the device, with a maximum error close to 10%. Also, the SPICE simulation in transient of a MOSFET operating in switching has provided results very close to those obtained through numerical physics simulation.

4.14 Interface SiC/gate-oxide of a power MOSFET: study and assessment of defect and trap effects by means of numerical simulations

In chapter 3 of this thesis, theoretical arguments were presented regarding the problem of crystalline defects affecting the wafers and therefore reducing the performance of the electronic devices produced and of their reliability over time. Furthermore, the problem of traps in semiconductors that act similarly to defects has been discussed, with the only difference that they have different origins and distribution densities. In the device under study, both traps and defects play a very important role, especially inside the semiconductor regions where the MOSFET channel is formed. In fact, a reduction in the performance of device due to channel problems results in an increase of the ON-state resistance, and this means greater losses and reduced electrical performances both static and in transient.

In the last five years, as reported by Yole Devéloppement's data, the manufacturers of wafers and chipmakers have developed special technological steps to mitigate these unwanted effects below a "negligible" threshold, at least for applications most common. In fact, for niche applications, such as those in the military field, in which superior performance and greater reliability are required, the further steps to make are still many. In this section, will be presented the physical models and their main parameters implemented in Atlas simulator.

4.14.1 The trouble of traps at the interface between the MOSFET channel and gate-oxide

The fundamental electrical parameters of a MOSFET in 4H-SiC, such as BV_{DS}, I_{DS}, and R_{ON}, could be heavily affected by an explicit trap/defect concentration at the Silicon oxide (SiO_2) interface in correspondence of the channel region [40, 44]. From literature, several papers have dealt with the SiC technological issues, for example, the stacking faults, screw dislocations, and micro-pipes [138]. The high density of defects/traps at the SiO_2/SiC interface, in fact, disallow the realization of an efficient conductive channel in the MOSFET structure.

Has been studied the same 4H-SiC MOSFET structure already shown in Fig. 4.30, but dimensioned for a voltage-class of (600 $V \div$ 700 V). In this case, an evaluation of conjoint defect-and-trap-effects on the current-voltage characteristics was performed by means of numerical simulations. More in detail, the conjoint contributions of defects and traps are modelled as a function of different physical parameters, such as trap and

defect densities, location in the energy bandgap, and effective capture cross-sections. Modelling and numerical simulations have required an intensive physical parametric study and a long CPU-time. The results of simulations have provided interesting data that have allowed to a better understanding of the device performance at different bias conditions and temperatures. In fact, as highlighted during the simulations, the interface quality of SiO_2/SiC plays a key role in determining the device specific ON-state resistance. As verified during the simulations, by taking into account trap-and-defect-effects as well as the effective low electron mobility along the inversion layer at the SiO_2/SiC interface, for this structure the channel resistance contribute R_{ch}, has a heavy weight on the R_{ON} value.

The study and evaluation of the *Poisson*'s equation and of the carrier continuity equations for a finely meshed device structure was performed through numerical simulations. In particular, a mesh spacing down to 25 nm around the MOSFET P-N junctions and within the channel region under the SiO_2/SiC interface was imposed.

The other key physical models include the bandgap temperature dependence and apparent bandgap narrowing, the incomplete ionization of dopants, the *Shockley–Read–Hall* (*SRH*) and *Auger* recombination processes, the impact ionization, and the concentration and temperature dependent carrier lifetime and carrier mobility. This simulation setup is presented in detail in [64, 66, 68, 139]. In addition, it is supported by experimental results on implanted p-i-n diodes in a wide range of currents and temperatures.

For this new challenge has been designed and simulated a modified structure of that shown in Fig. 2.1, with a thicker epilayer depth of 10 μm. The design of this different structure has been necessary in order to adopt the same parameters used by other devices studied in the literature. For this new voltage-class (600 $V \div$ 700 V) has been investigated the main electrical characteristics of a 4H-SiC MOSFET, namely I_{DS}, R_{ON}), BV_{DS}, by using a TCAD 2D physical simulator. Detailed results on the existing trade-off between these fundamental device parameters were presented in [140]. Was investigated the SiO_2/SiC interface trap effects, which are an unavoidable technological issue and, by developing further the simulations parameters, it was clear that an explicit traps concentration at the oxide-semiconductor interface with the channel region has an apparent detrimental effect on the device forward current of device, and therefore on the R_{ON} value.

4.14.2 Physical modelling of traps at the interface SiC and gate oxide

The numerical simulation analysis was performed by using the Silvaco-ATLAS physical simulator [72] to solve the *Poisson*'s equation and the carrier continuity equations for a finely meshed device structure. In particular, within the channel region below the SiO_2/SiC interface a mesh spacing of only 12.5 nm was imposed. This fine step has assured better precision of results. In a poor quality SiO_2/SiC interface, we can consider a large number of defect states within the semiconductor bandgap. This *Density of defect States* (*DoS*) can be modelled as a sum of four terms, namely two exponentially decaying band tail states close to the conduction and valence band-edges, and two Gaussian distributions of deep states in the midgap. Each term can act either as donor-like or acceptor-like level for free carriers [72, 141]. In other words, an acceptor-like centre is negatively charged when filled and becomes neutral when empty. On the other hand, a donor-like centre is positively charged when empty and captures electrons similarly to ionized donor impurities. More in detail, the expressions for the tail state densities are in the form of [142]:

$$D_{T,C}(E) = D^0_{T,C} \exp\left(\frac{E - E_C}{U_C}\right) \tag{4.6}$$

$$D_{T,V}(E) = D^0_{T,V} \exp\left(-\frac{E - E_V}{U_V}\right) \tag{4.7}$$

where U_C and U_V are the characteristic energy decays and $D^0_{T,C}$ and $D^0_{T,V}$ are the tail state densities at the conduction band edge and valence band edge, respectively. At the same time, the midgap state densities, modelled as two Gaussian, are given by [142]:

$$D_{G,C}(E) = D^0_{G,C} \exp\left[-\left(\frac{E - E_{GC}}{W_C}\right)^2\right] \tag{4.8}$$

$$D_{G,V}(E) = D^0_{G,V} \exp\left[-\left(\frac{E - E_{GV}}{W_V}\right)^2\right] \tag{4.9}$$

where $E_{G,C}$ and $E_{G,V}$ are the energy values of the defect concentration peaks $D^0_{G,C}$ and $D^0_{G,V}$, respectively. The terms W_C and W_V take into accounts the different spectral widths of the Gaussian distributions. According to the *Taylor-Simmons* theory [143] [66], the *Carrier Recombination Rate* (*CRR*) is calculated as four terms

in the form of eq. 4.8, 4.9. Where the density is one of the terms $D^0_{T,C}$, $D^0_{G,C}$, $D^0_{T,V}$, $D^0_{G,V}$ introduced above.

$$\int_{E_V}^{E_C} \left(\frac{D(E) \cdot \bar{n} \cdot \bar{p}}{\bar{n} + e_n + \bar{p} + e_p} \right) \cdot dE \tag{4.10}$$

While ν_n and ν_p are the thermal velocities, and σ_n and σ_p are the capture cross sections for electrons and holes, respectively. Finally, e_n and e_p are the emission rates given by:

$$e_n = \sigma_n \nu_n n_i \cdot \exp\left(\frac{E - E_i}{kT}\right) \tag{4.11}$$

$$e_p = \sigma_p \nu_p n_i \cdot \exp\left(\frac{E_i - E}{kT}\right) \tag{4.12}$$

where n_i is the effective intrinsic carrier concentration, and $\bar{n}$ and $\bar{p}$ are:

$$\bar{n} = \sigma_n n \cdot \nu_{th} \tag{4.13}$$

$$\bar{p} = \sigma_p p \cdot \nu_{th} \tag{4.14}$$

Here, ν_{th} (1.34×10^7 cm/s) is the thermal velocity, and σ_n and σ_p are the capture cross sections for electrons and holes, respectively.

The capture cross sections have to be properly defined both for acceptor-like and donor-like traps. Their values were fixed as in [144] and the fundamental DoS parameters used during the simulations are summarized in Table 4.7 [72, 144].

4.14.3 Physical modelling of defects at the interface SiC and gate oxide

SiC exhibit crystal defects, which are caused by the presence of dangling bonds at interfaces or by impurities inside the substrate. These traps centre, in semiconductor substrates, can inevitably influence the electrical characteristics of a 4H-SiC-based device. Trap centres, whose associated energy is set in a forbidden gap, exchange charges with the valence and conduction bands through the capture and emission of electrons. Trap centres influence the recombination statistics of charges and the density of space charge in a semiconductor bulk. It is possible to take into account of these charges

in *Poisson*'s equation in addition to the ionized donor and acceptor impurities. Interface quality of a 4H-SiC MOSFET is a crucial factor for its performance; indeed, the electric charges located at the interface or inside the oxide layer play a key role. The best processes to grown oxides on a semiconductor can carry impurities and different kinds of charges. Carbon presence inside oxide can migrate during a post-oxidation phase of SiC wafer, this unwanted Carbon presence leads to a higher concentration of defects at the interface in comparison to the Silicon oxidation process. A schematic representation of the associated charges with the grown of oxide on SiC is shown in Fig. 3.27 [55, 145], where all the oxide charges are classified as:

a. Mobile ions charge in the oxide are tied to atoms as potassium (K) and sodium (Na) and can be easily transferred during the oxidation process [23]. Their diffusion in the grown oxide, and at the interface during the technological steps, produce a threshold voltage shift.

b. Oxide trapped charges in the oxide are usually distributed in the bulk of the oxide and are responsible for structural imperfections [55].

c. Fixed charges are usually posted at the interface or near it, in a thin sheet and in a concentration such that depends on all the parameters of oxidation process [55]. Fixed charges cannot exchange charge carriers with the SiC [88], but their location can become as scattering centres and heavily influence the threshold voltage of MOSFET devices. Interface fixed charge is modelled as a thin sheet of charges at the interface and therefore is controlled by the interface boundary condition. Interface traps and bulk traps will add space charge Q_T directly into the *Poisson*'s equation.

d. The interface-trapped charges (red-cross in Fig. 3.27) are related to the traps which have energy levels inside the bandgap of SiC. These traps can exchange charge carriers with the semiconductors, this means that all amount of trapped charges depends on the position of the trap levels in relation to the *Fermi* level E_f, this last is strongly dependent by doping concentration level.

Poisson's equation including the carrier concentrations, the ionized donor and acceptor impurity concentrations, and the total charge due to traps, Q_T, is reported in eq. 4.15.

$$\boxed{\nabla \cdot (\varepsilon \nabla \Psi) = q\left(n - p - N_D^+ + N_A^-\right) - Q_T} \tag{4.15}$$

where, Q_T, is the interface charge density present at SiO_2/SiC interface. N_D^+ and N_A^- are the substitutional n-type and p-type doping concentrations, so defined:

$$N_D^+ = N_D \cdot \left[1 + 2\exp\left(\frac{E_{Fn} - E_D}{kT}\right)\right]^{-1} \tag{4.16}$$

$$N_A^- = N_A \cdot \left[1 + 4\exp\left(\frac{E_A - E_{Fp}}{kT}\right)\right]^{-1} \tag{4.17}$$

where, E_D and E_A are the donor and acceptor energy levels. E_{Fn} and E_{Fp} are the quasi-*Fermi* energy levels for electrons and holes. The trapped charge Q_T is defined by:

$$Q_T = q(N_{tD}^+ - N_{tA}^-) \tag{4.18}$$

where N_{tD}^+ and N_{tA}^- are the ionized densities for donor-like and acceptor-like traps, respectively:

$$N_{tD}^+ = n + N_D^+ = \rho \cdot F_{tD} \tag{4.19}$$

$$N_{tA}^- = N_A^- - p = \rho \cdot F_{tA} \tag{4.20}$$

The ionized trap of densities depends upon their density ρ, and by its probability of occupation, i.e. F_{tA} for acceptor-like and F_{tD} for donor-like traps. Thus, assuming that the trap capture cross sections be constant in the forbidden band in eq. 4.16 and 4.17 we can write [146]:

$$F_{tD} = \frac{\nu_{th}\sigma_n + e_p}{\nu_n\left(\sigma_p + \sigma_n\right) + \left(e_n + e_p\right)} \tag{4.21}$$

$$F_{tA} = \frac{\nu_{th}\sigma_p + e_n}{\nu_n\left(\sigma_p + \sigma_n\right) + \left(e_n + e_p\right)} \tag{4.22}$$

Moreover, when multiple traps at multiple trap energy levels are considered, eq. 4.16 and eq. 4.17 are in the form of:

$$N_{tD}^+ = \sum_{\alpha=1}^{k} N_{tD\alpha}^+ \tag{4.23}$$

$$N_{tA}^- = \sum_{\beta=1}^{m} N_{tA\beta}^- \tag{4.24}$$

4.14.4 Device structure and parameters

The schematic cross-section of the considered 4H-SiC MOSFET half-cell is shown in Fig. 4.30.

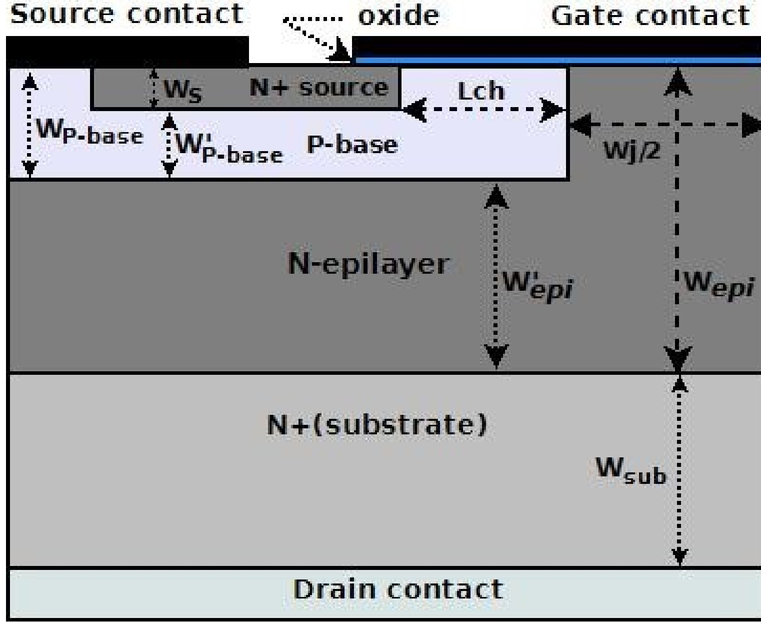

Fig. 4.30. Schematic cross-sectional view of the MOSFET half-cell. The drawing is not in scale.

The proposed structure is compatible with a process-run based on doping by ion implantation. The geometrical parameters and doping concentrations of the different MOSFET regions are summarized in Table 4.6. The device length along the Z-direction was set to 1.0 μm by default. The simulated MOSFET footprint area was:

$footprint = 6.5\ \mu m\ \times 1\ \mu m = 6.5\ \mu m^2$.

The device R_{ON} can be expressed as eq. 4.2 [23]:

$R_{ON} = R_{n+} + R_{ch} + R_a + R_j + R_d + R_b$

A good trade-off between the parameters N_{epi} and W_{epi} is therefore required as highlighted from the breakdown expression eq. 4.25 [23]:

$$BV_{DS} = W_{epi}^{'} \left(E_C - \frac{q N_{epi} W_{epi}^{'}}{2\varepsilon_s} \right) \tag{4.25}$$

Here, $E_C = 1.5\ MV/cm$ is the critical electric field assumed in this work, ε_s is the semiconductor dielectric constant, and q is the electron charge.

Result that the lower is the desired BV_{DS}, the higher should be N_{epi}, with consequent advantages in terms of a low R_{ON}. For the device in Table 4.6 with a W_{epi} = 8.70 μm is expected a $BV_{DS} \approx 650\ V$, and this value was verified during the simulations.

Table 4.6. MOSFET PARAMETERS.

PARAMETER	**UNIT**	**VALUE**
Silicon oxide thickness	nm	80
Source thickness, W_s	μm	0.50
Channel length, L_{ch}	μm	1.00
Base junction depth, W_{P-base}	μm	1.30
Interspace, W'_{P-base}	μm	1.00
Base-to-base distance, W_j	μm	5.00
Epilayer junction depth, W_{epi}	μm	8.70
Base-to-substrate distance, W'_{epi}	μm	0.50
Substrate thickness, W_{sub}	μm	100.00
N^+-substrate doping	cm^{-3}	10^{19}
N^+ source doping	cm^{-3}	10^{18}
N_{P-base} base doping	cm^{-3}	10^{17}
N_{epi} epilayer doping	cm^{-3}	10^{16}

Finally, for low-voltage MOSFETs ($BV_{DS} < 1\ kV$), the R_{ch} component of R_{ON} plays a key role and its value is determined by the effective carrier mobility (electrons) into the inversion layer.

The fundamental DoS parameters used for simulations are summarized in Table 4.7 [47, 72, 144, 147, 148]. In particular, the capture cross sections have been assumed as in [47]. Defect and trap effects in the channel region at the SiO_2/SiC interface are taken into account by solving the *Poisson*'s equation, which relates the variation of the electrostatic potential ψ to the local (total) charge density, in the form of eq. 4.11 and eq. 4.12.

Unfortunately, the chipmakers do not provide detailed information on the crystallographic properties of the SiC-wafers used or measures regarding the distributions of defects/traps in their semiconductor devices.

Detailed research in the literature was carried out with the aim to understand what were the range of distribution for the trap/defect densities that we could expect for a device in 4H-SiC. Thanks to the works of Roccaforte [57], Licciardo [149] and others [150] has been possible to understand the range of these distribution densities.

Table 4.7. DoS Reference Parameters.

Parameter	Unit	Value
$D_{T,C}^0$	cm^{-3}	1.0×10^{14}
$D_{T,V}^0$	cm^{-3}	4.0×10^{20}
$D_{G,C}^0$	cm^{-3}	5.0×10^{10}
$D_{G,V}^0$	cm^{-3}	1.5×10^{18}
$E_{G,C}$	eV	1.0
$E_{G,V}$	eV	0.4
U_C	eV	0.033
U_V	eV	0.050
W_C	eV	0.1
W_V	eV	0.1
v_n	cm/s	1.9×10^7
v_p	cm/s	1.2×10^7
$\sigma_{T,An}$	cm^2	1.0×10^{-16}
$\sigma_{T,Dn}$	cm^2	1.0×10^{-14}
$\sigma_{G,An}$	cm^2	1.0×10^{-16}
$\sigma_{G,Dn}$	cm^2	1.0×10^{-14}
$\sigma_{T,Ap}$	cm^2	1.0×10^{-14}
$\sigma_{T,Dp}$	cm^2	1.0×10^{-16}
$\sigma_{G,Ap}$	cm^2	1.0×10^{-14}
$\sigma_{G,Dp}$	cm^2	1.0×10^{-16}

4.15 Result about the traps

For the designed MOSFET with the parameters reported in Table 4.6 and in Table 4.7 has been evaluated the weight of traps on the electrical characteristics.

To compare the weight of traps on the forward characteristics, the curves at room and at high temperature have been graphed for a new bias voltage range (8, 12, 16) V. From Fig. 4.31 and for $V_{GS} = 8\ V$ we can assume that it is as the threshold voltage V_{TH}. The same $I_D - V_{DS}$ characteristics were simulated at $T = 473\ K$ as shown in Fig. 4.32. This is a typical operation temperature for SiC-based power devices.

From these results, it is clear that the interface defects have a strong impact in determining the MOSFET performance at any temperature, in particular, for increasing of bias condition (V_{GS}). In particular, our attention was focused on the R_{ON} value calculated assuming an operating point in the triode region for $V_{DS} = 1\ V$ similarly to [140]. The R_{ON} behaviours as a function of V_{GS} at $T = 300\ K$ and $473K$ are

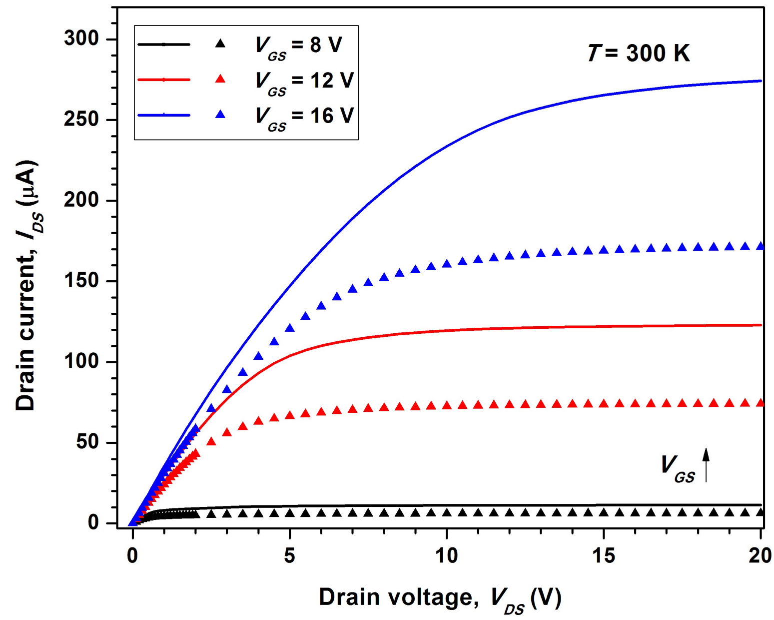

Fig. 4.31. MOSFET $I_D - V_{DS}$ characteristics for a device with trap (symbols) and no-trap (solid lines) effects at $T = 300\ K$.

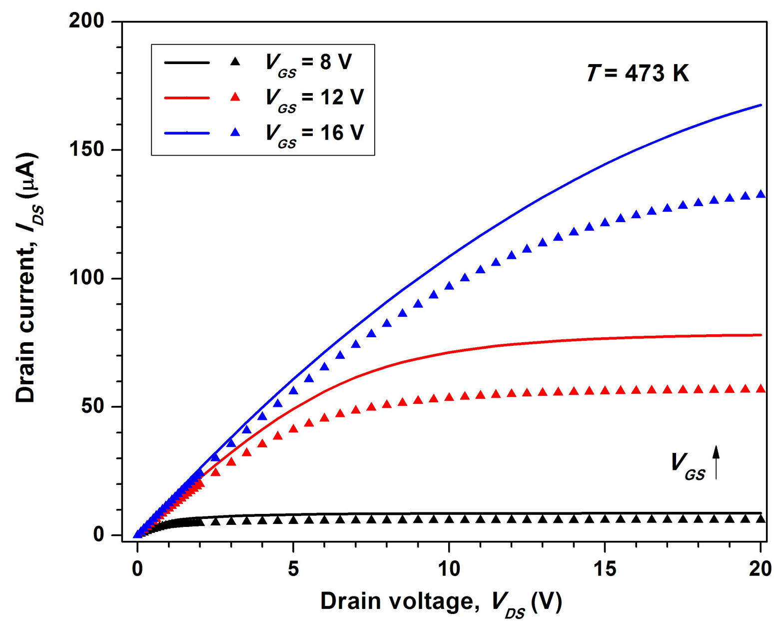

Fig. 4.32. MOSFET $I_D - V_{DS}$ characteristics for a device with trap (symbols) and no-trap (solid lines) effects at $T = 473\ K$.

shown in Fig. 4.33. One datasheet value of R_{ON} at $T = 300\ K$ is also reported for comparison [115].

The choice of this device was made considering one commercial device "similar" to ours. Unfortunately, geometry and technological information about the commercial devices are not disclosed directly by the chipmakers. But they can be deduced thanks to some data published by the Yole Développement reports and readjusted with scaling techniques to devices with different values of the breakdown voltage. [133].

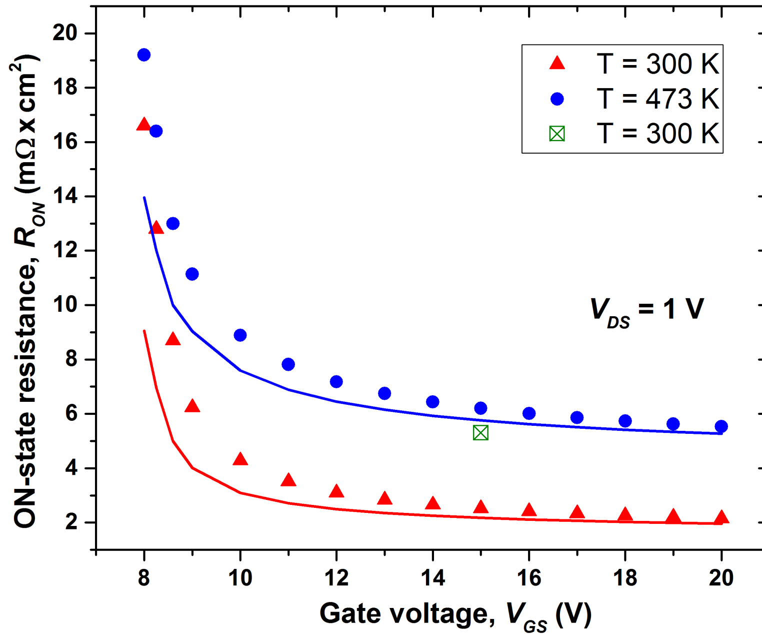

Fig. 4.33. R_{ON} behaviours as a function of V_{GS} for $V_{DS} = 1\ V$ with trap (symbols) and no-trap (solid lines) effects.

As expected, introducing the interface defect effects, the MOSFET R_{ON} increases for a fixed temperature especially for low V_{GS} voltages. This increase, however, tends to reduce for higher values of V_{GS}. More in detail, we calculated the percentage variation of R_{ON} vs. V_{GS} as shown in Fig. 4.34.

It is worthwhile noting that, in presence of a defect state distribution, the percentage variation of R_{ON} appears less severe for $T = 473\ K$ in the whole explored V_{GS} range. Moreover, a $V_{GS} > 2 \times V_{TH}$ aids to limit ΔR_{ON} in the order of 10%. The percentage variation of R_{ON} can be as high as 40% (red-line in Fig. 4.34) for low gate voltages at $T = 300\ K$.

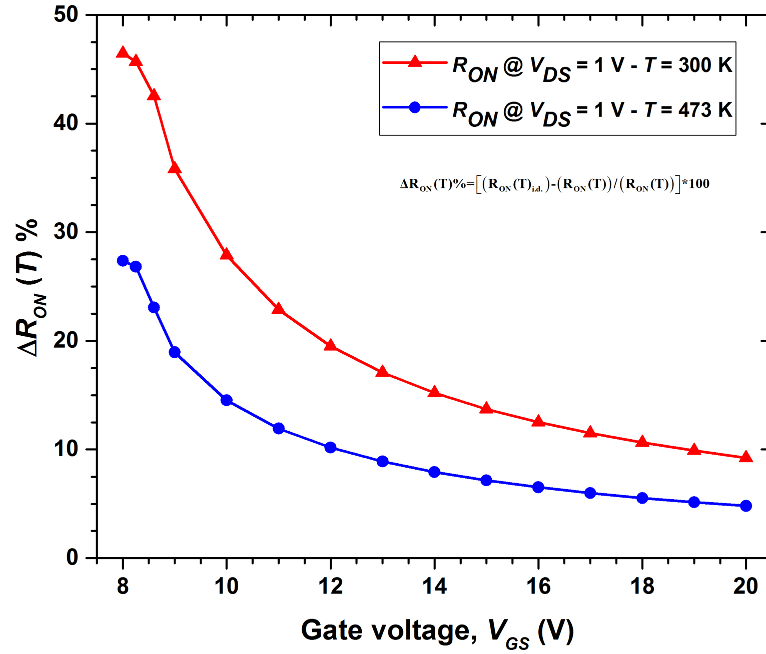

Fig. 4.34. Percentage variation of R_{ON} vs. V_{GS} introducing trap effects in the simulations.

4.16 The results on interface traps for a MOSFET structure of higher voltage-class

To continue to investigate the contribution of the traps on the electrical characteristics of the device and therefore on its performance, it was decided to simulate a device in SiC of higher voltage-class. Therefore, a modified structure was designed to support the voltage of 650 V. For this new structure, it was decided to consider as many as six different values of trap distributions. Of these values, used in literature for structures similar to ours, not all have been shown to be adequate for our device. In fact, due to higher density values, a completely negligible current flowed into the device, which is why we did not even plot the relative electrical characteristics. Thus, in order to assess the impact of traps (at room temperature), distributed at the SiO_2/SiC interface, on the MOSFET current capabilities, several simulations were performed. For the distribution of traps have been considered the typical densities well know in literature and here reported in Table 4.8 [149].

Table 4.8. Trap Densities distribution traps.

Density $(cm^{-3} \times eV^{-1})$
1.0×10^{10}
2.0×10^{10}
1.0×10^{11}
1.0×10^{12}
1.0×10^{13}
1.0×10^{14}

From a complete set of the forward characteristics (at room temperature) we extrapolated a subset of only three curves Fig.4.35 so to allow a better vision of final plots. To evaluate the impact of the traps on the performance of the device, simulations were performed with increasing density of traps, the results are shown in the following figures. It has been observed that for the electrical characteristics of the device object of this study, the distribution density present a maximum limit around the value of 10^{12} $cm^{-2} \times eV^{-1}$. Indeed, for higher density values the device stops working because traps intercept most of the entire carrier flows. The Fig.4.35 shows the forward characteristics for a device traps-free, they will be used later for a comparison with other curves. Thus, in Figure 4.36,4.37, 4.38, 4.39 has been reported the same characteristics of above but for a device affected by the traps problem. In

particular, each plot is referred to a particular density of traps. We can see that for a density of $10^{11}\ cm^{-2} \times eV^{-1}$ the device tend to turn-OFF because (for this structure with its parameters) the traps density tend to intercept the major part of the carrier.

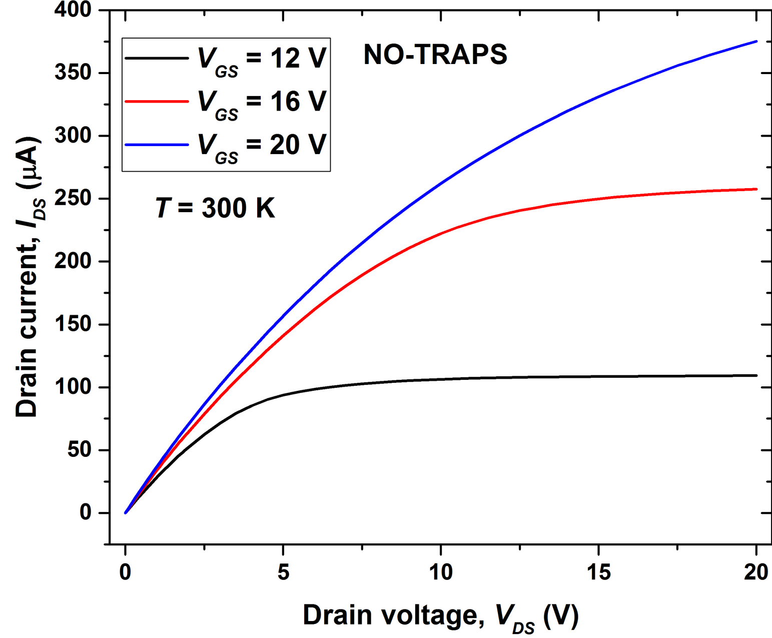

Fig. 4.35. Forward $I_D - V_{DS}$ characteristics for a traps-free device at room temperature. The geometrical and electrical parameters of the device are those listed in Table 4.7.

In Fig.4.40 is shown a comparison between a traps-free device and the same device with a density of traps of $1.0 \times 10^{11}\ cm^{-2} \times eV^{-1}$. The traps impact on the electrical characteristics its immediately evident, indeed, at $V_{DS} = 20\ V$ and for $V_{GS} = 20\ V$ there is an attenuation factor of about 8 times.

Moreover, Fig.4.41 shows the I-V curve of the traps-free device, obtained for a maximum bias voltage (considered) of 20 V, compared with other four curves obtained from the simulations for different densities' distribution traps. It is clear that an increase of trap density has a heavy impact on the device performance, just note that for $D_{it} = 10^{11}\ cm^{-2} \times eV^{-1}$ the current is about 10 times less.

Finally, has been observed the deep impact of trap distribution density on the ON-state resistance. Also, in this case, has been used the same four values of trap density aforementioned Fig.4.42. Today, producers of wafers and chipmakers suggest that it is not convenient to spend money on further technological steps with the aim to reduce the distribution density of the traps below the value of $1 \times 10^{10}\ cm^{-2} \times eV^{-1}$

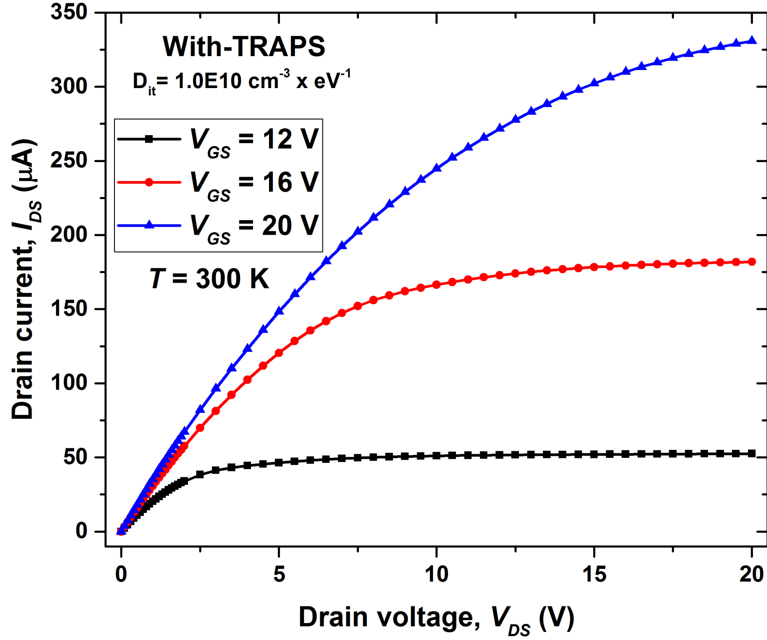

Fig. 4.36. Forward $I_D - V_{DS}$ characteristics for a trapped device at room temperature. Trap density of $1.0 \times 10^{10}\ cm^{-2} \times eV^{-1}$.

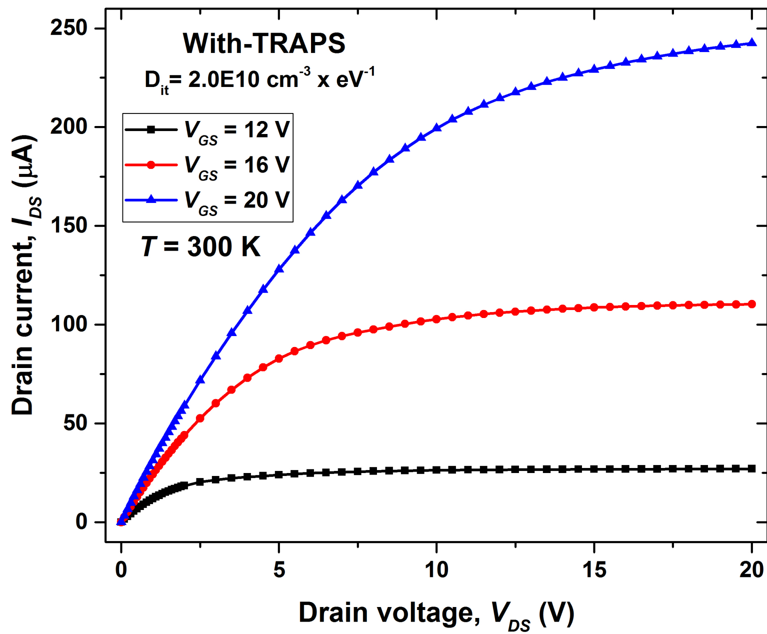

Fig. 4.37. Forward $I_D - V_{DS}$ characteristics for a trapped device at room temperature. Trap density of $2.0 \times 10^{10}\ cm^{-2} \times eV^{-1}$.

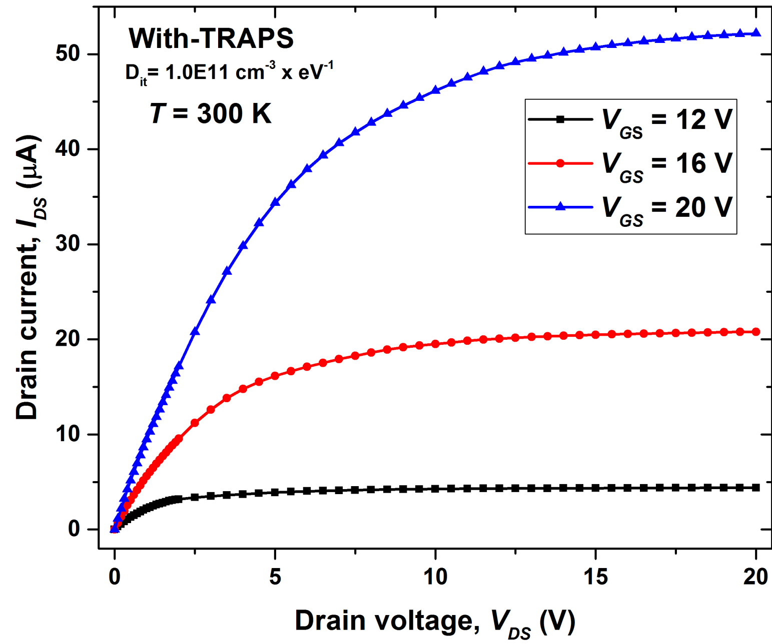

Fig. 4.38. Forward $I_D - V_{DS}$ characteristics for a trapped device at room temperature. Trap density of $1.0 \times 10^{11}\ cm^{-2} \times eV^{-1}$.

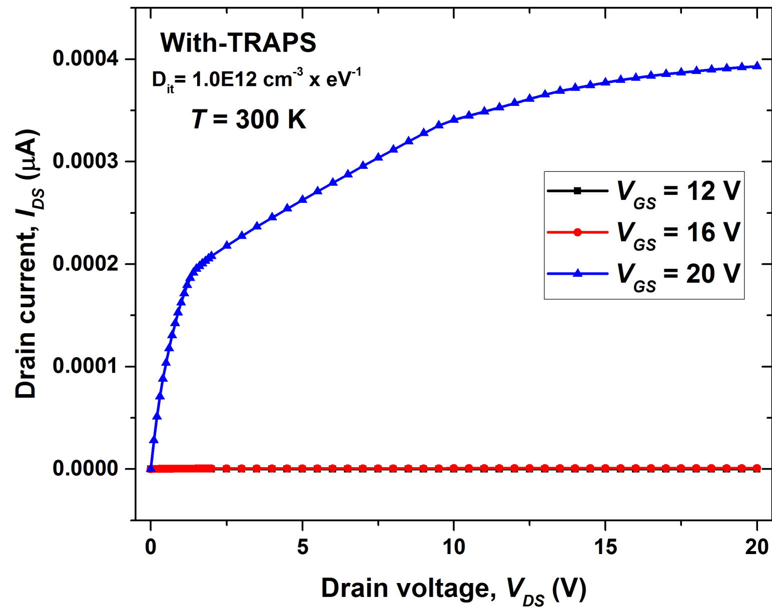

Fig. 4.39. Forward $I_D - V_{DS}$ characteristics for a trapped device at room temperature. Density of $1.0 \times 10^{12}\ cm^{-2} \times eV^{-1}$.

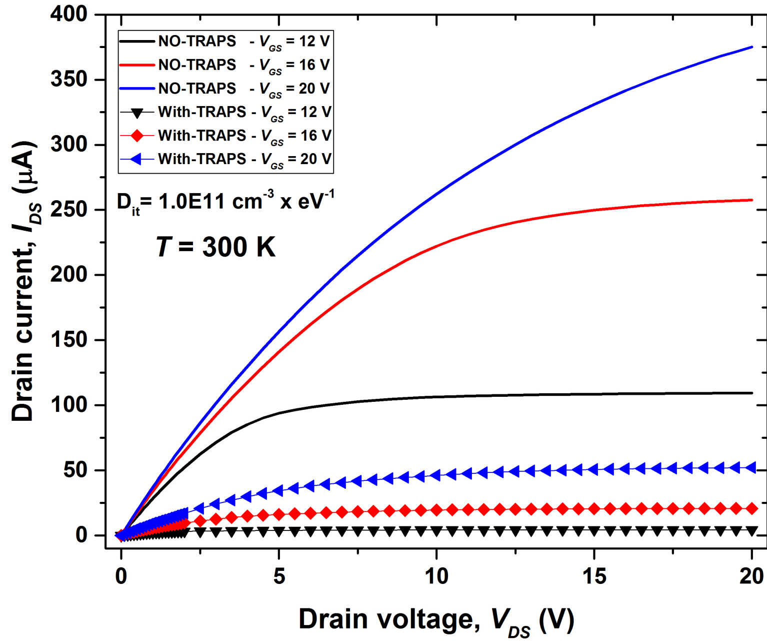

Fig. 4.40. Forward $I_D - V_{DS}$ characteristics. Comparison between the traps-free simulated device with a trapped device with a trap density of $1.0 \times 10^{11}\ cm^{-2} \times eV^{-1}$.

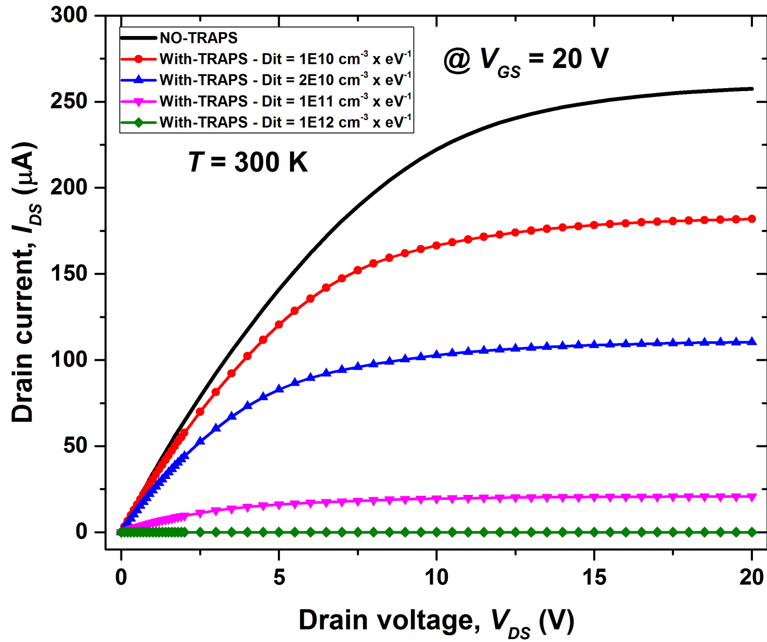

Fig. 4.41. Forward $I_D - V_{DS}$ characteristics at $V_{GS} = 20\ V$. Comparison of a traps-free device with the same device simulated for four different trap densities.

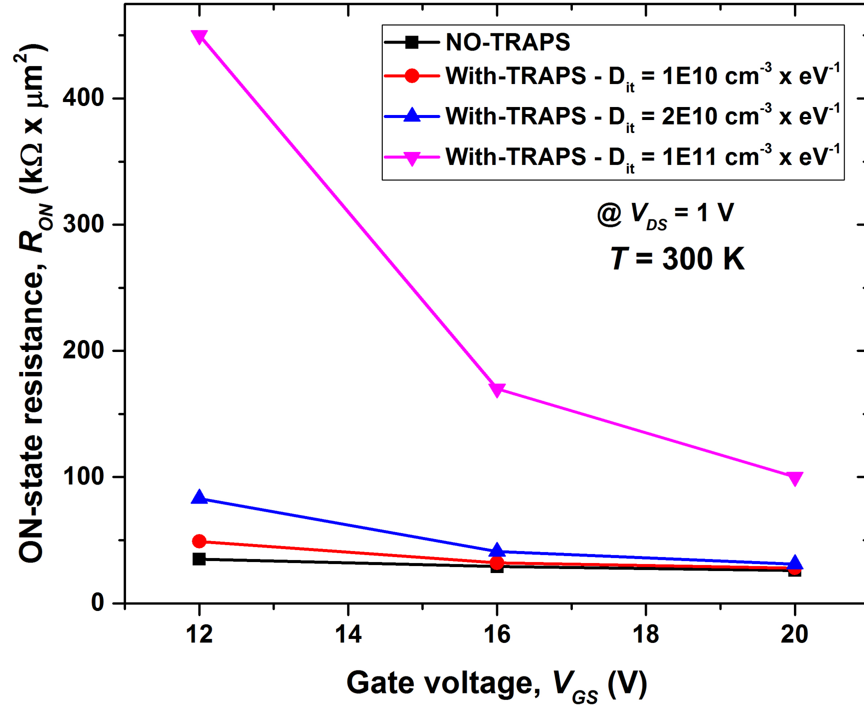

Fig. 4.42. ON-state resistance comparison of a traps-free device with the same device simulated for four different trap densities.

4.17 Comparison with other physical models

After the comparison with commercial devices reported in Table 4.4, we proceeded with the verification that our physical model, developed for the designed MOSFET, was adherent to what already existing in the literature. Unfortunately, chipmakers do not provide in their datasheets enough data regarding the traps and defects of their wafers, but they only provide a class-index-quality, without specifying details. Similarly, in the literature, researchers tend to not provide all the data characterizing the distributions of defects and traps that they have used. However, after thorough and accurate literature research, we were able to find the main parameters for structures similar to ours, but with different voltage classes.

Many parameters have been verified and varied, in some cases to adapt them to our structure; we had to use some empirical parameter, which better fitted with other values found. It was decided to make this comparison with the physical model developed by Licciardo et al. [149] in which, they have developed their own analytical model, providing the verification with both experimental and simulation data.

We performed a reverse analysis starting from their graphical results and comparing our simulations with their results. The obtained characteristics are shown in the following figures. In these plots are shown the comparison between our device

and the device of reference; the simulations have been performed and reported in the same conditions. Figure 4.43, shows a comparison between the two models at room temperature and for the bias voltage of 8 V. Figure 4.44 show the same comparison at high temperature. In this case, the according is not very good because for low bias voltage the difference between the two different voltage-class devices is more marked. Instead, Figure 4.45, 4.46 report the comparison for the bias voltage of 20 V. In both cases, results appear to be in good agreement with the data of reference [149].

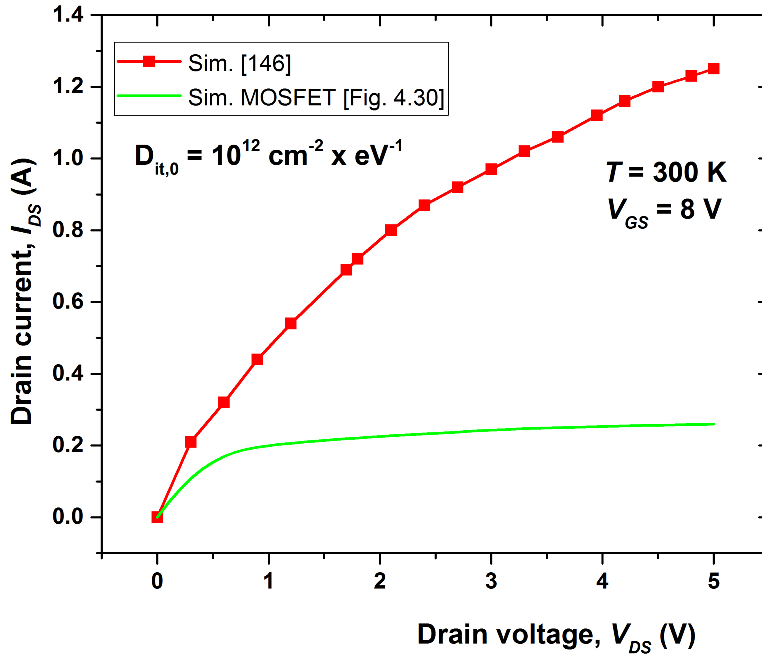

Fig. 4.43. Comparisons between the results of our physical model with that of reference. $I_{DS} - V_{DS}$ at $V_{GS} = 8\ V$ $T = 300\ K$.

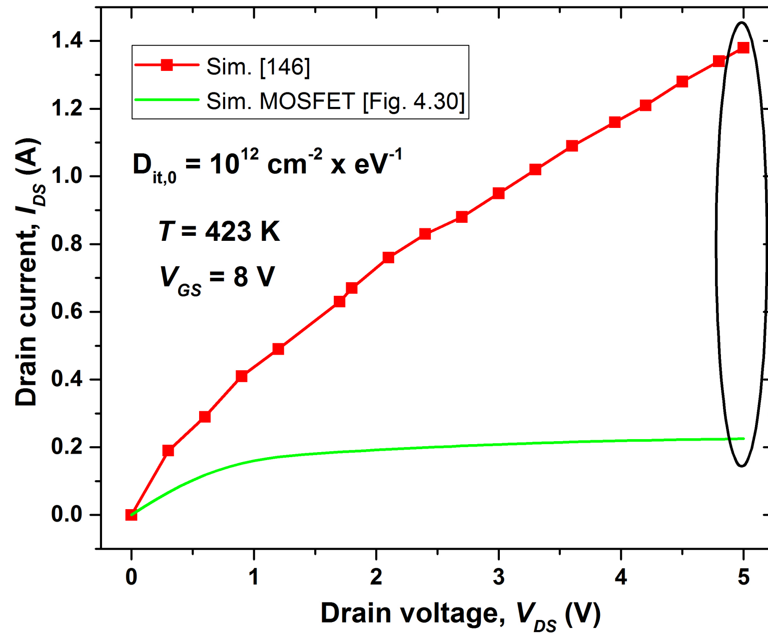

Fig. 4.44. Comparisons between the results of our physical model with that of reference. $I_{DS} - V_{DS}$ at $V_{GS} = 8\ V\ T = 423\ K$.

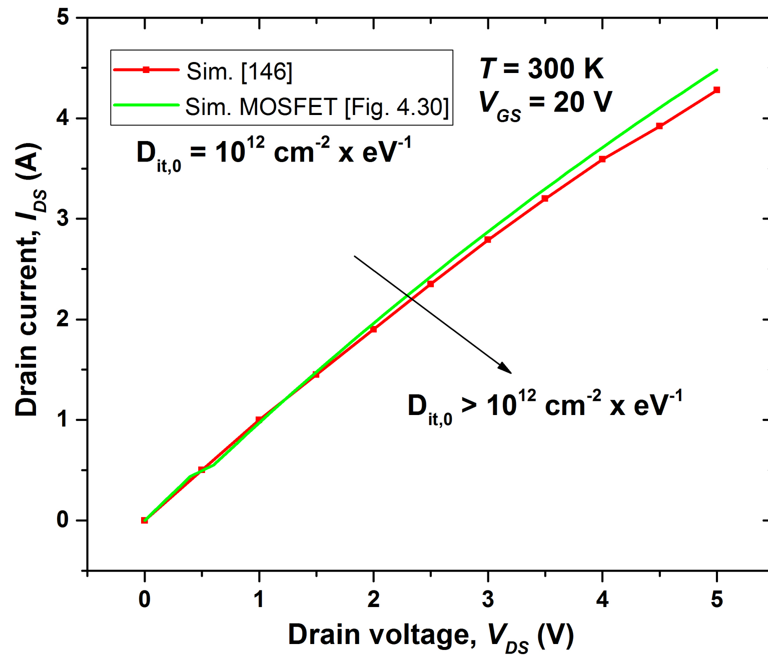

Fig. 4.45. Comparisons between the results of our physical model with that of reference. $I_{DS} - V_{DS}$ at $V_{GS} = 20\ V\ T = 300\ K$.

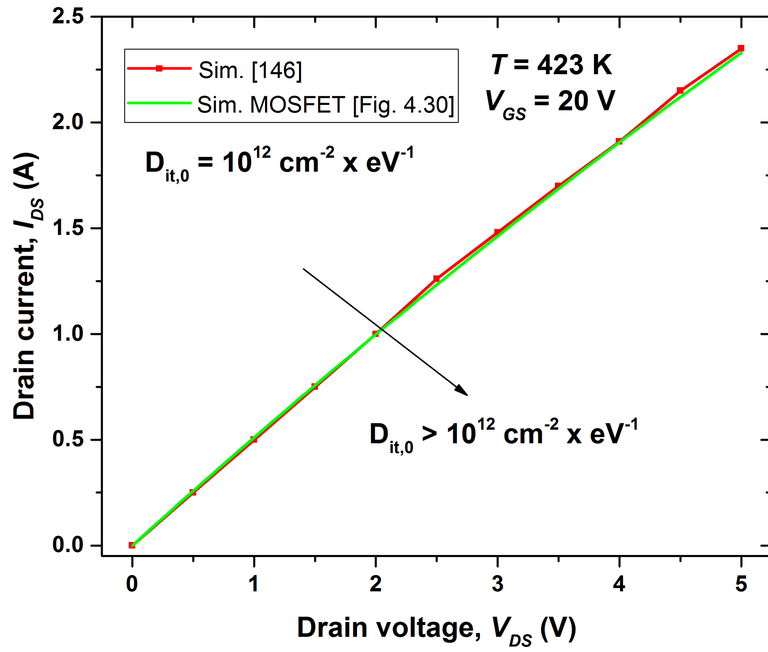

Fig. 4.46. Comparisons between the results of our physical model with that of reference. $I_{DS} - V_{DS}$ at $V_{GS} = 20\ V\ T = 423\ K$.

4.18 The results on interface defects

For the same MOSFET structure reported in Fig. 4.30 which parameters are in the Table 4.6 have been performed simulations to evaluate the weight of defects on the electrical characteristics. But, before to go ahead it is important to understand how the simulator treats these defects. More information on defects are reported in the section 3.12 and 3.14.

The fine grain structure of our polysilicon produces a large in-grain defect density; this is why our analysis is based on a continuous trap model, and we have simulated a spatially uniform density-of-states, (DoS), throughout the volume of the polysilicon layer. Our film can be considered as composed of small crystalline grains embedded in an amorphous tissue: the grain boundaries have a dimension comparable with the grain, so its properties, (E_g) and DoS, influence electron transport mechanisms, limiting, for instance, the mobility value and determining the overall electrical characteristics. We have modelled the grain boundaries as a-Si:H. It is worthwhile to point out that numerical simulation using a gap value of 1.12 eV does not fit the experimental results. Instead, the best results are obtained with E_g=1.6 eV [151]. The total DoS g(E) was modelled by the sum of two exponential tails near the conduction and the valence and two deep level bands with Gaussian distribution (one acceptor like and the other donor like). The physical model was [72]:

$$\begin{aligned} g(E) = NTA \exp\left(\tfrac{E-E_C}{WTA}\right) + NTD \exp\left(\tfrac{E_V-E}{WTD}\right) \\ +NGA \exp\left[-\left(\tfrac{EGA-E}{WGA}\right)^2\right] \\ +NGD \exp\left[-\left(\tfrac{E-EGD}{WGD}\right)^2\right] \end{aligned} \tag{4.26}$$

In Silvaco Atlas the INTDEFECTS statement is used to describe the density of defect states in the band gap at semiconductor interfaces. It is able to specify up to four distributions, two for donor-like states and two for acceptor-like states. Each type of state may contain one exponential (tail) distribution and one Gaussian distribution. Silvaco Atlas and [151] for polysilicon suggest the parameters reported in Table 4.9.

Considering the facts that the design of highly reliable, high-speed power MOSFETs is a very critical task, it is important to know how the power VDMOSFET acts when it is exposed to various stresses, such as high electric field stress. In this case, the defects in the form of traps (which can be neutral or charged), are generated in oxide and semiconductor bulk, as well as at the SiO_2/SiC interface. They significantly influence on the electrical characteristics of semiconductor devices. The traps, generated at the SiO_2/SiC interface and in the gate oxide, have the dominant

influence on the electrical characteristics of MOS transistors. Only to mention, we notice that in power VDMOS transistors the influence of traps inside the epilayer have a considerable weight on the electrical characteristics according to the fact that the current mainly flows vertically through the n-epitaxial epilayer and n^+-substrate to drain contact; but, for the line of research we have preferred to study the interface between the channel region and gate-oxide.

Table 4.9. Defects DoS Parameters.

Parameter	[151] **Value**	**Atlas Value**	**Unit**
NTA	9.20E20	1.0E21	cm^{-3}/eV
NTD	2.00E21	1.0E21	cm^{-3}/eV
WTA	0.10	0.033	eV
WTD	0.10	0.049	eV
NGA	5.0E17	1.5E15	cm^{-3}/eV
NGD	1.0E18	1.5E15	cm^{-3}/eV
EGA	0.60	0.62	eV
EGD	1.00	0.78	eV
WGA	0.40	0.15	eV
WGD	0.40	0.15	eV

Where the parameters represent:

- **EGA** Specifies the energy that corresponds to the Gaussian distribution peak for acceptor-like states. This energy is measured from the conduction band edge.
- **EGD** Specifies the energy that corresponds to the Gaussian distribution peak for donor-like states. This energy is measured from the valence band edge.
- **NGA** Specifies the total density of acceptor-like states in a Gaussian distribution.
- **NGD** Specifies the total density of donor-like states in a Gaussian distribution.
- **NTA** Specifies the density of acceptor-like states in the tail distribution at the conduction band edge.
- **NTD** Specifies the density of donor-like states in the tail distribution at the valence band edge.
- **WGA** Specifies the characteristic decay energy for a Gaussian distribution of acceptor-like states.
- **WGD** Specifies the characteristic decay energy for a Gaussian distribution of donor-like states.

- **WTA** Specifies the characteristic decay energy for the tail distribution of acceptor-like states.
- **WTD** Specifies the characteristic decay energy for the tail distribution of donor-like states.

During the last three decade, numerous papers and reports dealing with the degradation of the electrical characteristics of semiconductor devices due to different stress conditions have been published. Inside those suggested physical models was considered that the presence of defects inside semiconductor substrates was neglected because in Silicon MOS structures the defects generated in the gate oxide and at the SiO_2/Si interface have the dominant influence on the electrical characteristics.

In VDMOS structures their influence could not be ignored, because of vertical current flow. As already mentioned, traps which are generated, for example, due to the application of high electric field on the gate electrode of MOSFET, can significantly affect its electrical characteristics. As it is well-known, in these cases the defects or traps are formed at the SiO_2/SiC interface, as well as in the oxide and semiconductor bulk. The subjects of intensive research are the mechanisms of traps generation and the determination of their densities and charges (positive, negative or neutral). It is not easy to separate the traps (Donor-Traps, DT or Acceptor-Traps, AT) contribution from the contribution of defects. In addition, defects, according to the conditions, can assume an electric charge, and thus assume a behaviour as donor or acceptor. This problem can be solved efficiently by using the Silvaco Atlas software, where it is possible to separate the influences of different types of defects on the device electrical characteristics.

The large density of defect states (D_{it}) present at the interface between 4H-SiC and its native oxide SiO_2 has so far hindered the development of SiC-based devices [44]. In particular, the D_{it} shows large values just below the conduction band edge of 4H-SiC [44] [152] [153] [154], suggesting that the defects responsible for the electrical degradation situate in this energy range. In the designed n-channel Vertical DMOSFET, the drain current goes through the channel and flows vertically inside the drift region and n^+-substrate. In this case, the AT at the interface tend to influence the electrical characteristics (Fig.4.47), reducing drain current that flows through the channel. We simulated the electrical characteristics, firstly with DT, for different values of its densities (NDT), then with AT, for different values of its densities (NAT), and finally when both trap types are present in the channel region. The obtained simulation results for given values of NDT and NAT, for fixed energy trap level values,

are shown in Fig.4.48. We have observed that in the n-channel device the DT have a very negligible impact on the device performance.

Figure 4.49 shows the weight of acceptors on the electrical characteristics at very high-temperature. The green-line is the curve obtained with a trap-free device. Increasing the densities of acceptors we assist in a reduction of current a thus to an increment of R_{ON}. Moreover, it has been observed, for an n-channel device, that distributions of acceptor-type traps tend to worsen the electrical characteristics of the device and increase the threshold voltage. The data concerning this behaviour have been observed for a test-device of different voltage-class and with slightly different geometric and physical parameters from those of the devices reported here. For this reason, we preferred to omit this data, which would not have been contextualized to the discussed devices.

Finally, in Fig.4.50 is reported the comparison among the trap-free device (at room temperature) and the defected device at three different temperatures. It is clear that increasing temperature we assist in a reduction of drain current. It is important to take in mind that for this device the value of NTA=1.0^{13} cm^{-3}/eV could be considered a limit value because for a higher value of NTA in the device flow only a negligible current. Therefore, for a device with n-channel, the donors have a very minimal impact on the device performance.

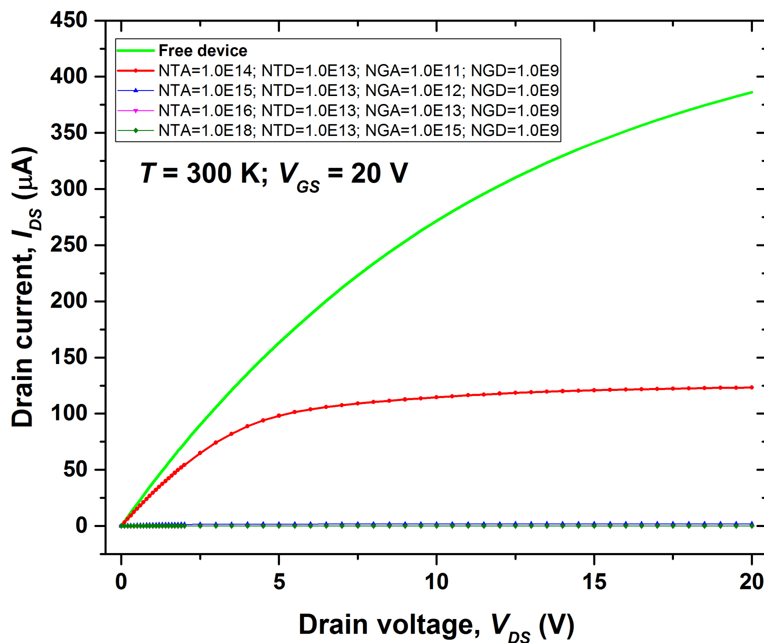

Fig. 4.47. Forward characteristics at room temperature. The line in green-light refer to a defect-free device. Other colours are used for different defect-distributions

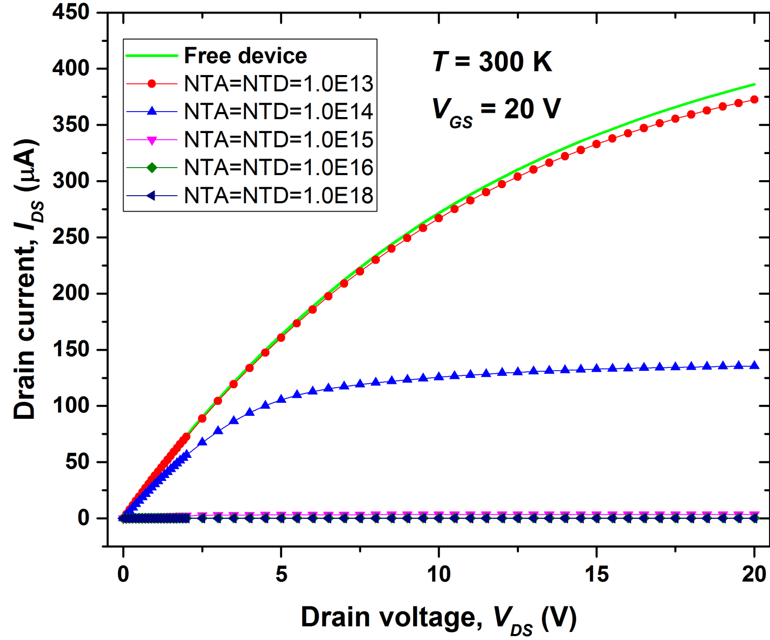

Fig. 4.48. Forward characteristics at room temperature. The line in green-light refer to a defect-free device. NTA=NTD. Other colours are used for different defect-distributions

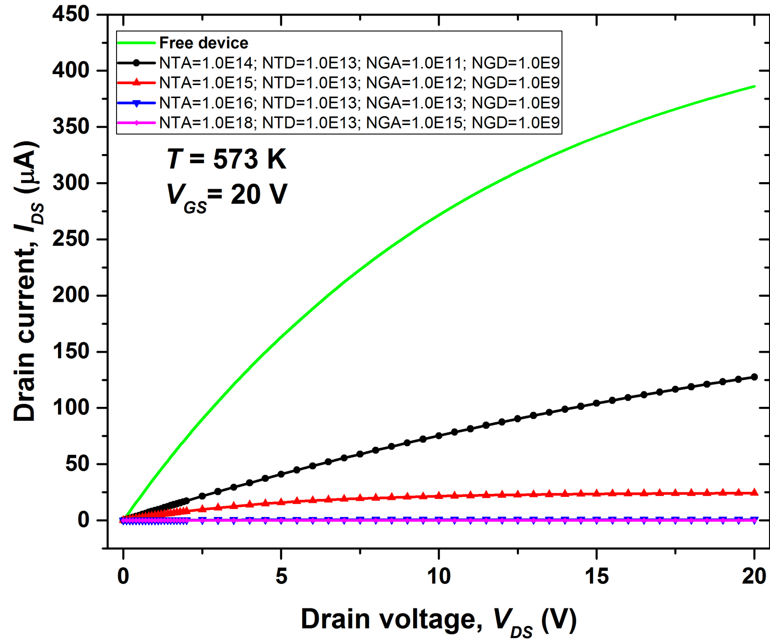

Fig. 4.49. Forward characteristics at very-high-temperature. The line in green-light refer to a defect-free device. Other colours are used for different defect-distributions.

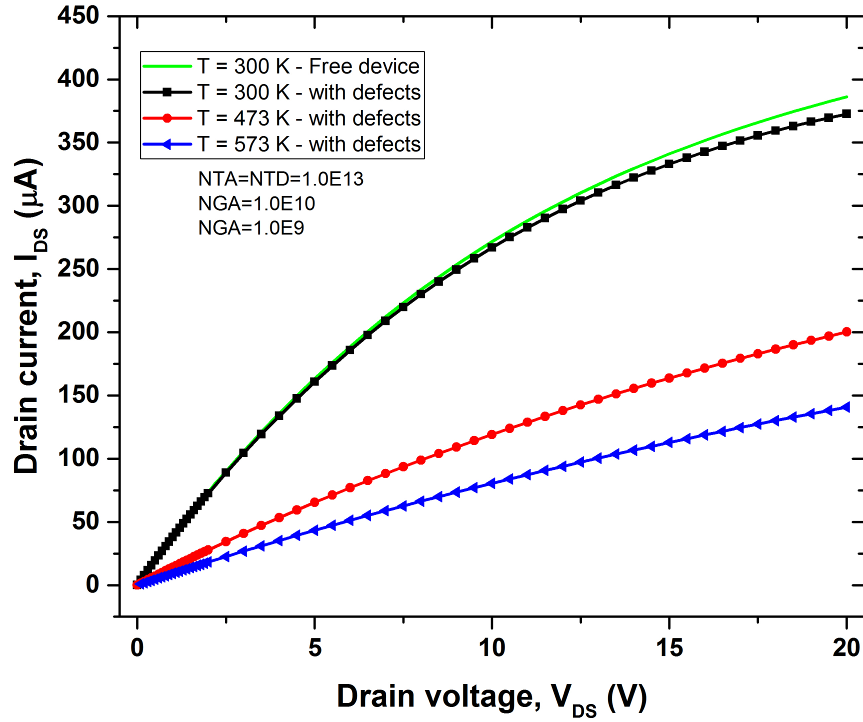

Fig. 4.50. Forward characteristics at very-high-temperature. The line in green-light refer to a defect-free device. Other colours are used for the same defect-distributions, but, for three different temperature.

4.19 The results on the contribution of traps and defects at MOSFET interface

4.19.1 Device free of defects and traps

For the same MOSFET structure reported in Fig. 4.30 which parameters are in the Table 4.6 have been performed simulations to evaluate the electrical characteristics under the conjoint weight of defects and traps. But, before to go ahead it is important to understand how the simulator treats these defects. More information on defects and traps are reported in chapter 3 from the section 3.12 onwards.

First of all, the designed 4H-SiC MOSFET without interface defects and traps has been simulated in the temperature range from 300 K to 573 K.

The current-voltage ($I_D - V_{DS}$) output characteristics of the studied device (V_{DS}= 650 V) at the room and high temperature, nearby and within the triode region, are respectively shown in Fig. 4.51, and Fig. 4.52 for $V_{GS} = 8 \div 20\ V$.

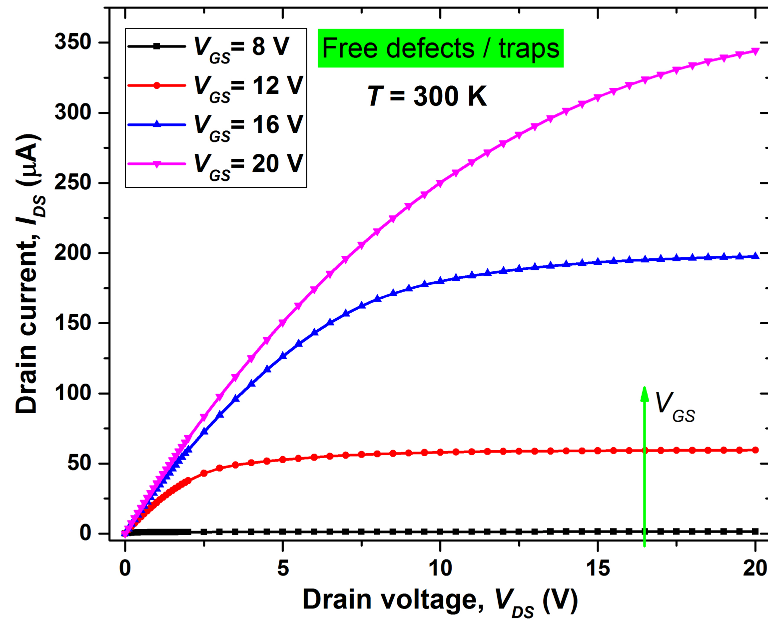

Fig. 4.51. Forward $I_D - V_{DS}$ characteristics at $T = 300\ K$.

The R_{ON} behaviour was calculated at two different temperatures, namely T = 300 K and 573 K, are shown in Fig. 4.53 as a function of the V_{GS}. The two red-lines represent the relative ON-state resistance, and the red-dotted-blue-line report for these two temperature, the percentage variation ($\Delta R_{ON}\%$) of the ON-state resistance. The same figure shows that increasing the bias voltage, consequently increase the percentage variation of the ON-state resistance $\Delta R_{ON}\%$. Its range extends from about

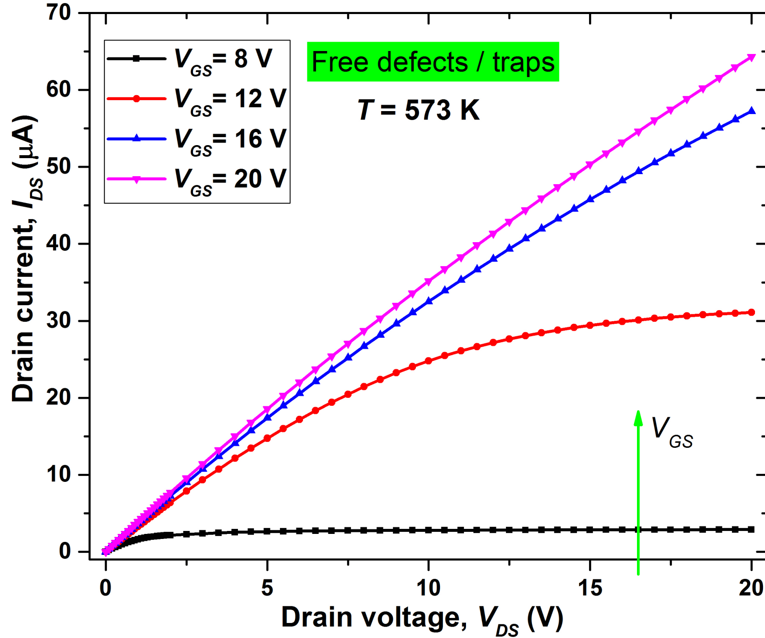

Fig. 4.52. Forward $I_D - V_{DS}$ characteristics at $T = 573\ K$.

97% at $V_{GS} = 8\ V$ to more of 300% for $V_{GS} = 20\ V$, meaning a severe impact of temperature on the MOSFET current capabilities [23].

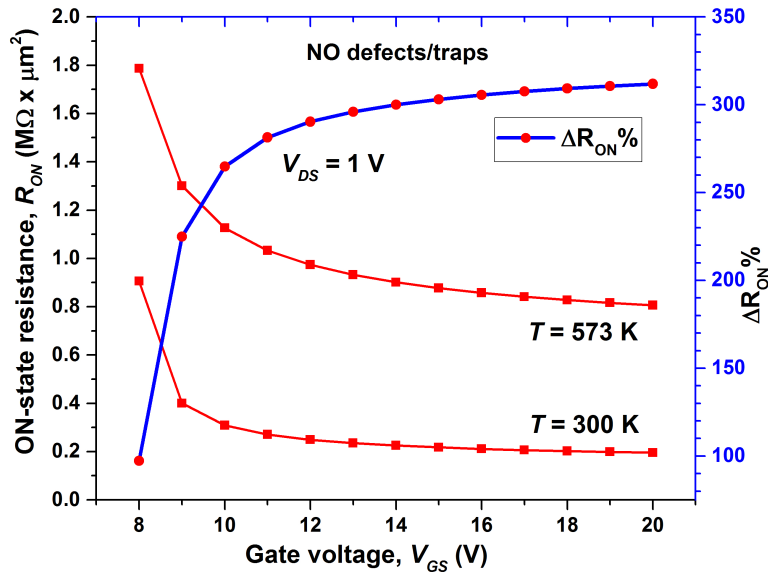

Fig. 4.53. ON-state resistance at $T = 300\ K$ and $573\ K$ versus the gate voltage.

After the presentation of electrical performances, it needs to be further investigated, for example at different operating temperatures. But, before continuing, it is important to specify which other parameters of the physical model have been con-

sidered, so will be possible to give an explanation of the phenomena involved at the interface with the gate oxide.

In the section 3.12 has been discussed the origin of defects and traps of wafers and the problems that they inflict to the produced electronic devices. This is a general problem of the semiconductors industry, regardless of the material with which the wafer is made. Although each material has several advantages and disadvantages, that of crystalline defects is a transverse problem that can be only mitigated in different percentages depending on the type of material and mainly of its purification degree. In the same section, the main technological solutions adopted by the wafers' producers are dealt with briefly. The solutions adopted by the chipmakers to further mitigate the formation of defects/traps due to technological processes as (e.g. diffusion, implantation, etching, etc...) vary according to the type of devices to be produced. For power devices, this problem is studied and dealt with very seriously, not only to improve the device performance but also to avoid premature breakage of the same device.

4.19.2 Physical models: density trap distributions and defects as charges in oxide

SiC MOSFETs have a very large number of interface traps that are spread over the entire bandgap causing degradation of device performance [141]. Interface trap density of states inside the 4H-SiC semiconductor bandgap is modelled as consisting of two components. One component is trap states in the middle of the bandgap that have a constant density with energy. The other component, which consists of traps near the band edges, is modelled as the tail of a distribution of traps, the maximum of which lies in the conduction band (valence band) [155]. These band-tail states are very large in number and give rise to a huge population of occupied traps at the interface. The temperature dependent density of acceptor-type interface traps located in the upper half of the bandgap can be written as [71, 156]:

$$D_{it}(E_t, T) = D_{it}^{mid} + D_{it}^{edge}(T) \exp\left(\frac{E_t - E_C}{\sigma(T)}\right) \tag{4.27}$$

We proceeded to allocate, inside the device and particularly at the interface between the channel MOSFET and the gate oxide, appropriate defects and traps distributions. In Figs. 4.54,4.55 are reported respectively the "Acceptor Bump Density" and the "Donor Bump Density" as the function of bandgap energy. In this case, is

important not only the single carriers density but also their net differences. The simulation parameters WTA and WTD indicate with "σ" represents respectively the characteristic decay energy for the tail distribution of acceptor-like states and the characteristic decay energy for the tail distribution of donor-like states.

Where E_t is the energy level inside the bandgap, E_C is the conduction band energy, T is the temperature, D_{it}^{mid} is the midgap interface trap density of states, $D_{it}^{edge}(T)$ is the band-edge interface trap density of states, and $\sigma(T)$ is the temperature dependent band tail energy parameter that governs the distribution of the states close to the band edge. A similar expression can be written for the donor states located in the lower half of the bandgap. The number of occupied traps as a function of temperature depends on the location of the surface *Fermi* level. The temperature dependent density of occupied acceptor-like interface traps at a given position x along the interface is then given by [155]:

$$N_{it}^{acc}(x,T) = \int_{Eneutral}^{E_C} D_{it}(E_t,T)\, f_t(x,E_t,T)\, dE_t \tag{4.28}$$

where $E_{neutral}$ is the neutrality point for the traps. We take the neutrality point to be the centre of the bandgap. As there is current flow in the MOSFET in the x-direction (along the channel), the surface $Fermi$ level varies with position x. Therefore, we use the $Fermi$ distribution function $f_t(x,E_t,T)$ governed by the position dependent electron quasi-*Fermi* level $E_F^n(x)$ to evaluate trap occupation along the interface. The quasi-*Fermi* level for electrons is calculated from the local electron concentration at the surface (n(x,0)). A similar equation is used to calculate the occupied donor-type interface traps by writing the distribution function using the hole quasi-*Fermi* level $E_F^p(x)$ which is calculated by using the surface hole concentration (p(x,0)). To characterize 4H-SiC MOSFETs, Silvaco Atlas to extract the values for the physical parameters D_{it}^{mid}, $D_{it}^{edge}(T)$, and $\sigma(T)$ and to specify their dependence on temperature. With the increase in temperature, the separation between the surface dangling bonds increases, leading to a variation in the potential energy, and the tail of the density of states for the traps located in the conduction band (valence band in case of donor states) spreads deeper into the bandgap.

This is reflected in the extracted temperature dependence of band-tail energy parameter WTA or WTD ($\sigma(T)$), as shown in Table 4.10. The increase in temperature causes bandgap narrowing, thereby moving the conduction band closer to the valence band. As a result, there is a reduction in the value of the band-edge density of states ($D_{it}^{edge}(T)$) with the increase in temperature (Table 4.10).

Table 4.10. Simulation parameters: density trap distributions and charges in oxide

Parameter	**Symbol**	**Units**	**T=300 K**	**T=373 K**	**T=473 K**	**T=573 K**
Midgap Trap DoS	D_{it}^{mid}	$cm^{-2}eV^{-1}$	5.0×10^{10}			
Band-edge Trap DoS	D_{it}^{edge}	$cm^{-2}eV^{-1}$	1.0×10^{14}	0.2×10^{14}	9.2×10^{13}	8.9×10^{13}
Band-tail Energy	σ	meV	33	47	67	87
Charges in Oxide: Q_f, Q_T	$N_f + N_T$	cm^{-2}	$1.0 \times 10^{8} \div$ 1.0×10^{12}			

Accurate simulation have given an interface charge distribution in the oxide of $Q_f = 3 \times 10^{10}\ C/cm^2$; this is a typical value for the interface charge found in SiC MOSFET devices.

Now it is interesting to evaluate the physical model when the interface charges changes. For this aim, we have simulated the device adding extra trapped charges directly at the interface.

These charges are positioned at the interface so that they directly affect the device performance; by degrading the channel mobility and increasing the channel resistance contribute. The interface trap density (D_{it}) for 4H-SiC has shown a flat distribution in the middle of the bandgap and an exponential increase near the band edges [155,156].

The parameters WTA or WTD ($\sigma(T)$) determines the $D_{it}(E_t)$ curve-shape, as reported in Fig. 4.56. It shows the energy distribution of interface states at room temperature. From this last figure and from eq. 4.27 it is evident that for a larger $\sigma(T)$ the traps distribution tend to be more centrally located inside the bandgap. The trap capture cross section for electrons and holes are respectively "$SIGN = 2.84 \times 10^{-15} cm^2$" "$SIGP = 2.84 \times 10^{-14} cm^2$".

4.19.3 Results on defects and traps

Simulation of the electrical characteristics led to the evaluation of R_{ON}, calculated at $V_{DS} = 1\ V$ and for six different intermediate temperatures in the range of ($293\ K \div 573\ K$). From Figs. 4.57, 4.58 it is clear that by increasing the temperature, the mobility is reduced, and therefore increases the R_{ON}.

For the simulated device in 4H-SiC has been obtained a reference value for total charges of about $Q_T = -10^8\ C/cm^2$. Therefore, we have proceeded to evaluate how the R_{ON} could change for different value of charges distribution Q_T positioned at interface with gate oxide. Thus, we have considered five different charge distributions in *Poisson*'s equation from $Q_T = -10^8\ C/cm^2$ to $Q_T = -10^{12}\ C/cm^2$ as reported in the Figs. 4.57 to 4.60.

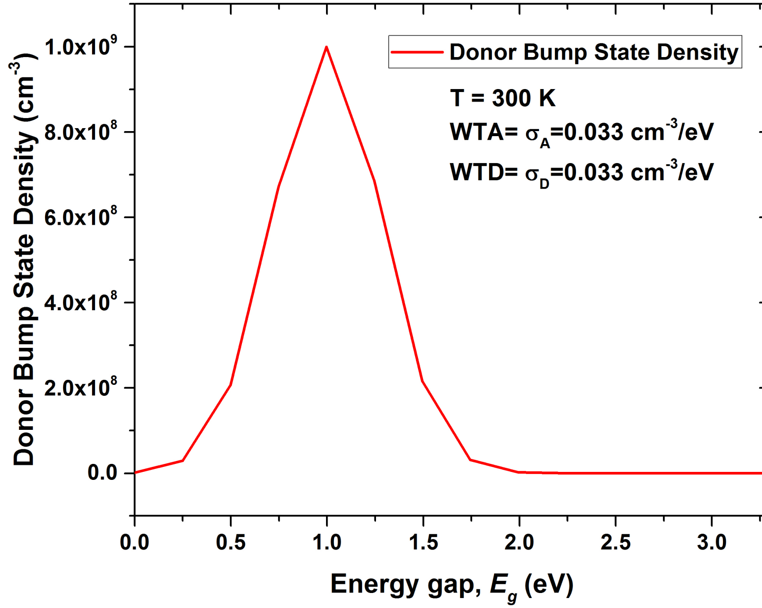

Fig. 4.54. Trap-donor: Bump density at the interface.

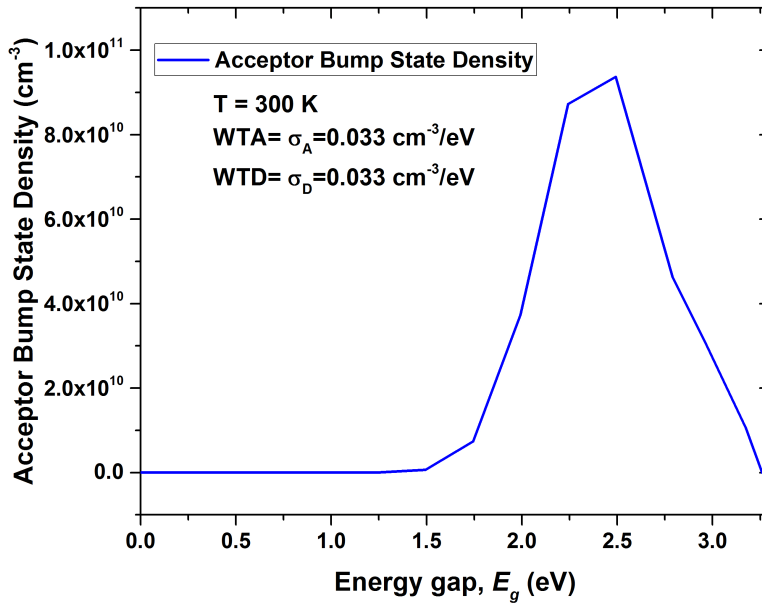

Fig. 4.55. Trap-acceptor: Bump density at the interface.

These charge distributions are directly linked with the doping of all the semiconductor interface junctions with the gate oxide, for this reason, its effect become important only for $|Q_T| > 10^{11}$ C/cm^2 as shown by the green-line in the Figs. 4.57 at room temperature, and 4.58 at high temperature. It is important to consider carefully the effects of the distribution charges; indeed, at $V_{GS} = 14$ V the R_{ON} increases in manner less evident for $Q_T = -10^8$ C/cm^2 to $Q_T = -10^{11}$ C/cm^2, instead it increases

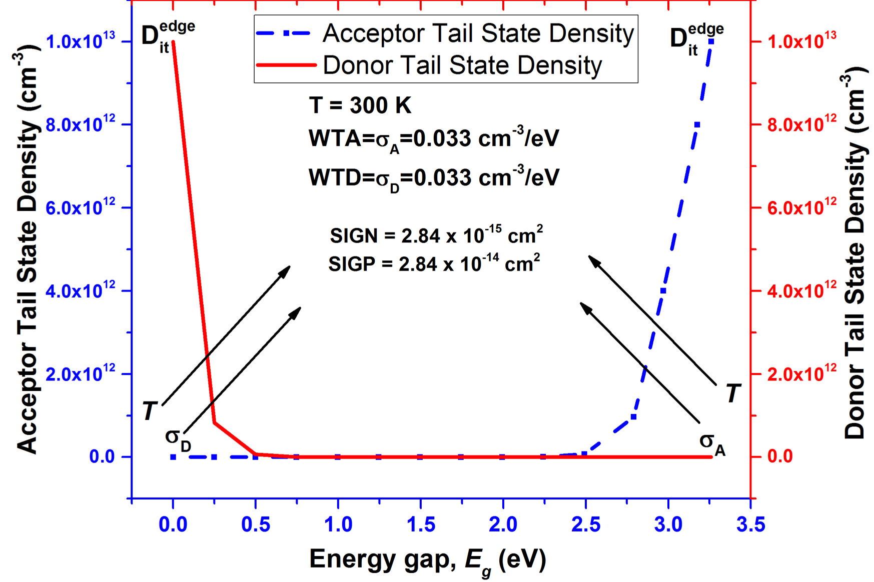

Fig. 4.56. Interface tail state density, for donor (red-solid-line) and acceptor (blu-dash-line), versus the energy bandgap.

greatly when $Q_T = -10^{12}\ C/cm^2$, which value become to influence the semiconductor doping at the interface.

The reduction of R_{ON} with temperature, highlighted in Figs.4.57,4.58 is tied to the mechanisms of scattering at phonons that influence the mobility. Phonons are an expression of the thermally stimulated lattice vibrations, its contribute increase with temperature (about $T^{3/2}$) [23]. Thus, scattering at phonons dominates at high temperatures, while scattering at dopant atoms may dominate at lower temperatures.

In Figs. 4.59 (room temperature), 4.60 (high temperature) are shown the drain current density. Obviously, at both temperatures the J_{DS} are influenced by the high interface charge density.

Thus, for a negative $Q_T = -10^{12}\ C/cm^2$ the MOSFET voltage threshold at $T = 573\ K$ tend to shift to lower V_{GS}, and thus the relative J_{DS} tends to increase, this leads to a R_{ON} reduction and consequently to better device performance.

Instead, for a positive $Q_T = +10^{12}\ C/cm^2$ the MOSFET voltage threshold at $T = 573\ K$ it tends to move slightly to higher V_{GS}, and thus the relative J_{DS} tends to decrease, this leads to a little increase of R_{ON} and consequently to the worst device performance.

Temperature influence all the component of R_{ON}, so the channel resistance R_{ch} and the JFET component R_{JFET} play an important role at high temperature in determining the R_{ON}. Thus, R_{JFET} is given by [23]:

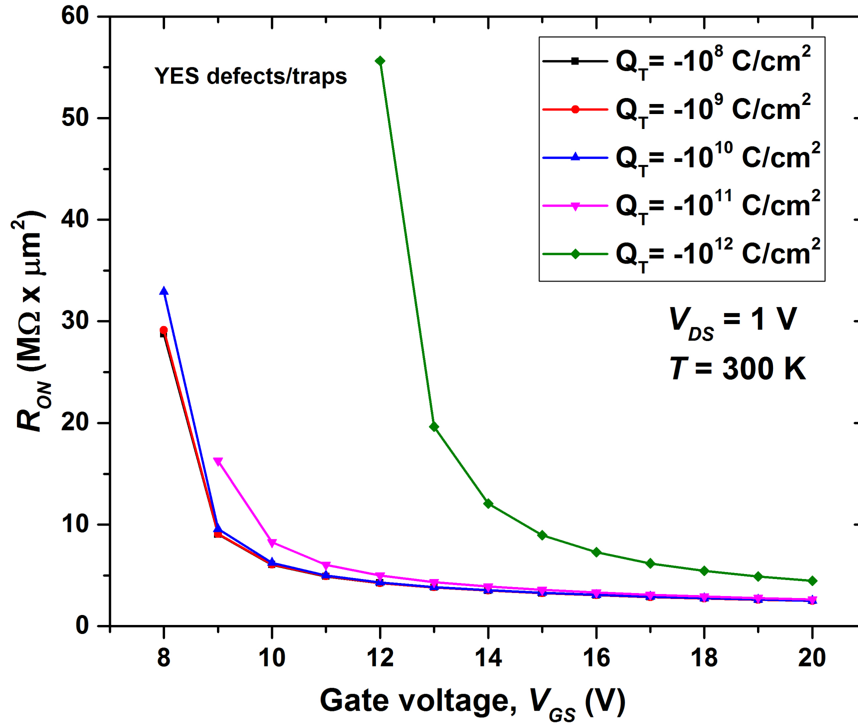

Fig. 4.57. ON-state resistance at room temperature for a simulated device with traps and defects as function of bias voltage and for different total charge densities.

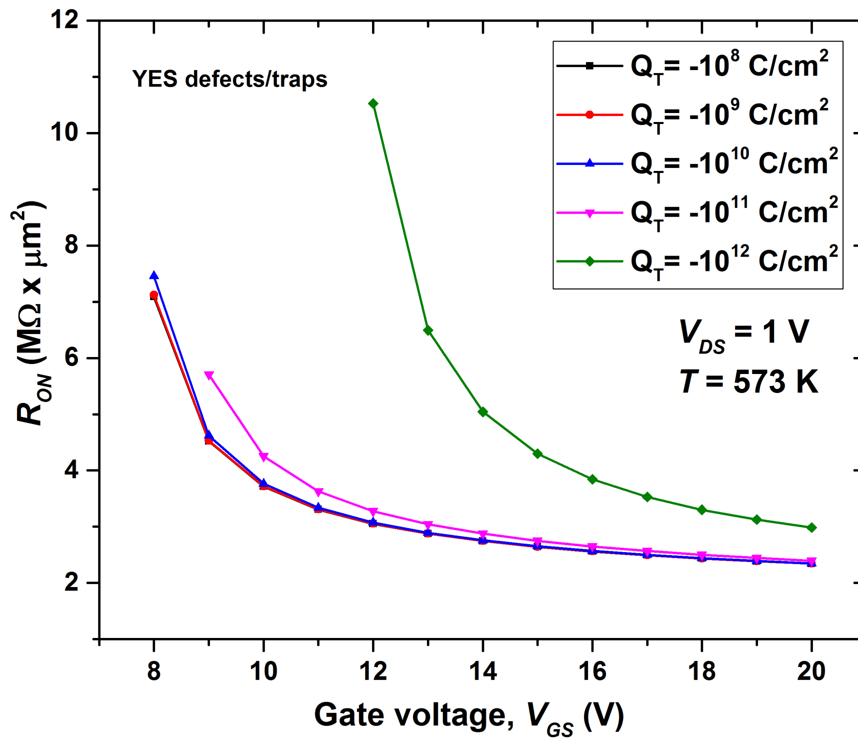

Fig. 4.58. ON-state resistance at high temperature ($T = 573\ K$) for a simulated device with traps and defects as function of bias voltage and for different total charge densities.

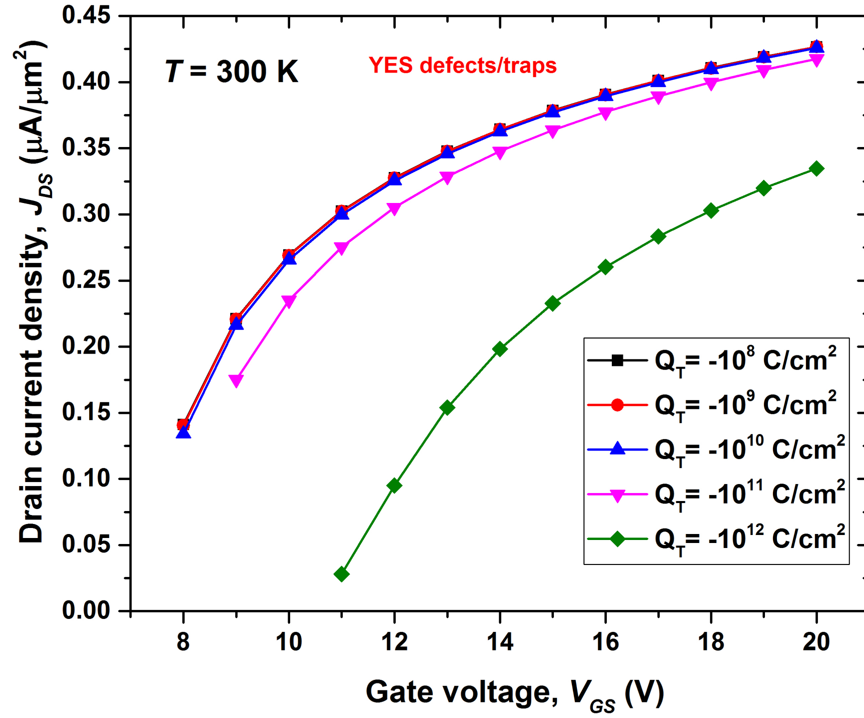

Fig. 4.59. Drain current density at room temperature for a simulated device with traps and defects as function of bias voltage and for different total charge densities.

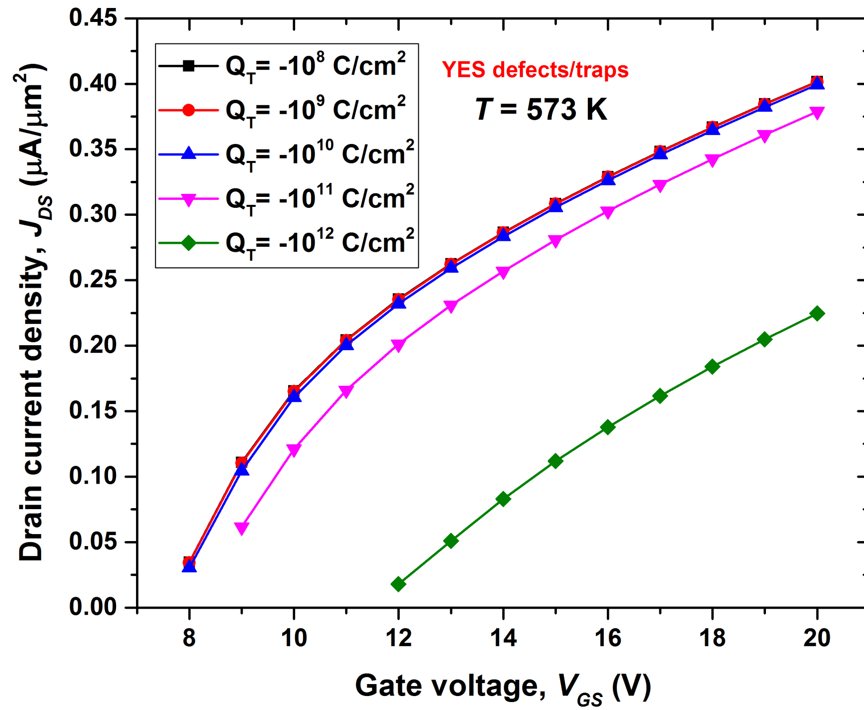

Fig. 4.60. Drain current density at high temperature ($T = 573\ K$) for a simulated device with traps and defects as function of bias voltage and for different total charge densities.

$$R_{JFET} \propto \frac{1}{\sqrt{V_{bi}}} \tag{4.29}$$

With

$$V_{bi} = \frac{KT}{q} \cdot \ln\left(\frac{N_A N_{DJ}}{n_i^2}\right) \tag{4.30}$$

where N_A is the doping concentration in the P-base region and N_{DJ} is the doping concentration in the JFET region, and V_{bi}, the built-in potential is related to the doping concentrations on both sides of the junction.

From these last equations, it is clear that increasing the temperature of the device, decreases the value of the built-in potential V_{bi} (Fig.2.13) and consequently, R_{JFET} increases by the factor $T^{-1/2}$, and ultimately, this tend to increases the value of the R_{ON}.

4.19.4 How temperature and scattering effects influence ON-state resistance

Simulations results and the physical models adopted have shown that the variation of temperature has two main effects on the carrier transport properties inside the channel MOSFET.

The first effect is relative to a change in the contributions of the scattering mechanisms and so to the channel mobility. The device performance of a SiC MOSFET is limited by *Coulomb* scattering with ionized impurities (in the bulk and at the charged interface) as well as by surface-roughness, surface-phonon and bulk-phonon scattering, Fig4.61.

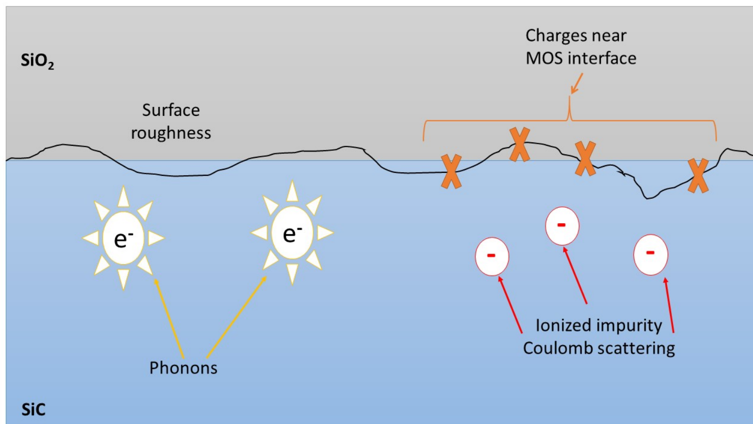

Fig. 4.61. Schematization of the scattering effects at the SiO_2/SiC interface.

Each kind of scattering mechanisms has its specific temperature dependence. When temperature increases, *Coulomb* scattering decreases and phonon scattering increases. Therefore, the dependence of mobility on temperature is strongly linked with the dominant scattering mechanism in the MOSFET inversion channel.

The second effect of temperature is a change of the bulk potential and, consequently, of the interface traps distribution, in this case, a temperature increment leads to a decrease of bulk potential. Two scattering mechanisms, bulk-phonon scattering and *Coulomb* scattering at ionized impurities determine the mobility in the bulk region. In the n-channel 4H-SiC MOSFET it is often assumed that *Coulomb* scattering at the charged interface is always the dominant scattering mechanism due to the high trap density distribution. In this case, the drain current increase with temperature. Instead, reducing temperature there will be a different dominant mechanism in the scattering process of the 4H-SiC MOSFET channel. The *Coulomb* scattering at the charged interface is the dominant scattering mechanism at the room temperature inside the n-channel of the SiC MOSFET, but with increasing temperature, *Coulomb* scattering at the charged interface decreases, and consequently the mobility increase with temperature.

A higher *Coulomb* scattering rate at the charged interface is mainly due to two effects:

- The first one is linked to an increase in the "trap density", where this effect is due to the change of the bulk potential with temperature.
- The second effect is linked to an increase of the "scattering centres" where this effect is due to the increment of free electrons' density inside the inversion channel.

In other words, considering that the process of *Coulomb* scattering decreases with the temperature, result that the channel mobility and the drain current I_D also increases and consequently the R_{ON} decrease with temperature, as observed in Figs. 4.57, 4.58.

In Fig. 4.62 is shown the R_{ON} behaviour at room temperature and at high temperature (573 K) for the designed devices, simulated considering the physical models with and without defects and traps distribution at the interface between inversion channel and gate oxide.

The black-line and red-line refer to device free of defects and traps, which trend has been already shown in Fig. 4.53 . The orange-line and blue-line of Fig. 4.59 demonstrate that the presence of defects and traps play a role very important in the determination of a low R_{ON} value which trends are reported in Figs. 4.57, 4.58. As expected, the interface with the distributions of defects and traps affect the perfor-

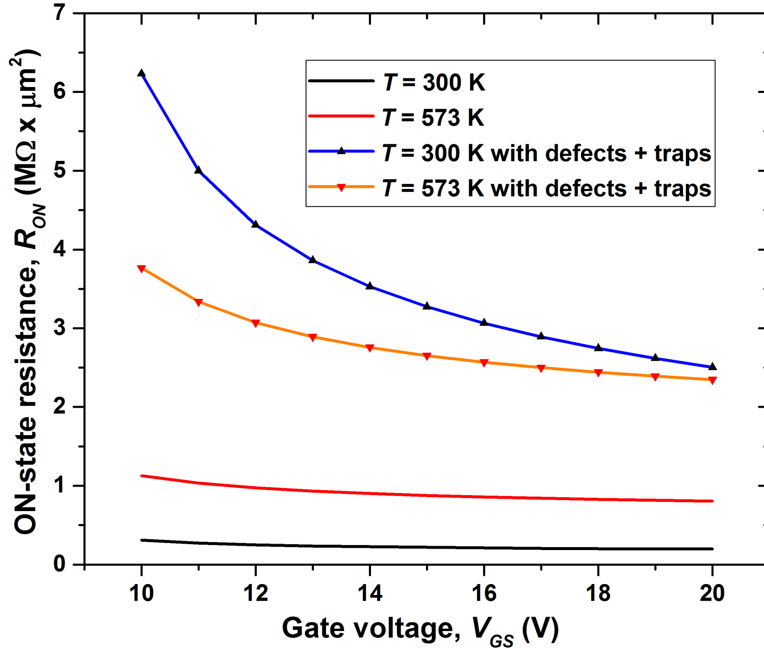

Fig. 4.62. The ON-state resistance vs gate voltage. The black-line and red-line refers to device free of defects and traps. The orange-line and blue-line are relative the simulated device with defects and traps.

mance of the power device. Indeed, the R_{ON} value increases for a fixed temperature, especially for low bias voltages. This increase tends to be smoother at higher bias voltage values. In apparent countertendency, the orange-line confirm the reduction of the R_{ON} at $T = 573\ K$, according to the fact that at high temperature the *Coulomb* scattering at the charged interface tends to decrease, consequently the mobility increase and will result in a lower value of the ON-state resistance. This behaviour leads to the question of whether the R_{ON} can continuously be reduced by increasing of temperature, until to the point of causing problems with thermal runaway. To answer this question we have to consider that the observed effect depends mainly on defects density and of temperature. Of course, at the room temperature, the device presents a positive thermal coefficient, thus for high defects density the device has a very high ON-state resistance, this leads it to operate with very low currents such as to render the device unusable. Instead, only at very high temperature ($T \geq 300\ ^{\circ}C$) the device shows a R_{ON} with a negative thermal coefficient.

5

CONCLUSIONS AND AN OUTLOOK ON THE FUTURE DEVELOPMENTS

> If you want something new, you have to stop doing something old.
>
> Peter Drucker

5.1 Conclusion

In this thesis, the development of a power MOSFET for photovoltaic applications has been addressed. The project focused on Silicon Carbide, which, as we have seen, is a material that allows superior performance than Silicon. In recent years, the sore point of SiC was represented by its relatively low mobility of carriers compared to Silicon. Moreover, the high costs did not favour their rapid diffusion and development. Nowadays the situation has changed, in fact, thanks to the continuous technological improvement, the production of SiC wafers has reached an excellent quality, indeed, SiC-based devices present good carriers' mobility, almost similar to those of Silicon, and also costs lower than that of a decade ago. The designed device has a vertical structure and represents a "novel" MOSFET inside the scenario of the commercial products. This developed device has been defined novel because it is of class-150-V. In the market of electronic devices, the SiC MOSFETs are developed in a range of voltages between 600 V to 2 kV. Our decision to design this SiC power MOSFET for lower voltage is mainly linked to a factor of reliability and robustness that guarantees a life cycle superior to that of Silicon. In the first part of this research work, a vertical 4H-SiC MOSFET has been designed, simulated and optimized. The requirements for power optimizers used in PV modules, generally rated for a maximum voltage of 100 V, include high efficiency, for a fast return of investments, and 20 years or longer life span, under any weather conditions. Both these requirements could be addressed in principle by deploying the fast and rugged SiC-based switches, if only they were avail-

able for this voltage range. The performances for this 150-V-class switching converters have been predicted by numerical simulations. The device features an ON-state resistance in the order of 0.9 $m\Omega \times cm^2$, with a small $FOM = R_{ON} \times Q_g$ of 0.48×10^{-9} $\Omega \times C$ which are comparable to that of commercial Silicon MOSFETs rated for the same voltage range. In the second part of the thesis, the study of defects and traps affecting the SiC MOSFET was addressed. From the literature, it has been understood that the region of the device which is most afflicted by these problems is the interface zone between the channel and the gate oxide. The presence of defects/traps tends to weigh negatively on the electrical characteristics of the device and on its performance. Thus, the impact of interface traps on the electrical characteristics of the device was assessed. Unfortunately, neither in the literature nor the chipmakers issue detailed information on the density of distribution of defects and traps, in particular, it is not easy to find in literature all the numerical values necessary to develop other numerical simulations. Normally, they reported only incomplete parameters table.

This led us to test the contribution of each physical model parameter related to the structure considered. Thus, in order to be able to use the parameters well-known in the literature and to be able to operate with a similar structure (at least for voltage class), it was decided to modify the designed structure and make it suitable for 650 V class. For this simulated device, the impact on the electrical characteristics, first of traps, second of defects alone was assessed and subsequently, they were combined to evaluate their conjoint impact. These results are useful not only to understand how it is possible to improve the ON-state resistance of the device, but they can also be used for future developments of a device for a different voltage-class.

In conclusion, in this thesis has been presented a novel power MOSFET in 4H-SiC useful for DC-DC converters of PV applications. It has been shown that defects and traps at the interface with gate-oxide play a key role in the reduction of ON-state resistance and thus on its performance, robustness and reliability. The deep comprehension of the connection between channel resistance, interface defects and electrical characteristics are a crucial point during the design and technological development of a new device.

5.2 A look at the future of power electronics

Silicon Carbide MOSFETs offer superior dynamic and thermal performance over conventional Silicon power MOSFETs. At the next generation SiC MOSFET will be required to respect the following technological constraints:

Features:

- Low capacitances and low gate charge
- Fast switching speed due to low internal gate resistance (ESR)[1]
- Stable operation at the high junction temperature
- Fast and reliable body diode
- Superior avalanche ruggedness

Benefits:

- High efficiency with lower switching losses
- Simple to drive and easy to parallel
- Improved thermal capabilities to the highest junction temperature
- Eliminates the need for an external freewheeling diode
- Lower system cost (smaller magnetics/heatsinks)
- Ruggedness for harsh environments

Applications:

- PV inverter, converter, and industrial motor drives
- Smart grid transmission and distribution
- Induction heating and welding
- Hybrid/electric vehicle (HEV)/(EV) power-train and charging
- Power supply and distribution

Considering the major data presented by the analysts of technology development, in the next years, we will have available better technological processes for improving the electronic device production and to reduce production costs while increasing the return on investment (ROI). Also, the projection of data related to the expansion of consumers markets and applications seems very promising, ergo there will be a new era of devices for power electronics and high frequency. Raw semiconductor it is the key around which all turns, thus we can trust to the commercial analysts' data, because Silicon, although it is still the undisputed leader among the semiconductors for

[1] Equivalent Series Resistance

electronics, it has now almost reached its theoretical limit of development. This means that in the future will be necessary to use new materials, with better characteristics; we remember that in these last years new materials have made powerfully and successfully peep into the market, becoming Silicon antagonists.

Power MOSFETs are a vast category of devices, in this research work we have focused our interest around the vertical DMOSFET for low voltage applications ($< 900\ V$). This topology needs to be further improved under any point of view, of course, each topology can be improved for its particular application area. The designed device in this thesis ($\sim 150\ V$) could be further developed to improve the mobility of carriers, its power losses and its behaviour in temperature.

In some advanced research centres, scientists are studying composite junctions with SiC, GaN and graphene. So it will not be difficult to see in the next years new research on power devices composed by the integration of these innovative materials in order to expand and improve their features and performances.

5.3 Today's MOSFET quality

During the past two years, commercially available class-1200-V SiC MOSFETs have great strides in terms of quality, indeed result:

- Channel mobility has risen to suitable levels.
- Gate oxide lifetimes have reached an acceptable level for most of the industrial projects.
- Threshold voltages have become increasingly stable.

Thus, we can be sure of today's SiC MOSFET quality, including long-term reliability, parametric stability, and device ruggedness.

From information provided by Yole Devéloppement, we learned that researchers at NIST (National Institute of Standards and Technology) have used TDDB (Time-Dependent Dielectric Breakdown) techniques to determine the oxide lifetime of a Monolith Semiconductor's MOS technology. With a temperature junction higher than $200\ ^{\circ}C$, they have estimated a lifetime of about 100 years. The NIST experiment used a lifetime acceleration factor of the applied electric field across the oxide ($E \geq 9\ MV/cm$) and junction temperature (up to $300\ ^{\circ}C$). These value can be considered satisfactory if we consider that the oxide electric field used in practice is around $4\ MV/cm$ (corresponding to $V_{GS} = 20\ V$), and junction temperatures during operation are typically lower than $175\ ^{\circ}C$.

5.4 Other future develop for this project

They should be the following:

- Study on the material properties to the specific operative range of temperatures, and on temperature dependence in the impact ionization model. In particular, for the 4H-SiC device used as a switch, an important factor for temperature dependence should be the physical parameters of impact ionization.
- Study and evaluation through numerical simulation of thermal conductivity of SiC.
- Evaluation under stress-mode of robustness and quality of SiC device, and comparison with the same Silicon class-device; this study, for a greater "guarantee" of results, should be performed both through numerical simulation and with experimental devices.
- AC operation simulation.
- Study of the use of high-doped ultra-thin layers, for improving electrical characteristics without having a significative breakdown voltage variation. On this point has been dedicated to the next paragraphs.

Anyway, the future of power electronics is declined through the following points:

1. Optimization of technological production processes.
2. SiC-wafer of better quality and at reduced costs.
3. Design of improved electronic devices.

Each of the above points has much to contribute to the development of future power electronics. From scientific literature available nowadays, it is clear that the design of novel geometric structures and the deep study of physical processes can be translated into a sure improvement of current devices. My idea of new development about SiC MOSFETs concerns the optimization of electrical characteristics, and thus the reduction of R_{ON}. There are several ways to try to tackle this problem, one of them is to use a very thin semiconductor layer with high doping and apply it upon the interface junction between the channel region and the gate oxide. Thanks to the highly doped layers, the current that flow in the channel region will increase proportionally to the relative junctions doping, with the final effect to reduce the channel resistance (R_{ch}) contribution, the relative weight of which is around 40% of the total R_{ON} value. Of course, as already seen in section 3.4, the doped layer thickness has a direct influence on breakdown voltage.

Challenges in development of SiC MOSFETs are summarised in list below, in which are reported the possible improvement to obtain a low R_{ON}, a better feasibility and reliability.

- Improve channel mobility
- Improve interface quality
- Increase current handling capability
- Reduce contact resistance
- Reduce resistivity of implanted layers
- Reduce substrate resistivity
- New gate dielectrics
- Channel engineering
- Crystallographic orientation
- Polytype (e.g. 15R, etc)
- Channel shape
- Substrate thinning

5.5 Encouraging results

My effort to improve the designed MOSFET performance has been focused around optimization of electrical characteristics and thus of the R_{ON}. We have seen that channel resistance has a high relative weight on the device R_{ON}. Therefore, for reducing this last contribute it is necessary to improve the electrons conductivity and mobility. I have tried to resolve this point through the use of very think layer highly doped, places at the interface between the MOSFET channel and the gate oxide. From a technological point of view, this extra-layer represents an extra low-deposition-energy process with a high dopant atoms concentration. Thus, has been considered the same designed structure of Fig. 4.2 free of defect and traps, which parameters was reported in Table 4.6. For this modified structure has been added one very thin layers (100 Å) positioned upon the P-base region. This extra layer were doped with a P-base doping concentration of $N_{P-base} = 10^{19}\ cm^{-3}$, see Fig. 5.1, instead in Fig. 5.2 is shown a zoom of channel area, where it is evident the highly doped thin layer.

From these tests and according to what reported in scientific literature, has been possible to understand many crucial factors before to proceed further in this new research challenge. First of all, the minimum energy for a technological deposition process allows to produce a superficial deposition, but this depth of penetration depends also by the type of dopants. For Boron dopant diffused on SiC, it is preferable

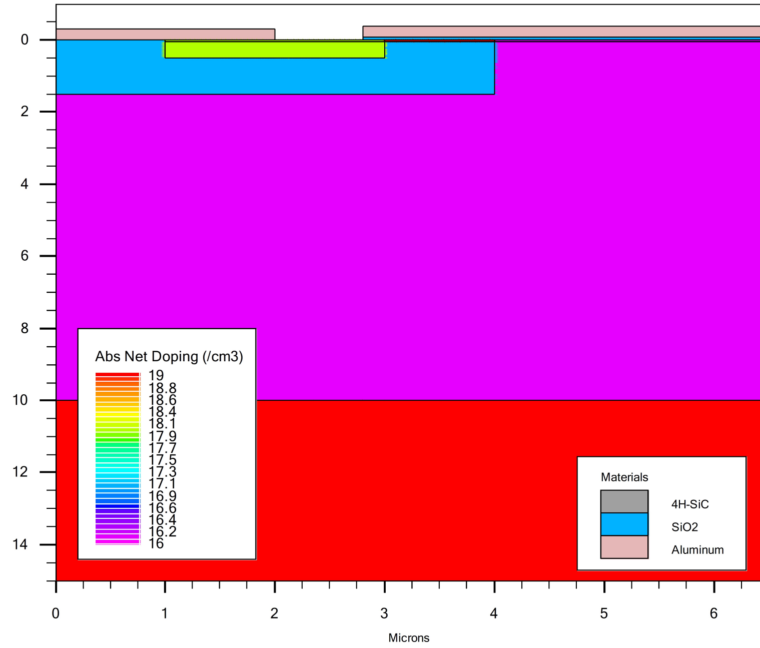

Fig. 5.1. Free-structure. Absolute net doping distribution for the structure with "top-layers".

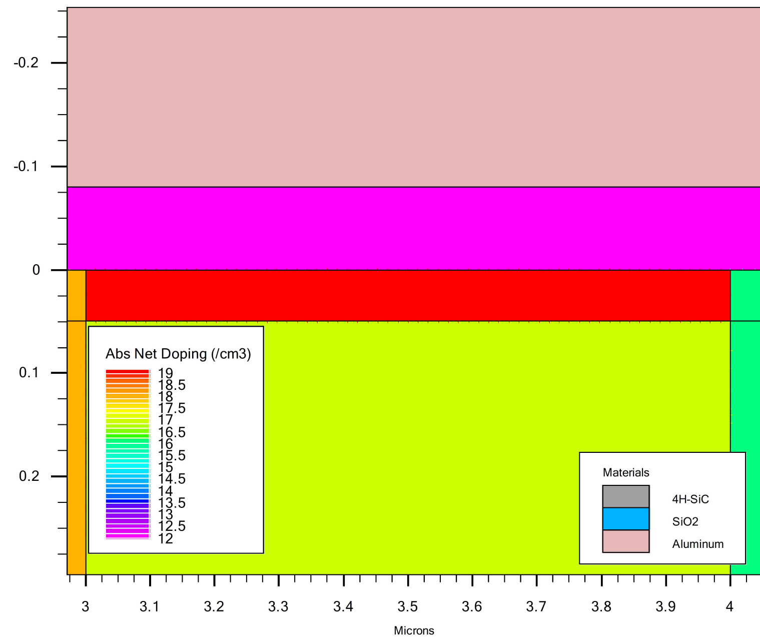

Fig. 5.2. Free-structure with "top-layers". Absolute net doping distribution in the channel region.

to consider an extra-layer deep at least 150 Å. At this depth, we are more sure to reap the benefits of the high superficial doping. Indeed, increasing the superficial doping and using a more appropriate doping profile, it is possible to improve further the electron mobility inside the channel region. In a better situation the yellow area as in Fig. 5.3, which corresponds to higher electron mobility, will tend to rise more towards the interface with the gate oxide. The net result will be an improvement in electrical characteristics. But, to quantify these margins of improvement, it will be necessary to continue to investigate in this direction. The value of the channel mobility in the case of the DMOSFET is the average mobility due to the Gaussian p-well doping distribution used in the simulations. It can be seen from simulations in Fig.5.4 that channel mobility depends by two-dimensional directions (x,y), so doping influences mobility also along the vertical direction of the channel.

Finally, in Fig. 5.5 is shown the comparison between the forward characteristics for the "classic" structure of Fig. 4.2 together with that of the modified structure Fig. 5.1. The curves marked with an asterisk are relative to the modified structure. It is clear that this modification can provide a considerable margin of improvement, but we need to invest further in this "solution" to understand how to proceed ahead with this research, and mainly without altering other device feature, such as the BV_{DS} and the established SiC robustness.

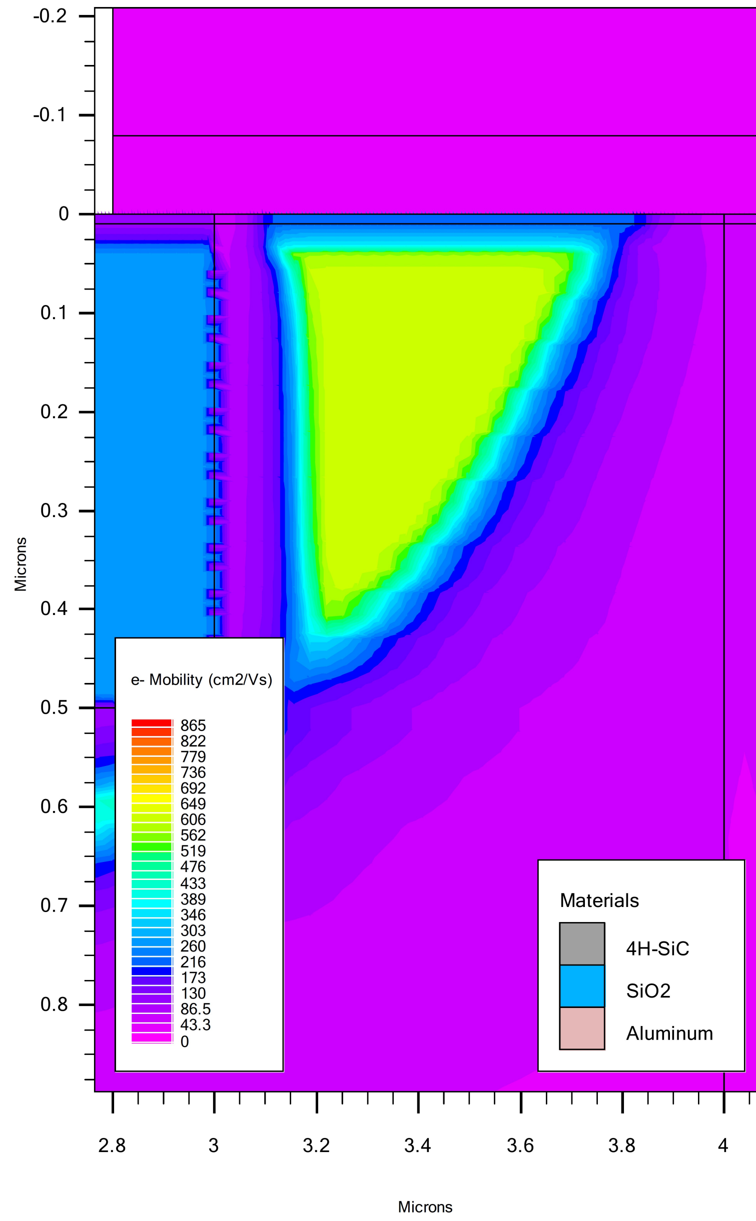

Fig. 5.3. Free-structure with "top-layers": electron mobility distribution inside the device. Zoom of area near the channel MOSFET.

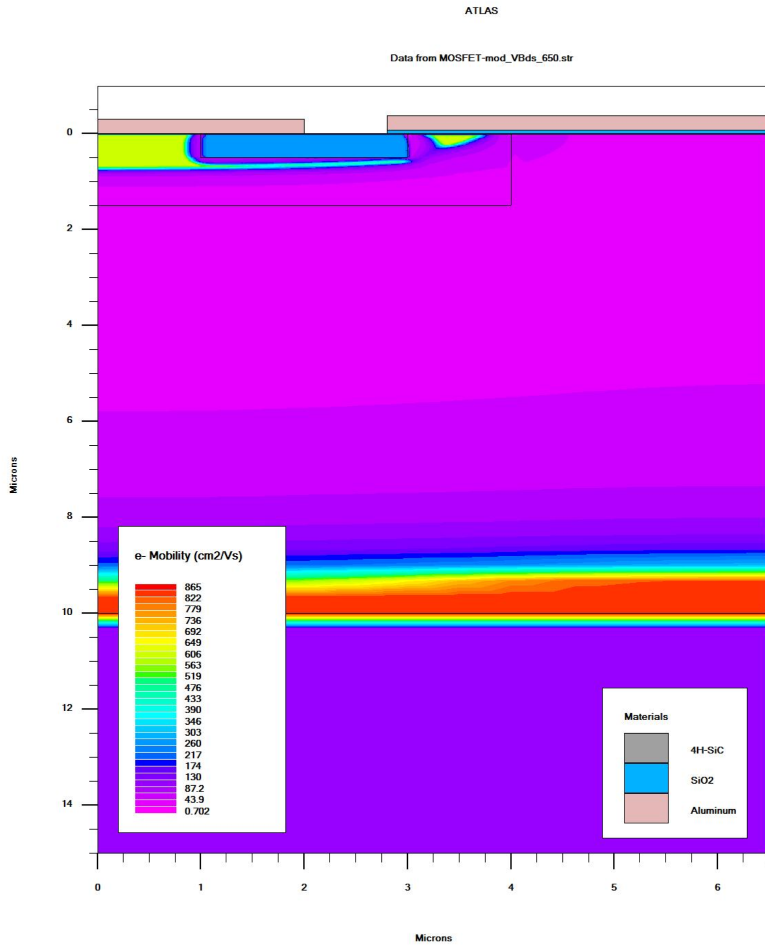

Fig. 5.4. Free-structure with "top-layers": electron mobility distribution inside the device.

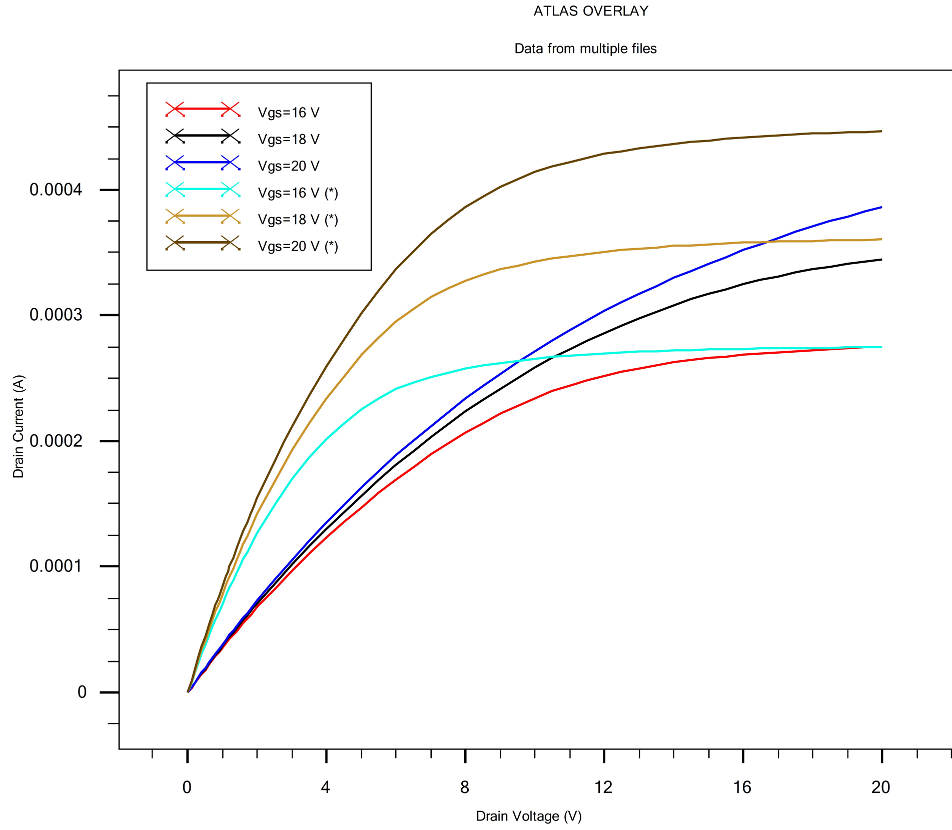

Fig. 5.5. Forward characteristics for a device with footprint of 6.5 μm^2. The curves plotted for Vgs values with the asterisk are relative to the modified MOSFET structure, which adopt a highly-doped thin top-layer.

A

Appendix A: List of symbols

β	Constant for saturation velocity
ε_r	Relative dielectric constant
ε_{SiC}	Dielectric constant of Silicon Carbide (F/cm)
φ_b	Barrier height metal to n-type semiconductor (V)
μ_{300}	Electron mobility at room temperature $T = 300\ K$ (cm^2/Vs)
μ_N, μ_P	Electron mobility (cm^2/Vs)
μ_{ch0}	Low-field mobility in inversion layer (cm^2/Vs)
μ_A	Accumulation layer mobility (cm^2/Vs)
μ_{JFET}	JFET region mobility (cm^2/Vs)
C_{GD}	Capacitance between gate and drain (F)
C_{DS}	Capacitance between drain and source (F)
C_{GS}	Capacitance between gate and source (F)
C_{OX}	Oxide capacitance per unit area (F/cm^2)
c_{ox}	Oxide capacitance (F)
E_{cr}	Critical breakdown electric field (kV/cm)
E_{max}	Maximum electric field (V/cm)
I_D	Drain current (A)
$I_{D,SAT}$	Saturation drain current (A)
K	*Boltzmann*'s constant (eV/K)
L_D	Thickness of drift region (cm)
L_{ch}	Length of channel (cm)
L_{DRIFT}	Length of drift region (cm)
L_{JFET}	Length of JFET region (cm)
η	Ideality factor
N_{DRIFT}, N_D	Doping concentration of drift region (cm^{-3})

N_{JFET}	Doping concentration of JFET region (cm^{-3})
q	Fundamental electronic charge (C)
R_{ACC}	Accumulation layer resistance (Ω)
R_{DRIFT}	Drift region resistance (Ω)
R_G	Gate resistance (Ω)
R_{JFET}	JFET region resistance (Ω)
$R_{ON,sp}$	Specific ON-state resistance ($\Omega \cdot cm^2$)
T	Absolute temperature (K)
ν_{sat}	Carrier saturation velocity in silicon carbide (cm/s)
V_{bi}	Built-in voltage in gate source junction (V)
V_B	Breakdown voltage (V)
V_{ch}	Channel voltage (V)
$V_{ch,SAT}$	Saturation voltage of the channel (V)
V_{DS}	Voltage applied to drain and source (V)
V_{GS}	Voltage applied to gate and source (V)
V_{GD}	Voltage applied to gate and drain (V)
V_{TH}	Threshold voltage (V)
ν_{th}	Thermal velocity (cm/s)
W'	Length of the depletion region under the gate oxide (cm)
W_{DRIFT}	Width of drift region (cm)
W_{DS}	Width of depletion region between drain and source (cm)
W_{GS}	Width of depletion region between gate and source (cm)
W_{JFET}	Depletion layer length. It begins to grow when $V_{DS} = V_{GS}$ (cm)
x	Temperature coefficient of carrier mobility
z	Length of device in vertical-to-paper dimension (cm)

B

Appendix B: ATLAS models

B.1 Incomplete dopant ionization in 4H-SiC

The ATLAS simulator takes into account the incomplete ionization of dopant impurities using *Fermi-Dirac* statistics, assuming a single donor or acceptor level. In this case, the ionized concentration of donors and acceptors, N_A^- and N_D^+, is expressed with the follows:

$$N_A^- = \frac{N_A}{1 + g_A \exp\left(\frac{E_A - E_{Fp}}{kT}\right)} \tag{B.1}$$

$$N_D^- = \frac{N_D}{1 + g_D \exp\left(-\frac{E_D - E_{Fn}}{kT}\right)} \tag{B.2}$$

where N_A and N_D are the concentrations of N-type and P-type dopant atoms; E_A and E_D are the energy levels of the acceptor atom and donor atom; E_{Fn} and E_{Fp} are the energy levels close to the *Fermi* level of holes and electrons; while g_A and g_D are adequate degeneration factors for the conduction and valence band.

Dopants atoms in SiC are incorporated inside the Silicon or Carbon atom matrix of the hexagonal crystal lattice. The stacking layer sequence of all polytypes, make that not all Silicon or Carbon sites are equivalent to their corresponding neighbours. Thus, each donor or acceptor can show multiple sites. Dopants on cubic sites typically have higher ionization energies than dopants on hexagonal sites.

Aluminium is the principal p-type dopant in 4H-SiC, and occupies either a hexagonal or a cubic Silicon site, having ionization energies of 197.9 meV and 201.3 meV respectively.

All materials with high ionization energy result not complete ionized at room temperature, among these we can consider aluminium. Incomplete ionization has a heavy effect on device performance

Nitrogen is the principal n-type dopants in 4H-SiC, and occupies a hexagonal Carbon site, having ionization energy of 61.4 meV. Phosphorus is the principal n-type dopants in 4H-SiC, and occupies a cubic Silicon site, having ionization energy of 60.7 meV [157]. Nitrogen and phosphorus donors have lower ionization energies and tend to be fully ionized at room temperature so in most cases $N_D^+ = N_D$.

Now, result important to calculate the effective density of states in the valence band (N_V) and in the conduction band (N_C), therefore we can begin from the density of ionized acceptors N_A^- (and donors N_D^+). The equilibrium hole and electron concentrations in extrinsic material ($N_A >> N_D$) or ($N_A << N_D$) at moderate temperatures ($n_i << N_{A,D}$) are given by $p = N_A^-$ (p-type material) or $n = N_D^+$ (n-type material). The ionized dopant concentrations N_A^- or N_D^+ in a neutral region can be calculated from the charge neutrality condition, and the equilibrium density of holes in p-type material can be written [158]:

$$p = N_A^- = \frac{\eta}{2}\left(\sqrt{1 + \frac{4N_A}{\eta}} - 1\right) \tag{B.3}$$

where η is given by:

$$\eta = \frac{N_V}{g_A}\exp\left(-\frac{E_A - E_V}{kT}\right) \tag{B.4}$$

here E_A is the energy level of the acceptor impurity, g_A is the degeneracy factor for acceptors (typically value is 4), and N_V is the effective density of states in the valence band, given by:

$$N_V = 2\left(\frac{2\pi m_{dh}^* kT}{h^2}\right)^{3/2} \tag{B.5}$$

Where m_{dh}^* is the density-of-states effective mass for holes and h is *Planck*'s constant. Similarly, the equilibrium density of electrons in n-type material is given by:

$$n = N_D^+ = \frac{\gamma}{2}\left(\sqrt{1 + \frac{4N_D}{\gamma}} - 1\right) \tag{B.6}$$

Where

$$\gamma = \frac{N_C}{g_D}\exp\left(-\frac{E_C - E_D}{kT}\right) \tag{B.7}$$

here E_D is the donor energy level, g_D is the degeneracy factor for donors (typically value is 2), and N_C is the effective density of states in the conduction band, given by:

$$N_C = 2\left(\frac{2\pi m_{de}^{*} kT}{h^2}\right)^{3/2} \tag{B.8}$$

where m_{de}^{*} is the effective density of states for the mass of electrons.

Figure B.1 [158] shows the ionization fraction for aluminium acceptors in neutral regions of 4H-SiC, computed using an ionization energy of 200 meV, the curve at room temperature is indicated by the dashed line. At a doping of 10^{17} cm^{-3}, only about 15% of the acceptors are ionized at room temperature, and the equilibrium hole concentration is only about $1.5 \cdot 10^{16}$ cm^{-3}. The ionization fraction increases with temperature, reaching about 75% at 300 $°C$.

Figure B.2 [158] shows the ionization fraction for nitrogen or phosphorus donors in 4H-SiC, computed using an ionization energy of 61 meV. At a doping of 10^{17} cm^{-3}, approximately 90% of the donor atoms are ionized at room temperature.

Figure B.3 [158] shows the *Fermi* potential ψ_F for aluminium-doped 4H-SiC calculated using:

$$\psi_F = \frac{kT}{q} \ln\left(\frac{N_A^-}{n_i}\right) \tag{B.9}$$

Figure B.4 [158] shows the intrinsic carrier concentration in 4H-SiC as a function of temperature. As temperature increases, the *Fermi* level ψ_F shift near the midgap, and the change is higher for lighter dopings. The reduction in ψ_F is caused by the rapid increase of n_i with temperature, as is shown in Fig. B.5 [158], for nitrogen or phosphorus-doped 4H-SiC. For a doping levels above 10^{19} cm^{-3} the mean space between dopant atoms is less than 5 nm, and electron wave functions from adjacent atoms overlap, increasing the energy of the impurity band that reduces the effective bandgap. This reduces the dopant ionization energies $E_{A,D}$, leading to more complete ionization than predicted by Eq. B.3 and B.6.

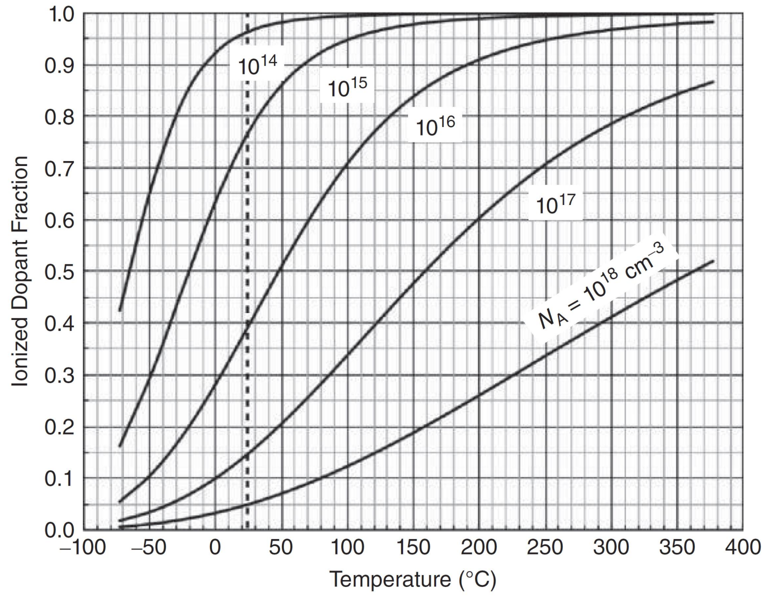

Fig. B.1. Ionization fraction for aluminium acceptors in 4H-SiC, computed using an ionization energy of 200 meV. Room temperature is indicated by the dashed line.

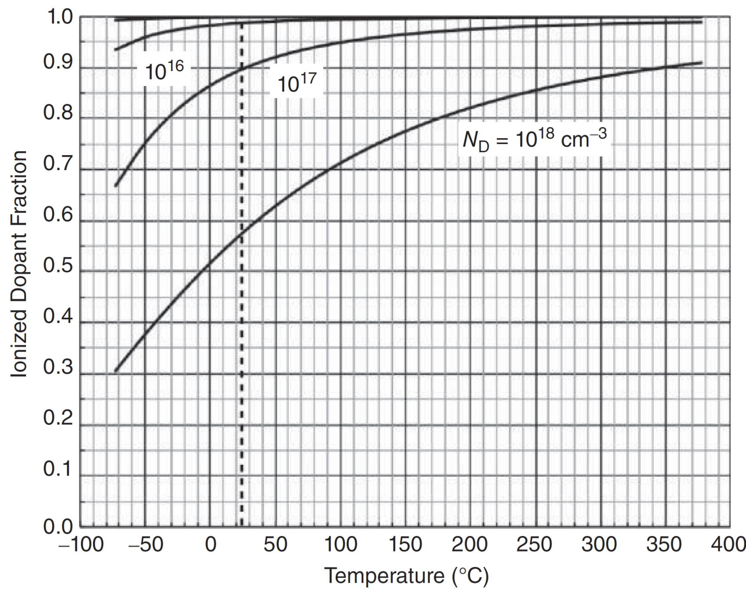

Fig. B.2. Ionization fraction for nitrogen or phosphorus donors in 4H-SiC, computed using an ionization energy of 61 meV. Room temperature is indicated by the dashed line.

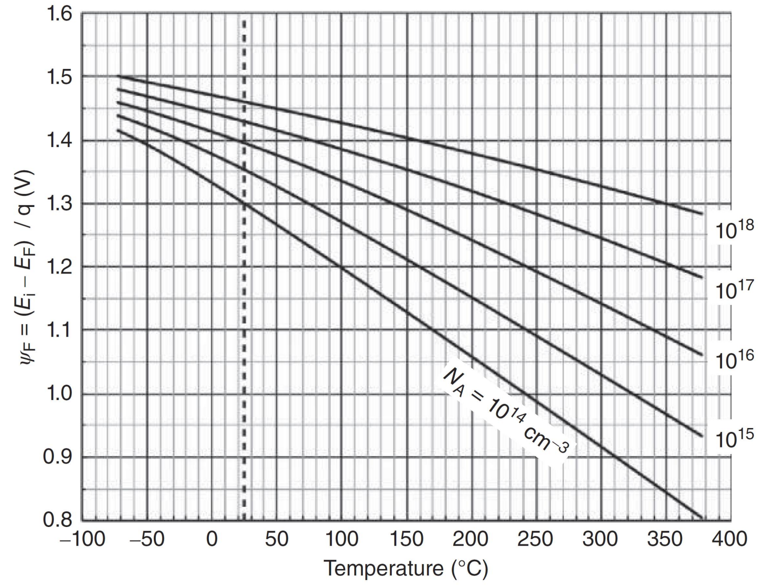

Fig. B.3. *Fermi* potential in aluminium-doped 4H-SiC as a function of doping and temperature.

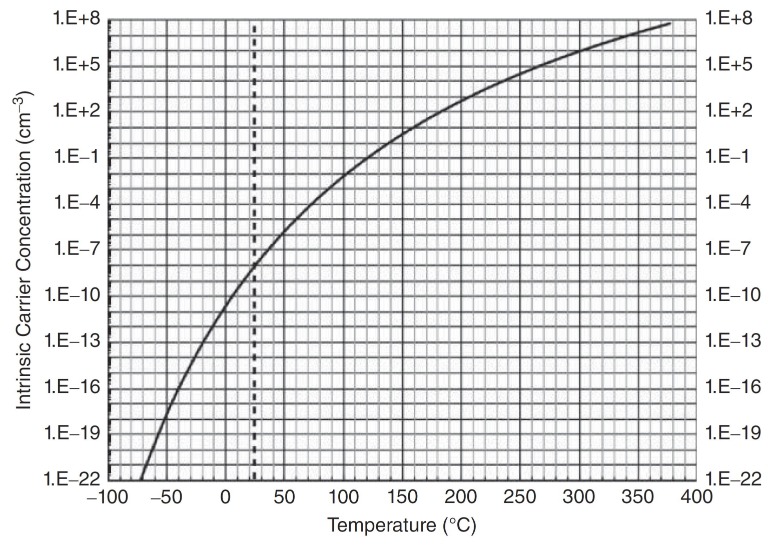

Fig. B.4. Intrinsic carrier concentration in 4H-SiC as a function of temperature. Room temperature is indicated by the dashed line.

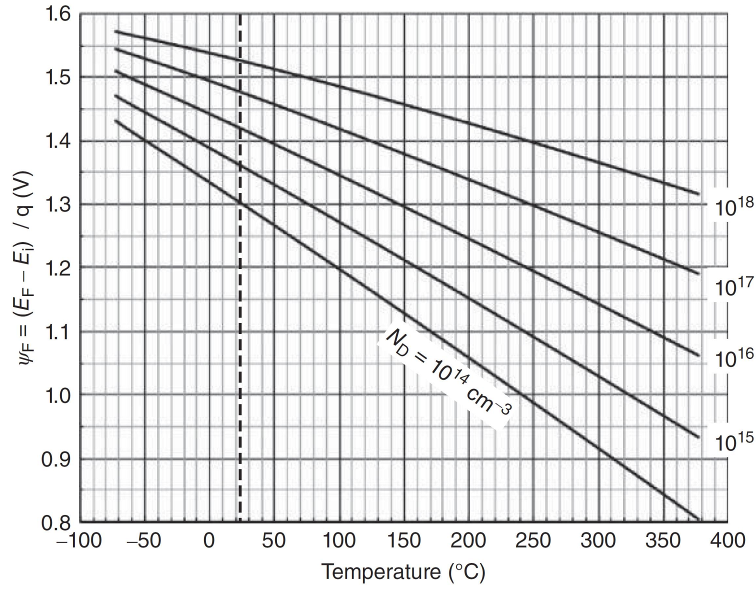

Fig. B.5. *Fermi* potential in nitrogen or phosphorus-doped 4H-SiC as a function of doping and temperature.

B.2 Impact ionization model in 4H-SiC

Impact ionization is a cascade process leading to a cascade of mobile carriers and very often the name avalanche multiplication is used instead of impact ionization. This multiplication process is characterized by an ionization rate or ionization coefficient α defined as the number of electron-hole pairs generated by a carrier per unit distance travelled. The multiplication factor, M, is the total number of electrons-holes pairs created in the depletion layer due to the single e-h pair initially generated at a location "x" in the depletion region. It can be shown [88] that the multiplication factor expressed in ionization rates and is given by:

$$M_n = \frac{1}{1 - \int_0^L \alpha_n \exp\left[-\int_0^x (\alpha_n - \alpha_p)\, dx'\right] \cdot dx} \tag{B.10}$$

$$M_p = \frac{1}{1 - \int_0^L \alpha_p \exp\left[-\int_0^x (\alpha_p - \alpha_n)\, dx'\right] \cdot dx} \tag{B.11}$$

The avalanche breakdown voltage is defined as the voltage where M_p approaches infinity. Hence the breakdown condition is given by the ionization integral:

$$\int_0^L \alpha_n \exp\left[\int_0^L - (\alpha_n - \alpha_p)\, dx'\right] \cdot dx = 1 \tag{B.12}$$

$$\int_0^L \alpha_p \exp\left[\int_0^L - (\alpha_p - \alpha_n)\, dx'\right] \cdot dx = 1 \tag{B.13}$$

However, various models have been proposed according to new experimental results, mainly on Silicon, as well as according to their implementation in device simulation (empirical models). The mostly used is that the often-called *Selberherr's model* [61]. It is especially used in TCAD simulator:

$$\alpha_n = a_n \exp\left(-\frac{b_n}{E}\right)^{c_n}, \alpha_p = a_p \exp\left(-\frac{b_p}{E}\right)^{c_p} \tag{B.14}$$

where E is the electric field. There are different models describing the relationship between ionization coefficients and the electric field. Most are local models. Indeed, ionization rates are assumed to be instant functions of the electric field E. This assumption is called the local model. Non-local models incorporate the carrier temperature magnitude as the main parameter of ionization. Up till now, there are no publications on non-local models for 4H-SiC simulations, only proposed models for

which one could choose. Most of the models proposed by TCAD simulators are inspired by Silicon data and therefore address suitably the impact ionization of this material. In the low-field region, the ionization rate is strongly temperature dependent because the ionizing carriers travel several mean free paths without an ionizing collision. Most TCAD simulators introduce the temperature dependence of ionization rates through the coefficients $a_{n,p}$, $b_{n,p}$ of the *Selberherr model*, according to the following formula [22]:

$$a_n = a_{n,300}\left(1 + A_{NT}\left[\left(\frac{T_t}{300}\right)^{ma_n} - 1\right]\right) \tag{B.15}$$

$$b_n = b_{n,300}\left(1 + B_{NT}\left[\left(\frac{T_t}{300}\right)^{mb_n} - 1\right]\right) \tag{B.16}$$

$$a_p = a_{p,300}\left(1 + A_{PT}\left[\left(\frac{T_t}{300}\right)^{ma_p} - 1\right]\right) \tag{B.17}$$

$$b_p = b_{p,300}\left(1 + B_{PT}\left[\left(\frac{T_t}{300}\right)^{mb_p} - 1\right]\right) \tag{B.18}$$

where $a_{n,300}$, $a_{p,300}$, $b_{n,300}$, $b_{p,300}$, are the corresponding values at $T = 300\ K$, describing the dependence on the electric field. For SiC, the ionization rate is a function of crystal orientation. Highly anisotropic band structure of the 4H-SiC, which is caused by a long period along c-axis of the crystal structure of 4H-SiC, brings about anisotropic high-field carrier transport and results in an anisotropy of the impact ionization coefficients. In this case, different impact ionization coefficients are used for transport at different crystal directions. To explain the observed impact of temperature in impact ionization rates measurements the model equations describe them had to be parameterized, such as to include the temperature impact.

This model in Silvaco ATLAS is represented as follows:

$$\alpha_n = AN_{1,2}\exp\left[-\left(\frac{BN_{1,2}}{E}\right)^{BETAN}\right] \tag{B.19}$$

$$\alpha_p = AP_{1,2}\exp\left[-\left(\frac{BP_{1,2}}{E}\right)^{BETAP}\right] \tag{B.20}$$

where E is the electric field in the direction of current flow at a particular position in the structure. The impact ionization model for continuity equations allows the accurate prediction of avalanche breakdown for power MOSFETs. To perform numerical simulation was considered the *Selberrherr Model*, with Baliga parameters value

for 4H-SiC MOSFET: $AP1$,$BP1$, $AN1$, and $BN1$ corresponds to field values greater than $EGRAN$, and $AP2$, $BP2$, $AN2$, and $BN2$ corresponds to field values less than $EGRAN$. $BETAN$ for electrons and $BETAP$ for holes correspond to coefficients for the power of E_{CRIT} / E.

The temperature variation for these parameters can be written as follows [72]:

$$AN = AN_{1,2}\left(1 + A.NT\left[\left(\frac{T_L}{300}\right)^{M.ANT} - 1\right]\right) \tag{B.21}$$

$$AP = AP_{1,2}\left(1 + A.PT\left[\left(\frac{T_L}{300}\right)^{M.ANP} - 1\right]\right) \tag{B.22}$$

$$BN = BN_{1,2}\left(1 + B.NT\left[\left(\frac{T_L}{300}\right)^{M.BNT} - 1\right]\right) \tag{B.23}$$

$$BP = BP_{1,2}\left(1 + B.PT\left[\left(\frac{T_L}{300}\right)^{M.BPT} - 1\right]\right) \tag{B.24}$$

The model parameters are:

$AN1 = 2.50 \times 10^5\ cm^{-1}$
$AN2 = 2.50 \times 10^5\ cm^{-1}$
$BN1 = 1.84 \times 10^7\ V/cm$
$BN2 = 1.84 \times 10^7\ V/cm$
$BETAN = 1$
$AP1 = 3.25 \times 10^6\ cm^{-1}$
$AP2 = 3.25 \times 10^6\ cm^{-1}$
$BP1 = 1.71 \times 10^7\ V/cm$
$BP2 = 1.71 \times 10^7\ V/cm$
$BETAP = 1$
$EGRAN = 6 \times 10^6\ V/cm$

B.3 Shockley-Read-Hall

The standard *Shockley-Read-Hall* model is chosen and the temperature dependency model is activated by assigning to one of its parameter a non zero value. The temperature dependence of electron and hole lifetimes in the *SRH* recombination model have the forms:

$$\tau_{SRH} = R_{SRH} = -G_{SRH} = \frac{\left(np - n_{ie}^2\right)}{\left[t_p\left(n + n_0\right) + t_n\left(p + p_0\right)\right]} \tag{B.25}$$

$$\tau_{n,p}^{\max}\left(T_L\right) = \tau_{n,p}\left(300\right)\left(\frac{T_L}{300K}\right)^{a_{n,p}^{SRH}} \tag{B.26}$$

As ATLAS model:

$$\tau_n = TAUN0\left(\frac{T_L}{300}\right)^{LT.TAUN}, \tau_p = TAUP0\left(\frac{T_L}{300}\right)^{LT.TAUP} \tag{B.27}$$

Thus, the SRH model is:

$$R_{SRH} = \frac{np - n_{ie}^2}{TAUN0\left[n + n_{ie}\exp\left(\frac{ETRAP}{k_B T_L}\right)\right] + TAUP0\left[p + n_{ie}\exp\left(-\frac{ETRAP}{k_B T_L}\right)\right]} \tag{B.28}$$

where $ETRAP$ is the difference between the trap energy level and the intrinsic *Fermi* level. while, $TAUN0$ and $TAUP0$ are the electron and hole lifetimes.

B.4 Auger lifetime

In ATLAS the $AUGER$ lifetime model is implemented with following:

$$\tau_{AUG}^{low} = \left(C_{n,p}N_{D,A}^2\right)^{-1} \tag{B.29}$$

The parameter values for 4H-SiC used are the default values reported in [72]: $AUGN = 5\times\ 10^{-31}$ and $AUGP = 2\times\ 10^{-31}$

B.5 Energy bandgap narrowing

This important parameter has been faced in section 2.4, here is shown the ATLAS model implemented in simulator. These effects may be described by an analytic expression relating the variation in bandgap, ΔE_g, to the doping concentration, N. The expression used in ATLAS is from the model of Slotboom and de Graaf [86, 159]:

$$\Delta E_g = BGN.E \left\{ \ln \frac{N}{BGN.N} + \sqrt{\left[\left(\ln \frac{N}{BGN.N} \right)^2 + BGN.C \right]} \right\} \tag{B.30}$$

C

Appendix C: Figures of Merit

Figures of Merit (*FOMs*) characterize power device from different aspects, such as conduction loss, switching loss, and thermal and semiconductor materials. As switching frequencies increase, it becomes of paramount importance to reduce the switching losses in the converter. These are the losses associated with the transition of the switch from its ON-state to OFF-state, and back. The higher the switching frequency, the greater the number of times the switch changes state per second. Therefore, these losses are proportional to the switching frequency. Further, of these frequency-dependent loss terms, the most significant are usually those that take place within the switch itself.

From Table C.1 [160] one can see, that 4H-SiC is much better than silicon or GaAs in all aspects. Compared to GaN, 4H-SiC switches about 3.5 times faster and has minimalistic loses. Therefore, one can conclude that 4H-SiC material with a combination of the JFET design, manifests the best choice for switching applications. Another important feature for high-voltage power devices to be considered is the thermal property of the semiconductors, Shenay et al. [161] proposed the model indicate inside Table C.1 with (e) and (f), where $\sigma_A = \varepsilon \mu E_{cr}^3$.

Table C.1. FOM's for Silicon and SiC.

Details and Materials	**a) JFOM**	**b) KFOM**	**c) BFOM**	**d) BHFOM**	**e) QF1**	**f) QF2**
Equation	$E_B^2 \nu_S / 4\pi^2$	$\lambda C_B^2 \nu_S / 4\pi^2$	$R_{ON} \times Q_g$	μE_{cr}^2	$\lambda \sigma_A$	$\lambda \sigma_A E_{cr}$
Year	1965	1972	1982	1989	1989	1989
FOM Considers:	H.F.,power capability	Switching speed	L.F. R_{ON}	H.F., switching losses	Thermal	properties
Si	1	1	1	1	1	1
4H–SiC	278	5.1	178	29	594	4357

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