Multiobjective optimization of design of 4H-SiC power MOSFETs for specific applications

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Abstract- The electrical characteristics of a 4H silicon carbide (4H-SiC) MOSFET are investigated by means of a multi-objective genetic algorithm (MOGA) in order to overcome the existing tradeoff between the main device figures of merit such as the breakdown voltage, drain current, and ON-state resistance. The aim of the work is to achieve an optimized device for a specific application. In particular, without loss of generality, we refer to a dual-implanted MOSFET (DMOSFET) dimensioned for use as low-power transistor in DC-DC converters for solar power optimizers. Typical blocking voltages of these transistors are, in fact, around 150 V. For our investigation, both analytical and numerical models are used as objective functions to determine via MOGA a set of optimized physical and geometrical device parameters that meet the application constraints minimizing the ON-state resistance (R_{ON}). The optimized DMOSFET performs a R_{ON} value of a few hundred kΩ×μm^2 for different breakdown voltages in the range 150-800 V.

Keywords- 4H-SiC MOSFET, power device, design optimization, on-state resistance, blocking voltage.

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1. Introduction

During the last decade, the use of 4H silicon carbide (4H-SiC)-based MOSFETs for high-power, high-temperature, and switching applications was extensively proposed [1-5]. Silicon carbide, in fact, thanks to its outstanding physical and electronic properties (*i.e.*, mechanical strength, thermal conductivity, and critical electric field) [6,7], was worldwide recognized as a promising material able to improve the device performance in terms of ON-state resistance, breakdown voltage, and switching capabilities. In particular, SiC MOSFETs were widely

used as power devices in DC-DC converters to be put on-board of specific modules. For example, in [8] a boost-based converter was proposed describing the design of a zero-voltage zero-current switch (ZVZCS) suitable for high duty cycle and wide load currents; in [9] dual-SiC MOSFET modules were designed for electric traction contexts; in [10] a dual active bridge (DAB) converter was implemented using 10 kV SiC MOSFETs; in [11] a high-frequency, 1 kW, 800 V output voltage boost DC-DC converter was developed.

In order to meet the specific constraints related to modern power electronics, the design of 4H-SiC MOSFETs requires the deployment of intensive modelling efforts based in turn on numerical, analytical, and empirical calculations, which carefully take into account the different geometrical and physical parameters that affect the device performance [12-15].

Despite the fact that several studies deal with the tradeoff between the electrical characteristics of a MOSFET in 4H-SiC [15-18], to the best of our knowledge, no investigations have been made about a global performance optimization based on evolutionary algorithms. These tools, in fact, are very useful for optimization problems where various objective functions must be treated simultaneously providing low complexity and reasonable computational times.

With this intent, in this paper, we investigate the optimized design of a 4H-SiC dual-implanted MOSFET (DMOSFET) well suited for a specific application by means of a multi-objective genetic algorithm (MOGA) [19]. More in detail, starting from a combined analytical and numerical analysis of the device current-voltage (I_D-V_{DS}) characteristics, both analytical and numerical models are used as objective functions to optimize via MOGA the fundamental design parameters which minimize the ON-state resistance of a device dimensioned for a blocking voltage (BV_{DS}) in the range 150-800 V. Although typical 4H-SiC MOSFETs are designed to support high breakdown voltages ranging from 600 to 1700 V [20-22], recent papers have also investigated low power transistors (100-200 V-class) to be used, for example, for photovoltaic module-level applications where they could be able to operate in harsh conditions ensuring a considerable lifetime [23-28]. In fact, smart maximum power point tracking converters for photovoltaics should be characterized by BV_{DS} close to 150 V or less and R_{ON} in the limit of a few hundred $k\Omega \times \mu m^2$. In particular, in [23] the authors have underlined the requirement to overcome the existing tradeoff between BV_{DS}, I_D, and R_{ON} in determining the optimized performance of low-voltage MOSFETs in 4H-SiC. As mentioned above, without loss of generality, we adopt a framework of genetic algorithm to search for the commonly called Pareto optimal solution (*i.e.*, non-dominated solution) of several physical and geometrical device parameters. The obtained results in terms of R_{ON} are compared with those reported in [23].

2. DMOSFET structure

The schematic cross-sectional view of the n-channel 4H-SiC DMOSFET single-cell considered in this work is shown in Fig. 1. Here, the adopted notation concerning the geometry of the different device regions is also reported. In particular, W_{cell} is the cell width, L_{ch} is the device channel length, X_{JFET} is the distance between the base regions, W_{drift} is the thickness of the n-drift region, and X_{JP} and X_{N+} are the p-base and n+-source depths, respectively.

The source contact shorts the source and the base regions to prevent the switch-on of the parasitic substrate(n^+)-epilayer(n)-base(p)–source(n^+) bipolar junction transistor. Finally, a silicon oxide layer is used to insulate the actual MOS structure.

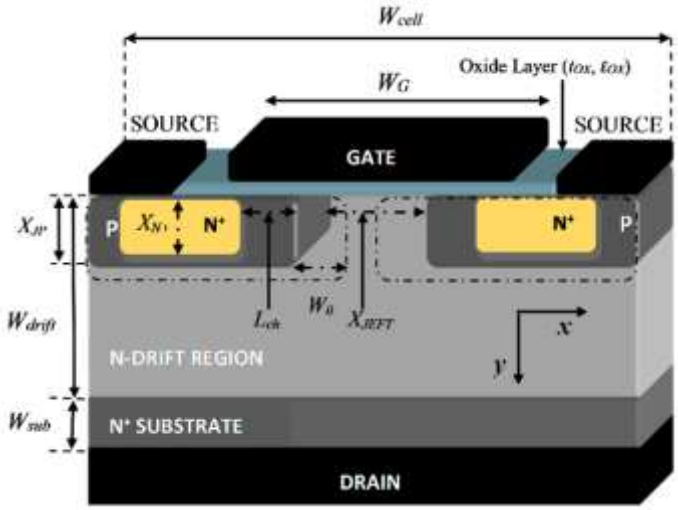


Fig. 1. Cross-sectional view of the n-channel 4H-SiC DMOSFET single-cell. The drawing is not in scale.

3. Computation methodology

Detailed analytical and numerical models are firstly used to investigate the DMOSFET current-voltage behaviors. Then, these models are assumed as objective functions to determine via MOGA the optimized physical and geometrical device parameters for a specific application. The fundamental simulation models are briefly recalled in the following subsections.

3.1. Analytical models

3.1.1. Breakdown voltage

The breakdown or blocking voltage (BV_{DS}) characteristics of a DMOSFET can be calculated when the device is in a firm off-state, *i.e.* $V_G = 0$ V and grounded source. The BV_{DS} value, in fact, is related to the onset of a breakdown within the base-drain p-i-n structure for an increasing bias voltage V_{DS}. By assuming the drift-region in a punch-through condition, namely totally depleted before the breakdown occurs, a first level prediction of BV_{DS}

is given by [7]

$$BV_{DS} = E_{pn}^{crit} W_{drift} - \frac{qN_{drift} W_{drift}^2}{2\varepsilon_{sc}} \tag{1}$$

where E_{pn}^{crit} is the critical electric field that appears somewhere along the border of the p-base/n-drift junction, ε_{sc} is the material permittivity, and N_{drift} is the doping concentration in the drift region. This expression is validated for $W_{drift} \le \varepsilon_{sc} E_{pn}^{crit} q^{-1} N_{drift}^{-1}$. For example, by considering typical values of the 4H-SiC permittivity and a critical electric field of 2 MV/cm, the width of the n-type drift region has to be in the limit of 10 μm for N_{drift} = 1×10^{16} cm^{-3} [7]. This result was also calculated in [29,30] for similar p-i-n structures. The electric field dependence on N_{drift} is in the form of [31]

$$E_{pn} = 2.49\times10^{6}\left(5 - 0.25\log N_{drift}\right). \tag{2}$$

3.1.2. ON-state resistance

The total ON-state resistance in the device current path is the sum of different terms as follows

$$R_{ON} = R_{N+} + R_{ch} + R_{acc} + R_{JFET} + R_{drift} + R_{sub} \tag{3}$$

where R_{N+} is the source resistance, R_{ch} is the channel region resistance, R_{acc} is the accumulation region resistance relative to the distance X_{JFET} next to the channel (see Fig. 1), R_{JFET} refers to the JFET channel portion, R_{drift} is the resistance of the drift region, and R_{sub} is the substrate contribution. In accordance with Fig. 1, the appropriate expressions of these terms can be written as [7]

$$R_{ch} = \frac{L_{ch} W_{cell}}{2\mu_{ch} C_{OX}\left(V_{GS} - V_{TH}\right)}, \tag{4}$$

$$R_{acc} = \frac{X_{JFET} W_{cell}}{4\mu_{acc} C_{OX}\left(V_{GS} - V_{TH}\right)}, \tag{5}$$

$$R_{JFET} = \frac{\rho_{JFET} X_{JP} W_{cell}}{W_G - 2X_{JP} - 2W_0}, \tag{6}$$

$$R_{drift} = \frac{\rho_{drift} W_{drift} W_{cell}}{W_{cell} - W_G + 2X_{JP} + 2W_0} \ln\left(\frac{W_{cell}}{W_G - 2X_{JP} - 2W_0}\right). \tag{7}$$

Here, in particular, C_{OX} is the gate oxide capacitance, μ_{ch} and μ_{acc} are respectively the doping-dependent carrier

mobilities in the inversion and the accumulation layer, ρ_{JFET} is the resistivity of the JFET region, and W_0 is the zero-bias depletion width in the JFET region computed by using

$$W_0 = \sqrt{\frac{2\varepsilon_{SC} N_A V_{bi}}{qN_{JFET}(N_A + N_{JFET})}} \tag{8}$$

where N_A and N_{JFET} are respectively the doping concentrations in the p-base and the JFET region, and V_{bi} is the built-in potential in the form of

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_{JFET}}{n_i^2}\right). \tag{10}$$

Note that, for the sake of simplicity, the resistance contributions R_{N+} and R_{sub} are considered negligible in our calculations because they are relative to heavily doped regions.

3.1.3. Threshold voltage and drain current

The MOSFET threshold voltage (V_{TH}) is defined as the gate bias voltage that assures the strong inversion regime in the channel region. Its value depends on the doping concentration in the p-base and increases linearly with the gate oxide thickness. A typical expression of V_{TH} is given by [7]

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4\varepsilon_{SC} kTN_A \ln\left(\frac{N_A}{n_i}\right)} + \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right). \tag{11}$$

By neglecting the subthreshold current (*i.e.*, $I_D = 0$ for $V_{GS} < V_{TH}$) and assuming the MOSFET operating point in the triode region (*i.e.*, $V_{DS} \le V_{GS} - V_{TH}$), the drain current is calculated as [10]:

$$I_D = \mu_{ni} C_{OX} \frac{W_{cell}}{L_{ch}} \left[2\left(V_{GS} - V_{TH}\right)\left(V_{DS} - I_D R_{ON}\right) - \left(V_{DS} - I_D R_{ON}\right)^2\right] \tag{12}$$

where the term $V_{DS} - I_D R_{ON}$ is the drain internal voltage that differs from the terminal voltage by the ohmic contribution.

Finally, for $V_{DS} > V_{GS} - V_{TH}$ we use:

$$I_D = \mu_{ni} C_{OX} \frac{W_{cell}}{2L_{ch}} \left(V_{GS} - V_{TH}\right)^2 \left[1 + \lambda\left(V_{DS} - I_D R_{ON}\right)\right] \tag{13}$$

where λ is an appropriate channel modulation coefficient.

3.2. Numerical framework

The DMOSFET numerical simulations were performed by using a commercial TCAD-2D physical simulator that provides the solution of Poisson's equation and carrier continuity equations [32]. The physical models and reference parameters taken into account at $T = 300$ K are summarized in Table I.

Table I. Physical models and reference parameters.

$R_{SRH} = \dfrac{pn - n_i^2}{\tau_p\left(n + n_i \exp\left(\dfrac{E_{trap}}{kT}\right)\right) + \tau_n\left(p + n_i \exp\left(-\dfrac{E_{trap}}{kT}\right)\right)}$	$n_i = 6.7\times10^{-11}$ cm^{-3}
$R_{Auger} = (C_{Ap}p + C_{An}n)(np - n_i^2)$	$C_{An} = 5\times10^{-31}$ cm^6/s $C_{Ap} = 2\times10^{-31}$ cm^6/s
$\tau_{n,p} = \dfrac{\tau_{0n,p}}{1 + \left(\dfrac{N}{N_{n,p}^{SRH}}\right)}$	$\tau_{0n} = 500$ ns $\tau_{0p} = 100$ ns $N_{n,p}^{SRH} = 1\times10^{30}$ cm^{-3}
$N_{A,D}^{-,+} = N_{A,D}\left(\dfrac{-1 + \sqrt{1 + 4g_{v,c}\dfrac{N_{A,D}}{N_{V,C}(T)}e^{\frac{\Delta E_{A,D}}{kT}}}}{2g_{v,c}\dfrac{N_{A,D}}{N_{V,C}(T)}e^{\frac{\Delta E_{A,D}}{kT}}}\right)$	$N_V = 3.29\times10^{19}$ cm^{-3} $N_C = 1.66\times10^{19}$ cm^{-3} $g_v = 4$, $g_c = 2$ $\Delta E_A = 190$ meV $\Delta E_D = 70$ meV
$\alpha_{n,p} = a_{0n,p}\exp\left(-\dfrac{b_{0n,p}}{E}\right)$	$a_{0n} = 2.5\times10^5$ cm^{-1} $a_{0p} = 3.25\times10^6$ cm^{-1} $b_{0n} = 1.84\times10^7$ V/cm $b_{0p} = 1.71\times10^7$ V/cm
$\Delta E_{gp,n} = A_{p,n}\left(\dfrac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{2}} + B_{p,n}\left(\dfrac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{3}} + C_{p,n}\left(\dfrac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{4}}$	$A_p = 1.54\times10^{-3}$ $B_p = 1.3\times10^{-2}$ $C_p = 1.57\times10^{-2}$ $A_n = 1.17\times10^{-2}$ $B_n = 1.5\times10^{-2}$ $C_n = 1.9\times10^{-2}$
$\mu_{n,p} = \mu_{0n,p}^{\min} + \dfrac{\mu_{0n,p}^{\max} - \mu_{0n,p}^{\min}}{1 + \left(\dfrac{N}{N_{n,p}^{crit}}\right)^{\delta_{n,p}}}$, $\mu_{n,p}(E) = \dfrac{\mu_{n,p}}{\left[1 + \left(E\dfrac{\mu_{n,p}}{v_{sat}}\right)^{\kappa_{n,p}}\right]^{\frac{1}{\kappa_{n,p}}}}$	$\mu_{0n}^{\min} = 40$ cm^2/V·s $\mu_{0p}^{\min} = 15.9$ cm^2/V·s $\mu_{0n}^{\max} = 950$ cm^2/V·s $\mu_{0p}^{\max} = 125$ cm^2/V·s $N_n^{crit} = 2\times10^{17}$ cm^{-3} $N_p^{crit} = 1.76\times10^{19}$ cm^{-3} $\delta_n = 0.76$, $\delta_p = 0.34$ $k_n = 2$, $k_p = 1$ $v_{sat} = 2\times10^7$ cm/s

They include the Shockley-Read-Hall recombination (R_{SRH}) [33], the Auger recombination (R_{Auger}) [34], the incomplete ionization of impurities ($N_{A,D}^{-,+}$) [35-37], the apparent bandgap narrowing ($\Delta E_{gp,n}$) [38], the doping dependent carrier lifetime ($\tau_{n,p}$) [39,40], the impact ionization rate ($\alpha_{n,p}$) [41], and the low-field and high-field carrier mobility ($\mu_{n,p}$) [42-44].

The simulation setup assumed in this work has been used in other recent works of ours [45-48] where it is also supported by comparison with experimental results obtained on both p^+-i-n and Schottky structures in a wide range of currents and temperatures [49-52].

4. Simulation analysis

In this section, we develop the background for the MOGA optimization. In particular, the impact of the fundamental design parameters on the DMOSFET main figures of merit is investigated by using the reference values listed in table II as initial entry data for modelling.

Table II. DMOSFET reference parameters (see Fig. 1).

Silicon oxide thickness, t_{ox} (μm)	0.08
Source thickness, X_{N+} (μm)	0.5
Channel length, L_{ch} (μm)	1
Base junction depth, X_{JP} (μm)	1.5
Base-to-base distance, X_{JFET} (μm)	7
Epilayer thickness, W_{drift} (μm)	10
Substrate thickness, W_{sub} (μm)	100
Gate width, W_G (μm)	9.4
Cell width, W_{cell} (μm)	15
Device footprint area (μm^2)	15
N^+-source doping, N_D (cm^{-3})	1×10^{18}
P-base doping, N_A (cm^{-3})	1.5×10^{17}
N-drift doping, N_{drift} (cm^{-3})	1×10^{16}
N^+-substrate doping, N_{sub} (cm^{-3})	1×10^{19}

4.1. Blocking voltage characteristics

The device BV_{DS} value is strictly dependent on the n-drift thickness which determines the distance between the base junction and the substrate, namely the difference W_{drift} - X_{JP} in Fig. 1.

In the numerical analysis, BV_{DS} was calculated by considering the device in the off-state and raising gradually V_{DS} up to the occurrence of an electric field threshold of 1.9 MV/cm. The increase of V_{DS}, in fact, is responsible for the expansion of the depletion region to the low-doped side of the p-base/n-drift junction and the more the depletion region expands, the more the electric field increases. The drain leakage current density, J_D, was kept below 10 mA/cm^2.

For the device in Table II, we calculated a BV_{DS} of about 900 V. Then, W_{drift} was reduced up to 1.8 μm to meet the constraint of a BV_{DS} close to 150 V. Different values of BV_{DS} as a function of W_{drift} are summarized in Table III.

Table III. DMOSFET breakdown voltage *vs.* n-drift thickness assuming an electric field threshold of 1.9 MV/cm and $N_{drift} = 1\times10^{16}$ cm^{-3}.

W_{drift} (μm)	BV_{DS} (V)
10	900
8	800
6	700
4	500
3	350
2	200
1.8	150

The influence of the n-drift doping concentration on BV_{DS} was also evaluated. In particular, decreasing the doping concentration N_{drift} from 1×10^{16} cm^{-3} to 1×10^{15} cm^{-3} we calculated a decrease in the critical electric field with a maximum reduction of BV_{DS} on the order of 10% for the same drain leakage current level assumed previously. For example, for the device in Table II, we simulated $BV_{DS} = 850$ V for $N_{drift} = 3\times10^{15}$ cm^{-3} as in [23]. However, N_{drift} has only a limited effect on the device BV_{DS} characteristics considering the thinner values of W_{drift} (*i.e.*, $W_{drift} \leq 3$ μm in Table III) [7].

4.2. ON-state characteristics and temperature effect

The I_D - V_{DS} curves of a DMOSFET which has $W_{drift} = 1.8$ μm and $N_{drift} = 3\times10^{15}$ cm^{-3} are shown in Fig. 2 for V_{GS} from 10 V to 14 V. From the simulations, in fact, it was pointed out that the device is in a really on-state for $V_{GS} > 8$V at room temperature.

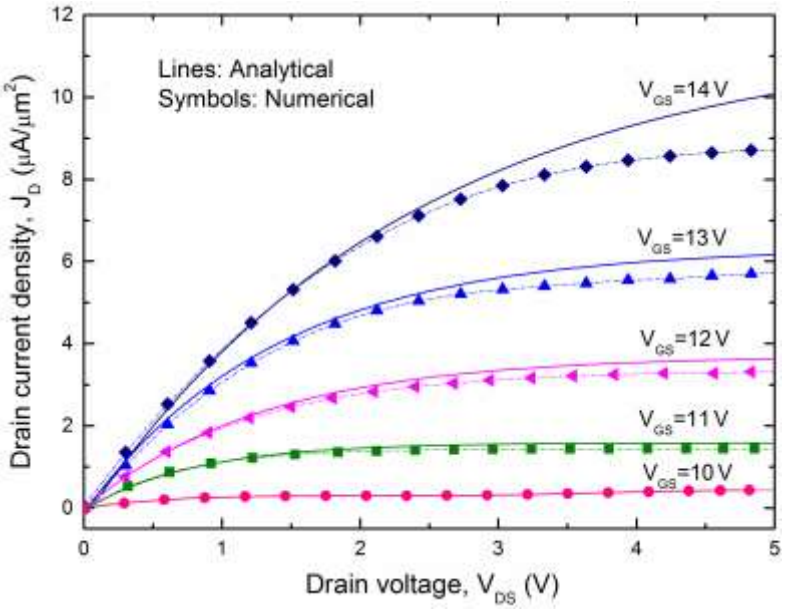


Fig. 2. DMOSFET forward J_D - V_{DS} characteristics at T = 300 K. W_{drift} = 1.8 μm and N_{drift} = 3×10^{15} cm^{-3}. The other geometrical and electrical parameters are those listed in Table II.

As we can see, the numerical simulations and the analytical results are in good agreement especially by assuming the device operating in the deep triode region ($V_{DS} \leq 2$ V). For V_{DS} =1 V and V_{GS} = 14 V, the drain current is close to 3.9 μA/μm^2 corresponding to an on-state resistance R_{ON} of about 255 kΩ×μm^2. From Fig. 2, the R_{ON} values calculated for different V_{DS} as a function of V_{GS} are plotted in Fig. 3.

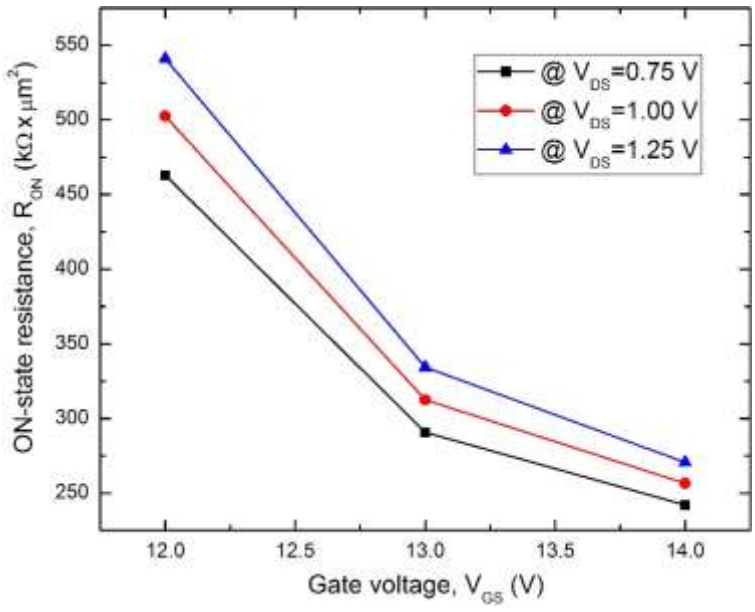


Fig. 3. R_{ON} as a function of V_{GS} for different V_{DS} at T = 300 K.

It is worthwhile noting that, although for comparison purposes with the results reported in [23] an isotropic mobility behavior was assumed by default, during the simulations the impact of an anisotropic model in determining the device R_{ON} was also evaluated. In particular, the anisotropic mobility model was defined with different parameters along the x- and y-direction in Fig. 1 which we can suppose applied to the planes <1100> and <0001> [32] within the 4H-SiC structure, respectively. In other words, the MOS channel lies in the high mobility plane <1100>, whilst the perpendicular plane <0001> is characterized by a resistive longer path over which the drain current flows. By assuming for the Caughey-Thomas mobility model parameters in Table I a perpendicular to parallel ratio of 0.83 as suggested in [53], the variation of R_{ON} for different mobility behaviors is shown in Fig. 4.

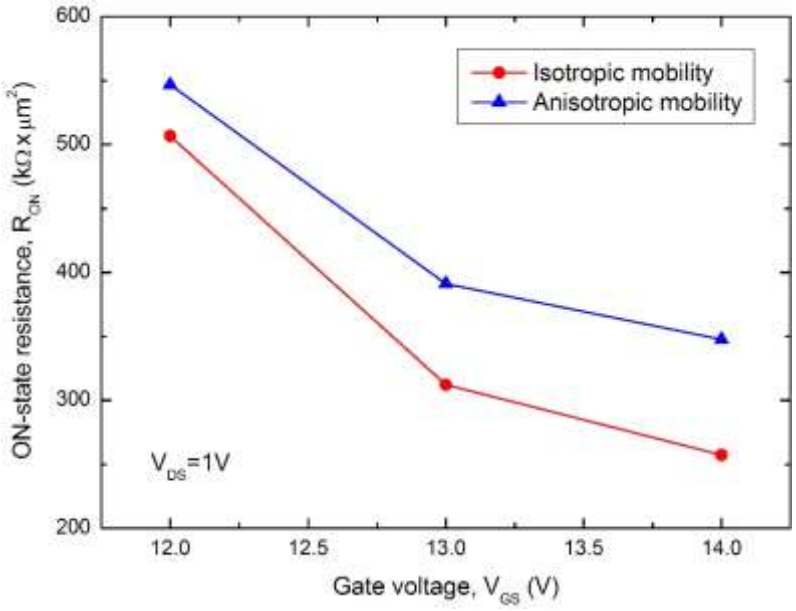
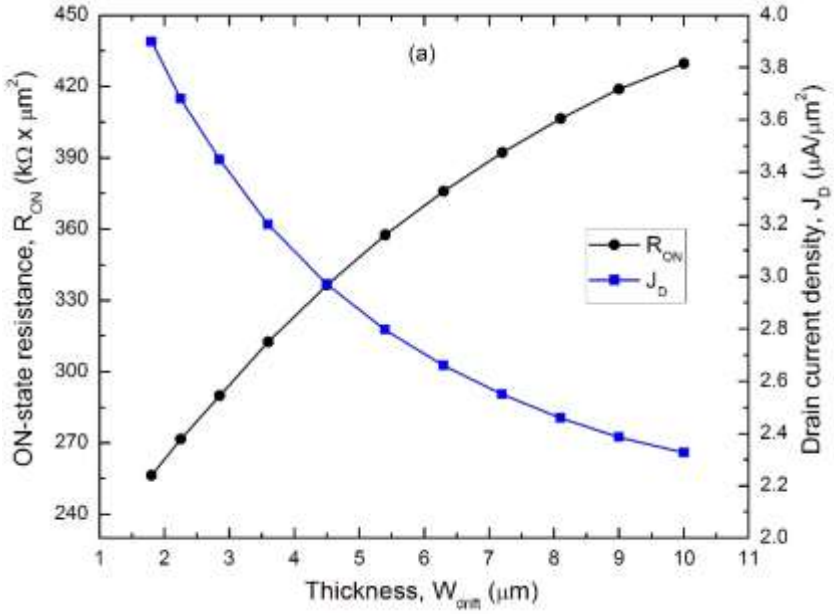


Fig. 4. R_{ON} as a function of V_{GS} for different mobility behaviors at T = 300 K.

By accounting for the current degradation in the plane <0001> due to the thickness and doping concentration of the drift region, the anisotropic mobility gives higher values of R_{ON} and the isotropic model determines an average underestimation of R_{ON} on the order of 25% in the considered voltage range.

The drift region thickness W_{drift} and doping concentration N_{drift}, as well as the channel length L_{ch}, are critical parameters affecting R_{ON} as shown in Fig. 5 for V_{GS} = 14 V and V_{DS} = 1 V.


(a)
ON-state resistance, R_{ON} (kΩ x μm^2)
Drain current density, J_D (μA/μm^2)
Thickness, W_{drift} (μm)
R_{ON}
J_D
450
420
390
360
330
300
270
240
4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
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2.0
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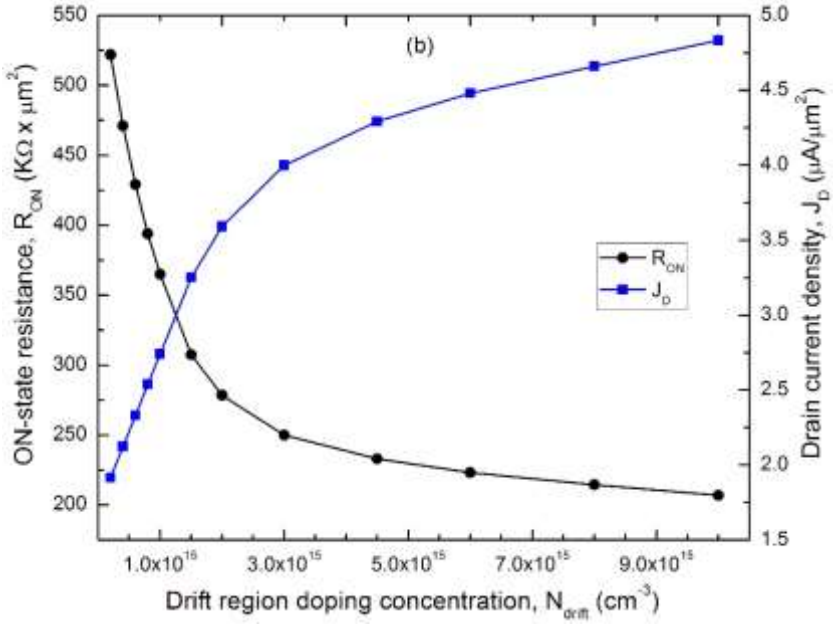

(b)
ON-state resistance, R_{ON} (KΩ x μm^2)
Drain current density, J_D (μA/μm^2)
Drift region doping concentration, N_{drift} (cm^{-3})
R_{ON}
J_D
550
500
450
400
350
300
250
200
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0x10^{16}
3.0x10^{15}
5.0x10^{15}
7.0x10^{15}
9.0x10^{15}

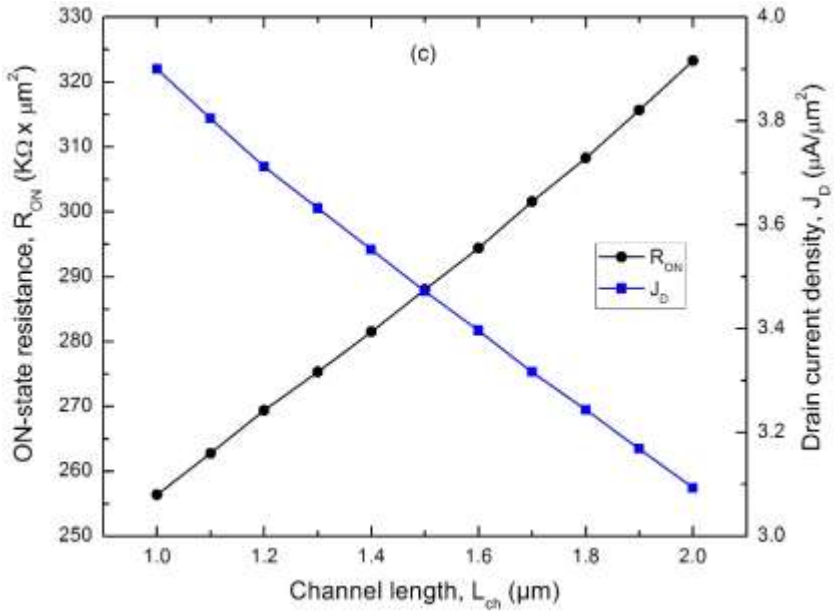
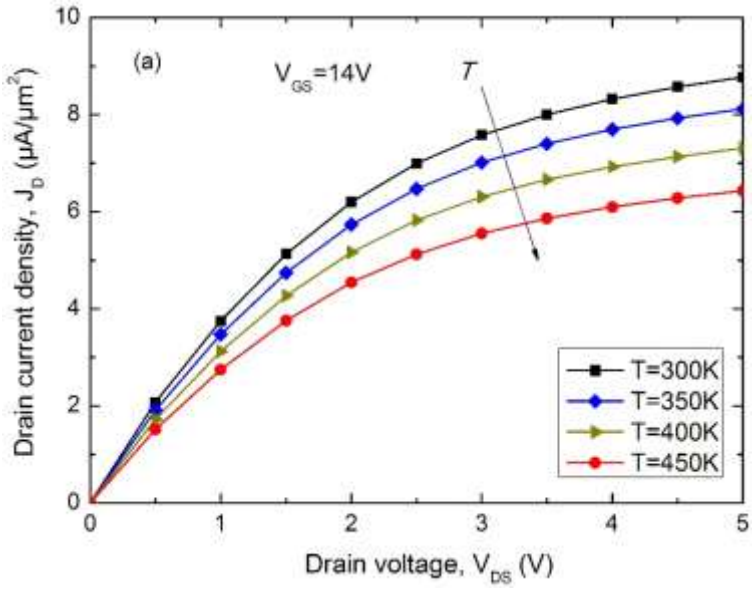


Fig 5. R_{ON} and J_D behaviors as a function of (a) W_{drift}, (b) N_{drift}, and (c) L_{ch}, for V_{GS} = 14 V and V_{DS} = 1 V.

From Fig. 5 (a) and (b) the drain current increases with decreasing W_{drift} and increasing N_{drift} as a result of the R_{ON} decreasing due to a reduction of its component R_{drift}. On the other hand, from Fig. 5 (c) an increasing channel length tends to increase R_{ON} via the component R_{ch} in a rather linear manner.

The effect of the temperature on the device current capabilities is shown in Fig. 6 (a) and (b).



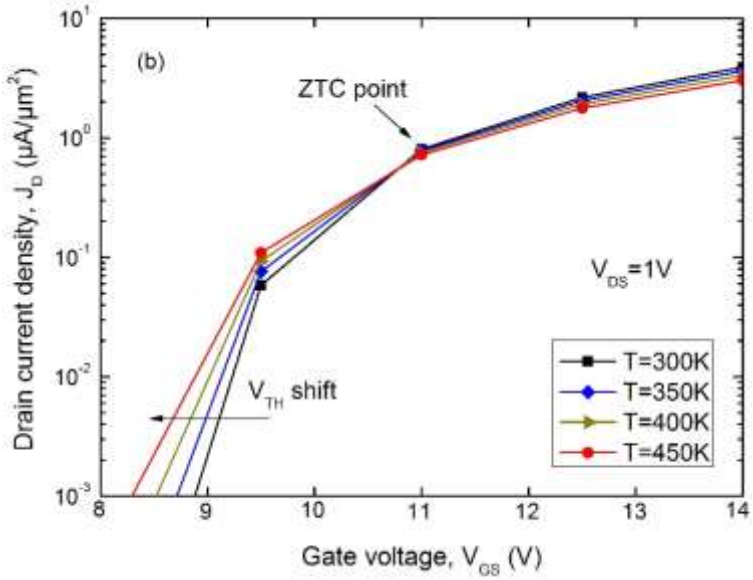


Fig. 6. (a) J_D-V_{DS}, (b) J_D–V_{GS} curves in the 300-450 K temperature range. W_{drift} = 1.8 μm and N_{drift} = 3×10^{15} cm^{-3}.

As expected, J_D decreases with increasing temperature in Fig. 6 (a). This effect is due to the temperature dependence of the carrier mobility and the overall increase of R_{ON} as shown in Fig. 7. In particular, the increased temperature limits the current components which origin in the inversion layer and the drift regions [7]. At the same time, linked to the increase of the 4H-SiC intrinsic carrier concentration, from Fig. 6 (b) we can note that the DMOSFET threshold voltage tends to decrease leading to a zero temperature coefficient (ZTC) point close to V_{GS} = 11 V.

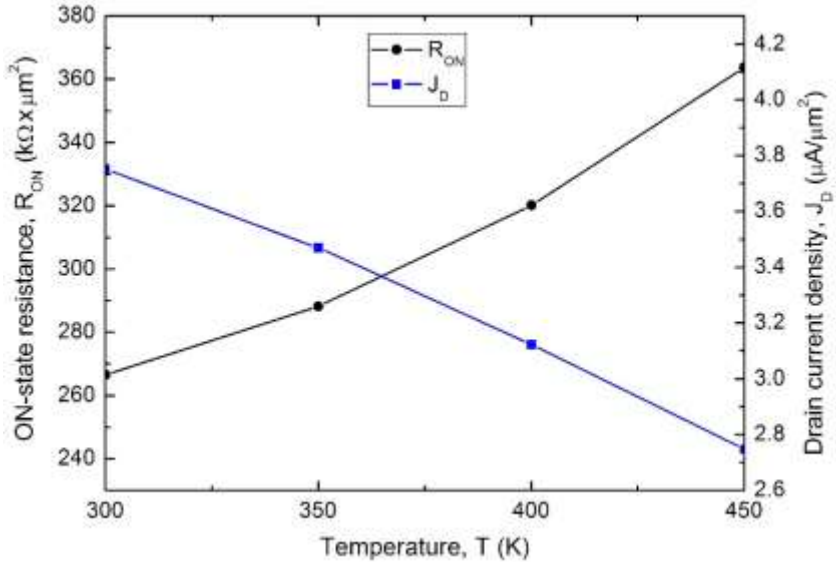


Fig. 7. R_{ON} and J_D behaviors as a function of the temperature for V_{GS} = 14 V and V_{DS} = 1 V.

Finally, keep fixed the base depth and the distance between the base regions, we simulated the R_{ON} behavior for different doping concentrations in the JFET region under the gate oxide (N_{JFET}). In the adopted doping range of N_{JFET} (3×10^{15} cm^{-3} - 3×10^{16} cm^{-3}), the results show that this parameter has only a limited impact on R_{ON} at the different temperatures, resulting the device on-state current capabilities weakly dependent on the majority carrier concentration in the JFET region where the inversion layer is formed.

5. Theoretical basis for MOGA

In recent years, MOGA-based techniques have gained great popularity in the scientific community and encompass many research areas focused on the optimal solution of multi-dimensional and nonlinear problems [54-57]. Distinctive characteristics of the MOGA approach are the universality and simple implementation. It is well known that the majority of optimization procedures provide a single solution. In contrast, MOGA-based techniques permit to find a set of optimized solutions commonly called "Pareto front" that allow to select an appropriate combination of results according to the application field.

The background in this scenario is to establish many proper arguments, namely a set of objective functions, different constraints, and design parameters. Then, the multi-objective optimization provides different solutions achieving the best compromise between the considered functions. Moreover, the criteria can involve dilemma and/or complementary conditions.

A simplified schematic flowchart for a multi-objective genetic algorithm is shown in Fig. 8. As we can see, it is based on the application of selection, crossover, and mutation operations on a certain generation. Starting from an initial population, these operations allow the algorithm to evolve through different generations up to a required criterion is reached. Otherwise, the constraint on the maximum number of iterations will determine its end.

In MOGA terminology, a population is a set of chromosomes generated randomly where each chromosome is made of numbered units called genes. The genes correspond to the design physical and geometrical fitting parameters (e.g., drift region thickness and doping, channel length, and so on). The initial population is made of two chromosomes (parents) and the operation of crossover consists in combining them to obtain a new chromosome called offspring. This process is repeated for all the chromosomes to yield the best offspring. At the same time, the mutation occurs at the genetic level and assures the exploration of all the parameters taken into account. Finally, the selection permits the choice of the best offspring to create the next population.

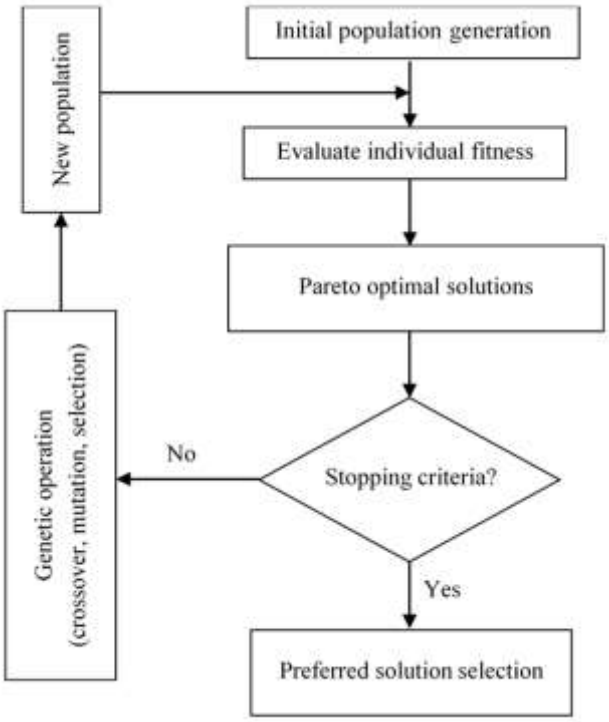


Fig. 8. Schematic flowchart for a multi-objective genetic algorithm.

6. 4H-SiC DMOSFET optimized design

In this section, the MOGA-based technique is used to support the numerical and analytical simulation results in order to find the 4H-SiC DMOSFET optimized design in terms of breakdown voltage and ON-state resistance. In other words, we deal with two objective functions that are considered in the form of $BV_{DS}(Y)$ and $R_{ON}(Y)$ where $Y = \{t_{ox}, W_G, L_{ch}, W_{drift}, X_{JP}, X_{N+}, X_{JFET}, N_A, N_D, N_{drift}\}$ is a vector of device parameters.

The design optimization is evaluated according to the following purpose: minimization of the ON-state resistance maximizing the breakdown voltage for a fixed drain-source voltage range. Proper constraints in determining the physical and geometrical parameters in *Y* with respect to their realistic values were defined during the computations. Also, tournament selection and scattered crossover techniques were employed to generate random vectors and each combination of *Y* was binary coded by biomimicry considerations.

A full set of configuration parameters assumed for the MOGA-based optimization is summarized in Table IV [58,59].

Table IV. Configuration parameters used for the MOGA-based optimization.

Number of variables	10
Population size	1000
Maximum number of generations	100
Selection	tournament
Crossover	scattered
Mutation	adaptive feasible migration
Crossover fraction	0.8
Migration fraction	0.2
Pareto front population fraction	0.5

It is worth to note that a MOGA-based technique can use indifferently either the analytical or numerical models as fitness functions. However, the complexity of the DMOSFET design, which involves different interwoven parameters, suggests to evaluate the algorithm computational time performing a comparison between the procedures based on numerical or analytical prerequisites. Moreover, as shown previously, the output I_D-V_{DS} characteristics of both models are in good agreement within the device triode region.

In order to deal with this computational time comparison, the weighted sum approach method was used to incorporate the two objective functions defined above in a single one expressed by

$$F(Y) = w_1(1/BV_{DS}) + w_2 R_{ON} \tag{14}$$

where the optimal solution varies according to the values of the weighting factors w_1 and w_2. In particular, we considered three cases, namely (a) $w_1 = 0.25,\ w_2 = 0.75$, (b) $w_1 = w_2 = 0.5$, and (c) $w_1 = 0.75,\ w_2 = 0.25$. The $F(Y)$ behaviors as a function of the evolving generations needed to determine the algorithm convergence in the cases (a), (b), and (c) are shown in Fig. 9.

As we can see, for a mono-objective function $F(Y)$ based on a numerical fitness function the convergence occurs within 28 (a), 18 (b) and 5 (c) generations, respectively. In contrast, it occurs within 55 (a), 35 (b) and 28 (c) generations for the analytical assumption. In addition, these latter optimization procedures required a much longer computational time (about twice), which takes about 10-15 minutes on an up-to-date PC. For the sake of rapidity, therefore, in what follows only the numerical model is considered.

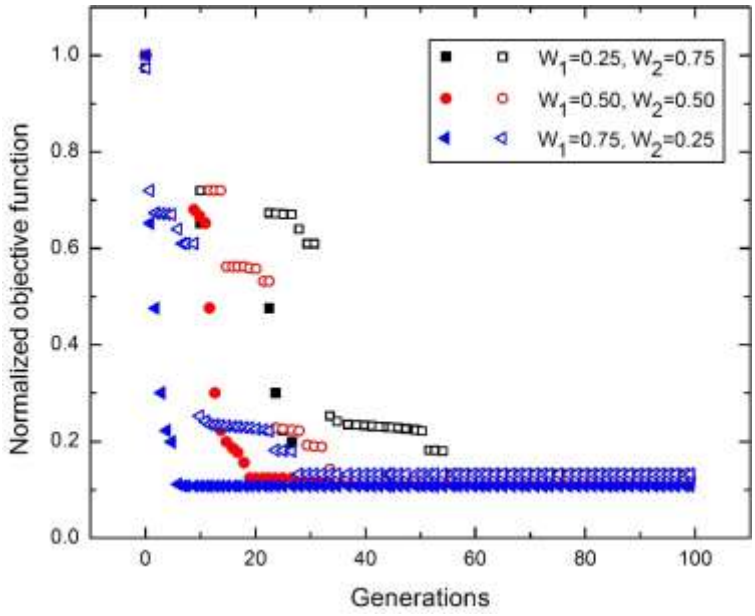


Fig. 9. $F(Y)$ behavior *vs.* generations for different weighting factors w_1 and w_2 by using both the numerical (filled symbols) and the analytical (empty symbols) models as fitness functions.

The Pareto front with the assumed objective functions $R_{ON}(Y)$ and $BV_{DS}(Y)$ is depicted in Fig. 10. Each pair of solutions (R_{ON}, BV_{DS}) corresponds to a specific combination of the vector Y.

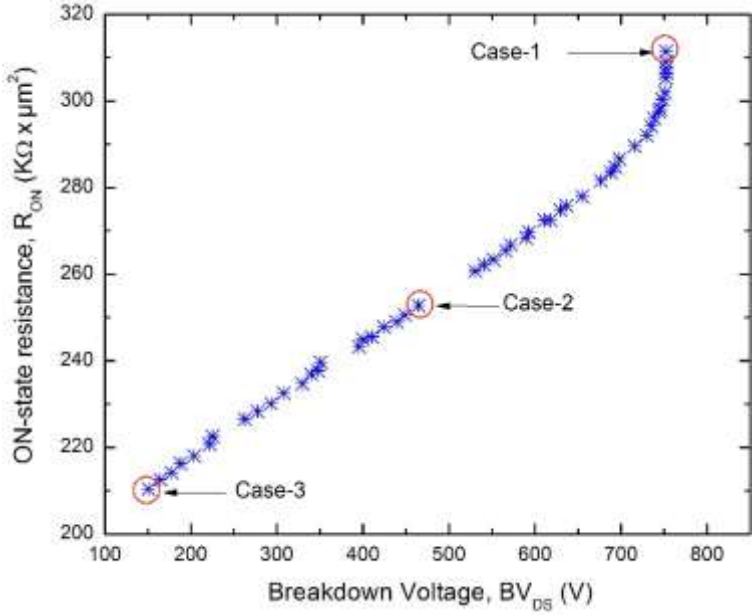


Fig. 10. Pareto-optimal solutions for the DMOSFET design.

As shown in Fig. 10, we chosen three pairs of solutions to assess the accuracy of the proposed optimization in the design of a device rated for BV_{DS} of 150 V (case-1), 450 V (case-2), and 800 V (case-3), respectively. The relative

geometrical and physical parameters are summarized in Table V. Here, the fundamental device parameters reported in [23], which refer to a 4H-SiC DMOSET with the same device footprint area (15 μm^2) and dimensioned for BV_{DS} = 150 V, are also listed for comparison. The R_{ON} values are calculated for V_{GS} = 14 V and V_{DS} = 1 V.

Table V. MOGA-based optimization of the 4H-SiC DMOSFET design parameters.

Design parameters	**Case 1**	**Case 2**	**Case 3**	**[23]**
Silicon oxide thickness, t_{ox} (μm)	0.085	0.085	0.085	0.08
Source thickness, X_{N+} (μm)	0.5	0.5	0.5	0.5
Channel length, L_{ch} (μm)	1.06	1.14	1.0	1.0
Base junction depth, X_{JP} (μm)	2.0	2.0	1.65	1.5
Base-to-base distance, X_{JFET} (μm)	6.13	6.72	7.6	7.0
Epilayer thickness, W_{drift} (μm)	10	3.75	1.8	1.8
Gate width, W_G (μm)	8.65	9.4	10	9.4
N^+-source doping, N_D (cm^{-3})	1×10^{18}	1×10^{18}	1×10^{18}	1×10^{18}
P-base doping, N_A (cm^{-3})	1×10^{17}	1×10^{17}	1.25×10^{17}	1.5×10^{17}
N-drift doping, N_{drift} (cm^{-3})	2.88×10^{15}	2.89×10^{15}	2.89×10^{15}	3×10^{15}
Objective functions				
ON-state resistance, R_{on} (kΩ×μm^2)	315	250	210	260
Breakdown voltage, BV_{DS} (V)	800	450	150	150

In order to better highlight the efficiency of the proposed design strategy, a comparison with the R_{ON} results calculated in [23] for V_{GS} that spans from 11 V to 15 V and V_{DS} = 1 V is shown in Fig. 11.

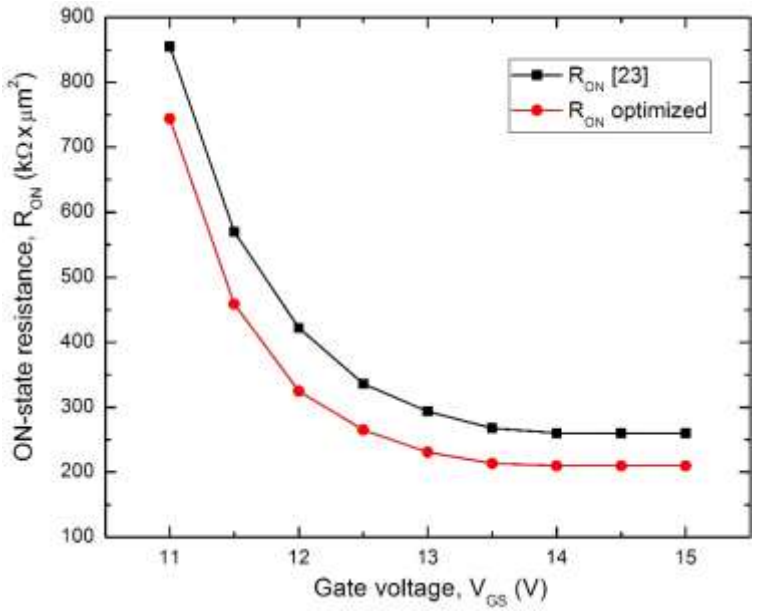


Fig. 11. R_{ON} comparison between the MOGA-based results and those reported in [23].

It can be clearly seen that, for a device with the same BV_{DS} value, the MOGA-based optimization performs a lower R_{ON} in the whole explored V_{GS} range. In a full ON-state condition, R_{ON} decreases by a factor up to 20%.

7. Conclusion

The optimized design of a 4H-SiC DMOSFET for a specific application has been carried out via a multi-objective genetic algorithm. The device electrical characteristics have been investigated in terms of the ON-state resistance and the breakdown voltage by means of both analytical and numerical models obtaining a good agreement in the considered voltage range. In order to evaluate the effective device performance, the temperature effect and the drain current degradation due to an anisotropic carrier mobility behavior have also been introduced. Afterward, the simulation models have been used as fitness functions for a MOGA-based design aimed to fix the optimal geometrical and physical parameters that minimize the ON-state resistance value for devices with different breakdown voltages (150-800 V). The analytical and numerical results have also been used as a basis to evaluate the MOGA analysis effectiveness. By referring to a low-voltage DMOSFET dimensioned for BV_{DS} = 150 V, the optimized device performs a R_{ON} value close to 210 kΩ×μm^2 which is decreased by a factor 20% with respect to that reported in a previous work.

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Figure captions

Fig. 1. Cross-sectional view of the n-channel 4H-SiC DMOSFET single-cell. The drawing is not in scale.

Fig. 2. DMOSFET forward J_D - V_{DS} characteristics at T = 300 K. W_{drift} = 1.8 μm and N_{drift} = 3×10^{15} cm^{-3}. The other geometrical and electrical parameters are those listed in Table II.

Fig. 3. R_{ON} as a function of V_{GS} for different V_{DS} at T = 300 K.

Fig. 4. R_{ON} as a function of V_{GS} for different mobility behaviors at T = 300 K.

Fig 5. R_{ON} and J_D behaviors as a function of (a) W_{drift}, (b) N_{drift}, and (c) L_{ch}, for V_{GS} = 14 V and V_{DS} = 1 V.

Fig. 6. (a) J_D -V_{DS}, (b) J_D –V_{GS} curves in the 300-450 K temperature range. W_{drift} = 1.8 μm and N_{drift} = 3×10^{15} cm^{-3}.

Fig. 7. R_{ON} and J_D behaviors as a function of the temperature for V_{GS} = 14 V and V_{DS} = 1 V.

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