Analysis of the *I-V-T* characteristics of Au/*n*-InP Schottky barrier diodes with modelling of nanometer-sized patches at low temperature

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The aim of the work is to investigate the current-voltage (*I-V*) characteristics of inhomogeneous Au/*n*-InP Schottky barrier (SB) diodes in the 100-300 K temperature range. More in detail, a numerical simulation study is carried out by using a physical device simulator and the diode *I-V* experimental curves are fitted both in forward and reverse bias conditions by explaining the current transport mechanisms at low temperature. Tunneling current flows through the native oxide and nanometer-sized patches embedded at the Au/*n*-InP interface. These patches determine a lower barrier height (local) which is temperature-dependent and responsible of the diode current behaviors in the low bias regime. The patch area is in the order of one-millionth of the total diode area and the SB is between 0.01 and 0.3 eV in the patch region. The simulations are in good agreement with the measurements in the whole explored current range extending over six orders of magnitude.

Keywords: Schottky diode, barrier height, numerical simulation, patch area.

INTRODUCTION

Among III-V semiconductors, indium phosphide (InP) is one of the most interesting material that has received great attention in the last two decades thanks to the high electron mobility, direct transition band-gap, and radiation hardness [1,2]. By considering these electronic properties, the InP substrates are particularly suited for Schottky contact-based devices which found application in many technological areas, such as infrared detectors, sensors in thermal imaging, and metal-semiconductor field-effect transistors [3-5]. On the other hand, the major drawback of the InP Schottky contact is its low barrier height (~ 0.5 eV) which could lead to high leakage currents [6-8].

From literature data concerning the electrical characteristics of Schottky barrier diodes (SBDs), often it was highlighted an abnormal temperature dependence of the fundamental device parameters, namely the barrier height (BH), ideality factor, and series resistance [9-15]. These results require a clear understanding of the barrier nature and the charge transport mechanisms at the metal-semiconductor (MS) interface. For example, in [9] the temperature dependence of the SBD parameters was explained considering the diode current dominated by an explicit thermionic-field emission effect and the presence of deep levels near the MS interface. Other works [10-13] deal with a Gaussian distribution of the BH based on the Werner and Güttler's model [16] as well as the Tung's model [17]. In [14] a modified thermionic emission (TE) theory, which takes into account the presence of MS interface states, was used. Finally, in [15] the experimental results were fitted by assuming a BH inhomogeneity and by tuning the saturation current equation with a transmission coefficient across the interfacial region.

In the last decade, the presence of BH inhomogeneities and thin oxide layers at the contact interface of InP-based diodes was experimentally discussed in several papers [7,8,11,18,19]. The BH inhomogeneities were successfully detected by microscopy techniques, such as ballistic electron emission microscopy (BEEM) and atomic force microscopy (AFM). More in detail, nanometer-sized regions, so-called "patches", were recognized randomly distributed with lower BHs [18,19]. At the same time, the creation of a native oxide was revealed as unavoidable when exposing the semiconductor surface to the clean room air even if the InP surface was treated with adequate polishing and chemical etching process steps and the metal evaporation was carried out in a proper vacuum system [7,8,11].

In this paper, the experimental current-voltage (*I-V*) characteristics of Au/*n*-InP SB diodes are investigated at low temperature ($100 \leq T \leq 300$ K) by means of a physical device simulator modelling an inhomogeneous BH with nanometer-sized patches embedded at the MS interface. A preliminary simulation study, which neglects the BH spatial inhomogeneities, was already presented in [20]. There, the model appeared useful to describe the diode current behaviors at operation temperatures up to 400 K, but failed to fit the measurements for $T \leq 200$ K.

By fitting the *I-V-T* experimental results reported in [21], this work highlights the patch effect in determining a BH behavior which is strictly dependent on the atomic structure at the InP surface, in particular at the lower temperatures ($T < 160$ K). The thermionic emission theory and tunneling phenomena are assumed as current transport mechanisms. The simulation setup ensures a good agreement between the simulations and the measurements for different voltages and temperatures.

DEVICE STRUCTURE AND SIMULATION BACKGROUND

The considered Au/*n*-InP SB structure is shown in Fig. 1. The *n*-InP substrate doping concentration is 1.2×10^{16} cm^{-3} and a circular dot of gold (Au) with a diameter of 1 mm performs the Schottky contact. A low resistance ohmic contact on the backside of the sample is made by evaporating an 88%Au:12%Ge alloy. Further details about the fabrication process are reported in [21].

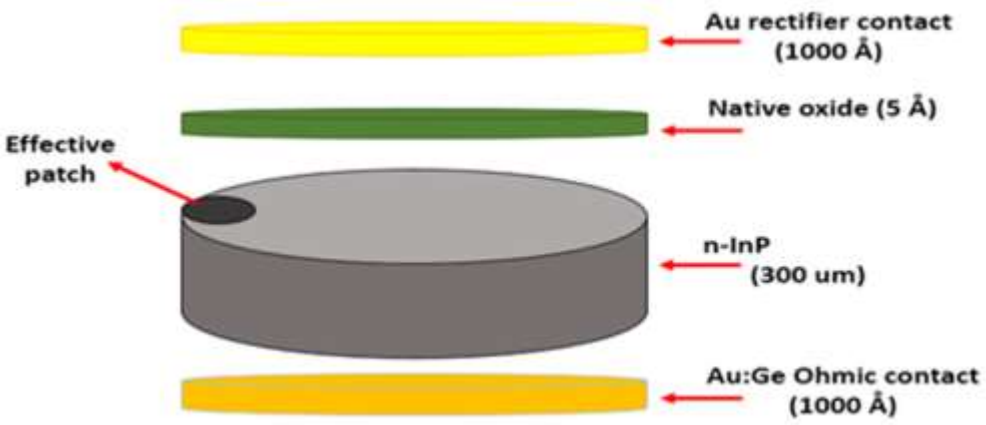


Fig. 1. Au/*n*-InP SB structure with a native oxide layer and nanometer-sized patches at the contact MS interface. The drawing is not in scale.

In Fig. 1, a small circular region called effective patch with specific radius and BH lower than the BH of the InP Schottky contact represents the overall low-BH region distributing on the *n*-InP surface under a thin-film oxide. The presence of the native oxide layer at the Au/*n*-InP interface of the samples with a thickness of a few angstroms was experimentally discussed in [21].

For a finely meshed device structure, the numerical simulation setup was developed by means of the Atlas-Silvaco 2D physical simulator. The fundamental physical models, which mainly influence the device electrical characteristics, include the Shockley-Read-Hall and Auger recombination processes, the impact ionization, the incomplete ionization of impurities, and the band-gap and carrier mobility as a function of temperature [22-25]. Details about the physical models used during the simulations are reported in recent author papers focused on Schottky [12,13,20] and p-i-n structures [26-31]. Key parameters in this study are the Au work function of 4.8 eV [32], the native oxide dielectric constant of 7.9 [8], and the InP electron affinity and dielectric constant of 4.38 eV and 12.4 [2], respectively.

MODELLING OF THE CURRENT-VOLTAGE EXPRESSION

By taking into account nanometer-sized patches embedded at the MS interface, according to the Tung's model based on the TE theory, the total current flowing in the SB can be written as [17]

$$I_{total} = I_s[exp(\beta V_a) - 1] \times \left[1 + C_i A_p exp\left(\beta^2 \frac{\sigma^2}{2}\left(\frac{V_{bb}}{\eta}\right)^{\frac{2}{3}}\right)\right] \quad (1)$$

where $I_s = A^* A T^2 exp(-\beta \emptyset_{b0})$ is the saturation current, $V_{bb} = V_{bi} - V_a$ is the difference between the built-in potential (V_{bi}) and the applied bias voltage (V_a), $\beta = q/kT$, and $\eta = \varepsilon_{sc}/qN_d$ is a device constant. In (1), A is the barrier homogeneous area, A^* is the effective Richardson constant, $\emptyset_{b0}$ is the BH of the junction (mean value), σ is the standard deviation of the patch distribution, C_i is the total patch density, and A_p is the effective area of one patch given by [33]

$$A_p = \frac{8\pi\sigma^2}{9}\left(\frac{\eta}{V_{bb}}\right)^{1/3} . \quad (2)$$

The effective area of the patch region is therefore calculated as

$$A_{eff} = A\, C_i A_p. \quad (3)$$

The diode current in (1) is, in practice, defined by two components (double diode effect). The former is related to the current flowing through the homogeneous barrier, which dominates at high temperatures and exhibits an ideality factor close to 1. The latter represents an additional current with an ideality factor greater than 1, which is due to the presence of the low-BH patches that cannot be neglected at low temperatures and low bias voltages [9-11].

The cumulative patch effect may be represented by an overall small region with a local temperature-dependent BH that is in the form of [34]

$$\emptyset_p = \frac{q\sigma^2}{2kT}\left(\frac{V_{bb}}{\eta}\right)^{\frac{2}{3}}. \quad (4)$$

The difference between the BH when the Schottky barrier is homogeneous ($\emptyset_{hom}$) and $\emptyset_p$ defines the effective BH, i.e.

$$\emptyset_{eff} = \emptyset_{hom} - \frac{q\sigma^2}{2kT}\left(\frac{V_{bb}}{\eta}\right)^{\frac{2}{3}}. \quad (5)$$

RESULTS AND DISCUSSION

An accurate simulation analysis of the device *I-V* characteristics that accounts for the patch effects can be performed after determining the terms A_{eff} and $\emptyset_{eff}$ introduced above. More in detail, for the A_{eff} calculation we considered the modified Richardson plot achieved from the following expression of the saturation current [34]

$$ln\left(\frac{I_S}{A_{eff}T^2}\right) - \frac{\beta^2\sigma^2 {V_{bb}}^{2/3}}{2\eta^{2/3}} = ln(A^*) - \beta\emptyset_{hom} \quad (6)$$

by assuming C_i as fitting parameter [34,35]. This expression is in accordance with the Gaussian distribution of the patches at the SB interface [17]. In addition, the standard deviation σ is taken from the plot $\emptyset_{eff}$ vs. $\beta/2$ shown in Fig. 2. In fact, the intercept with the ordinate axis gives the $\emptyset_{hom}$ value and σ can be derived from the line slope according to (5) [36].

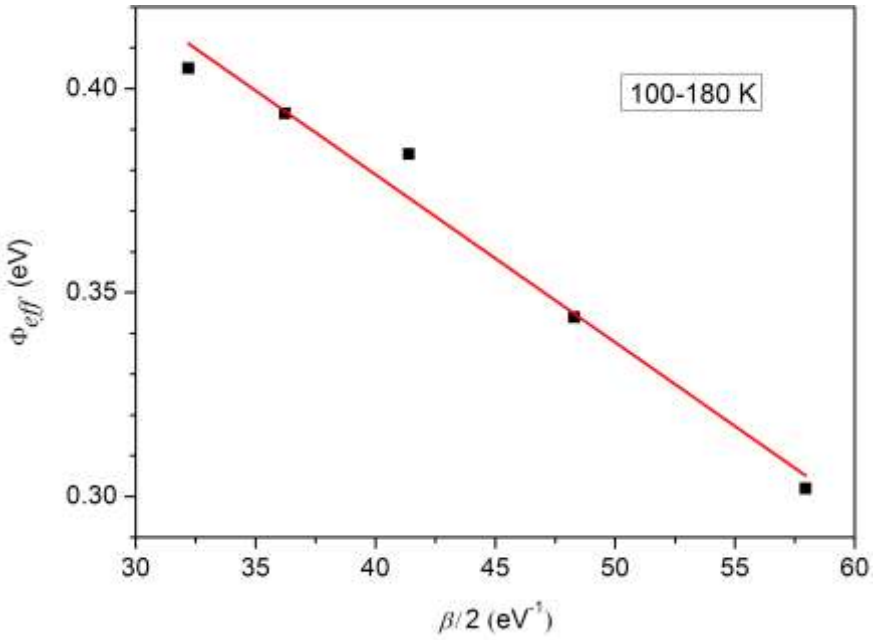


Fig. 2. $\emptyset_{eff}$ vs. $\beta/2$ for the Au/*n*-InP Schottky contact from 100 K to 180 K in steps of 20 K.

The plot shows a good linear fit for $\emptyset_{hom}$ = 0.543 eV. The σ values and the effective patch parameters calculated in the considered temperature range for C_i = 2×10^6 cm^{-2} are listed in Table I. This value of C_i is consistent with the results reported in [36]. The saturation current I_s is extracted from the diode experimental characteristics.

Table I. Patch parameters from the TE theory.

T (K)	I_s (A)	V_{bb} (V)	σ (cm$^{2/3}$)	A_p (cm^2)	A_{eff} (cm^2)	$\emptyset_{eff}$ (eV)
180	6×10^{-12}	0.36	7.08×10^{-5}	1.64×10^{-11}	2.58×10^{-7}	0.424
160	5×10^{-13}	0.367	7.04×10^{-5}	1.55×10^{-11}	2.44×10^{-7}	0.409
140	2×10^{-14}	0.373	7×10^{-5}	1.44×10^{-11}	2.27×10^{-7}	0.39
120	4×10^{-15}	0.38	6.95×10^{-5}	1.56×10^{-11}	2.45×10^{-7}	0.364
100	8×10^{-16}	0.387	6.91×10^{-5}	1.58×10^{-11}	2.47×10^{-7}	0.328

Starting from (6), the modified Richardson plot is shown in Fig. 3. The best fit results in a straight line and, from the intercept with the ordinate axis, the Richardson's constant is calculated close to 10.8 AK^{-2}cm^{-2}. This result is in good agreement with the expected theoretical value of 9.4 AK^{-2}cm^{-2} for n-InP [36]. Also, the correspondent BH $\emptyset_{hom}$ is 0.48 eV in close agreement with the result extracted from Fig. 2.

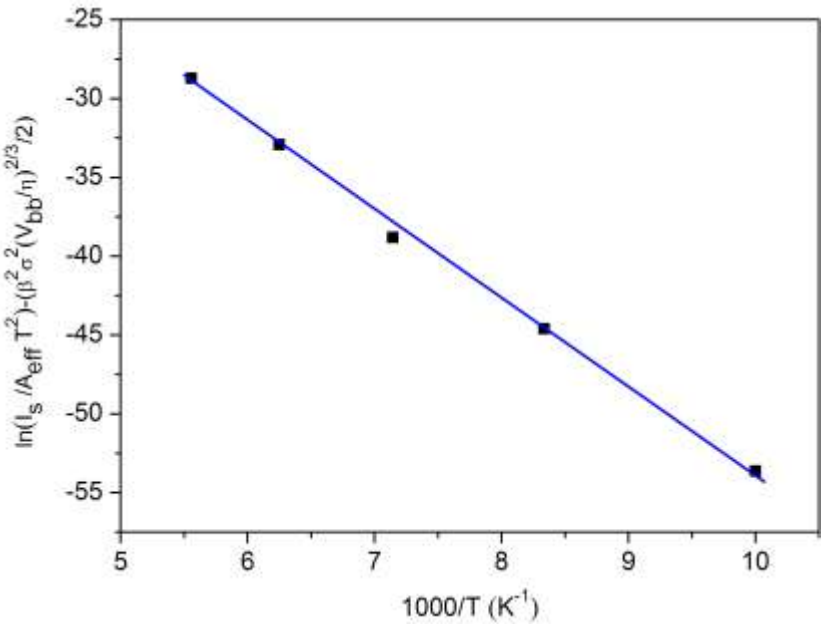


Fig. 3. Modified Richardson plot according to the Tung's model in the 100-180 K temperature range.

By using the effective patch parameters in Table I, the *I-V-T* characteristics of the Au/*n*-InP Schottky diode were simulated as shown in Fig. 4 both in forward (a) and reverse (b) bias. Here, the experimental measurements are also reported for comparison. As we can see, the simulated reverse and low-forward bias currents appear so much lower than the experimental data at all temperatures. This disagreement has to be ascribed to the use of the Tung's model and the extraction of the barrier parameters by means of the pure TE theory, while the dominating transport mechanism could be relate to tunneling phenomena as discussed in [20].

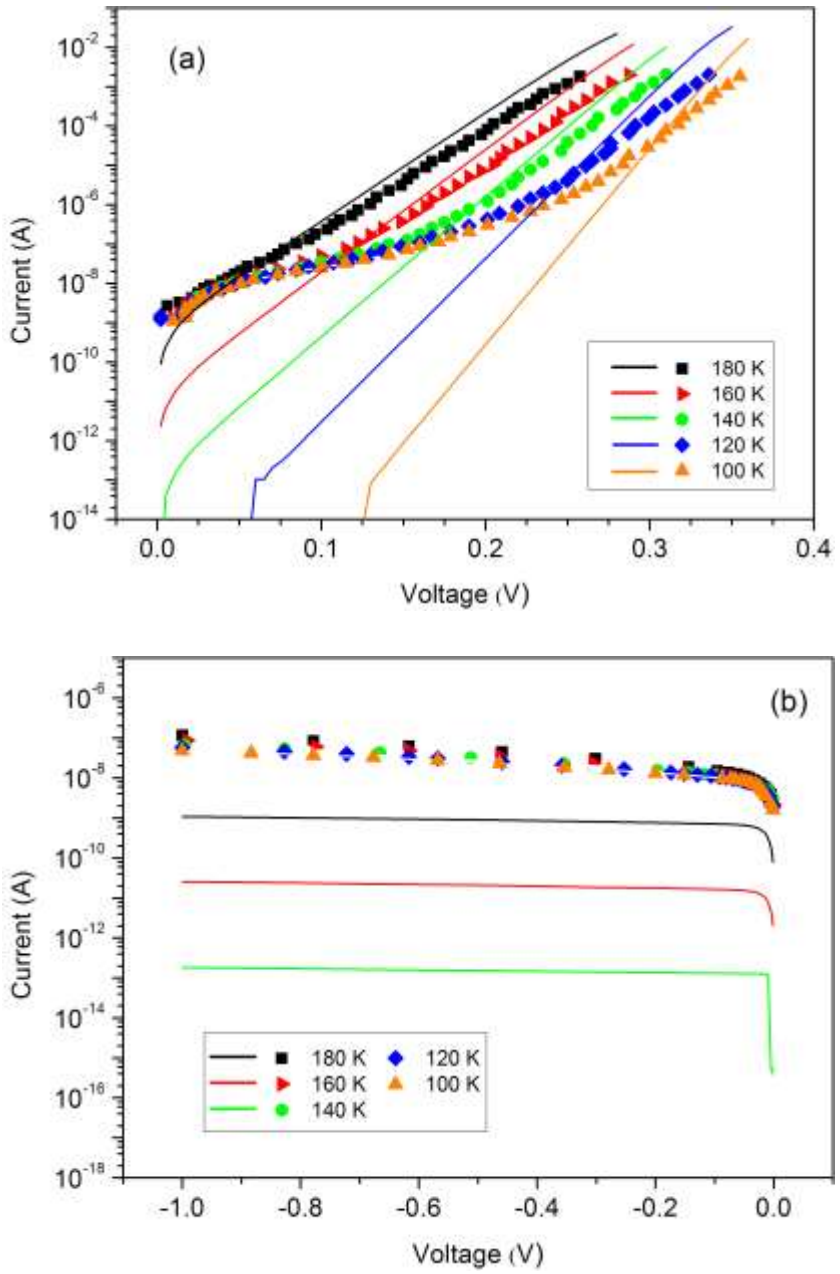


Fig. 4. *I-V-T* experimental data (symbols) and the simulated characteristics (solid lines) by using the patch parameters in Table I. (a) Forward bias. (b) Reverse bias.

From the measurements, the conventional Richardson's plot of $\ln(I_s/T^2)$ is shown in Fig. 5. Here, the temperature dependence of the ideality factor calculated in the low-medium regime of the curves in Fig. 4 (a) is also reported.

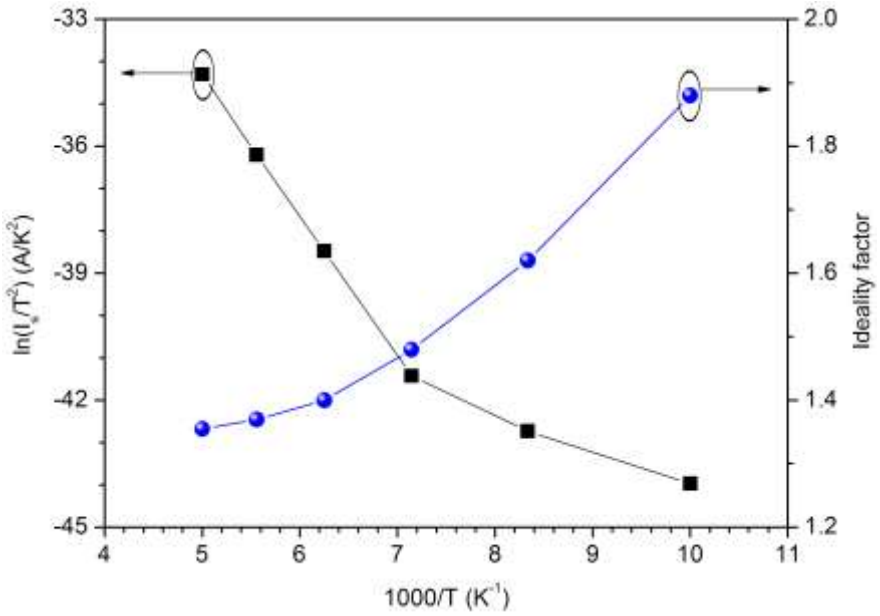


Fig. 5. Richardson plot and ideality factor vs. 1000/T for the experimental curves in Fig. 4 (a).

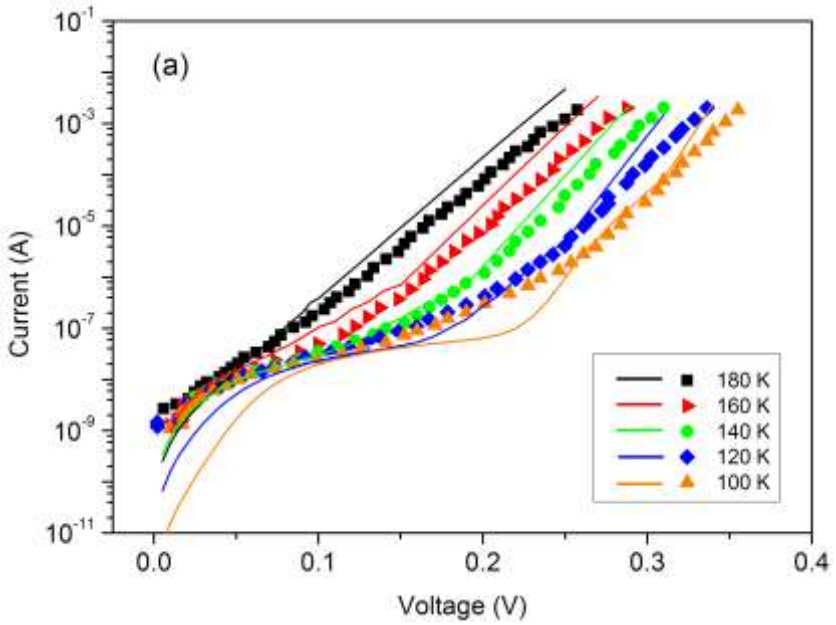
A noticeable curvature in the Richardson's plot occurs for $T \leq 140$ K due to the temperature dependence of the diode BH. Whereas a quite straight line indicates that the current tends to flow through a uniform SB, the curvature confirms the presence of low barrier areas at the MS interface which determine the effective junction current at the lower temperatures [17]. At the same time, the ideality factor is strongly dependent on temperature. In particular, as the temperature decreases the diode current more and more flows through the lower barrier patches increasing the slope of the forward *I-V* characteristics before the series resistance effect becomes predominant. Moreover, high values of the ideality factor, which are mainly due to the presence of the oxide layer in the device structure, confirm that there is a deviation from the standard TE theory in the current conduction mechanism [37].

In order to overcome the curve disagreement in Fig. 4 (a) and (b), we carried out a new set of simulations by taking A_p and $\emptyset_p$ as fitting parameters. In particular, we performed the simulations assuming A_p in the limit of one-millionth of the total diode area while $\emptyset_p$ is much lower than the BH homogeneous value. The revised patch parameters are listed in Table II and the comparison between the simulated and measured *I-V-T* characteristics is shown in Fig. 6.

Table II. Patch parameters used in the simulations to fit the diode *I-V-T* experimental characteristics as shown in Fig. 6.

T (K)	Reverse bias		Forward Bias	
	$\emptyset_p$(eV)	A_p (cm^2)	$\emptyset_p$(eV)	A_p (cm^2)
100	0.01	1.256×10^{-11}	0.10	3.14×10^{-10}
120	0.02			
140				
160				
180			0.15	

It is important to note that the parameters in Table II are consistent with the literature data on SB inhomogeneities. In fact, in [38] it was found that a large amount of current comes from small patches with a low BH decreasing as the temperature decreases. Also in [39] the authors showed that the junction current almost originates from isolated small patches (radius < 20 nm) with a local BH lower up to 0.4 eV than the homogeneous barrier. In [40] it was highlighted that most of the diode current is contributed by few and deep patches in the tail of the Gaussian distribution. Finally, in [41] for Au/InP-based structures with Ag nanoparticles at the Au/InP interface the radius of the patches was estimated between 7 and 17 nm and the relative BH ranging from 0.05 to 0.3 eV.



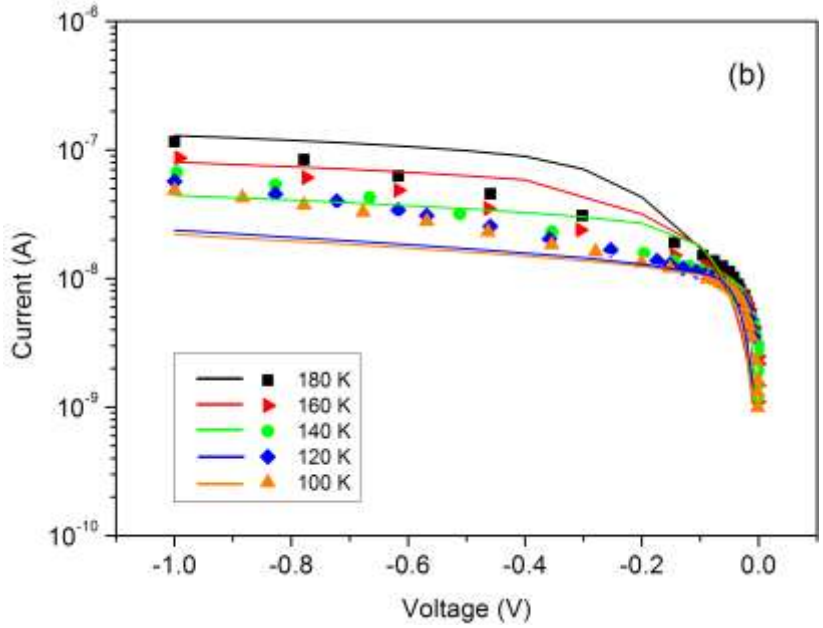


Fig. 6. *I-V-T* experimental data (symbols) and the simulated characteristics (solid lines) by using the patch parameters in Table II. (a) Forward bias. (b) Reverse bias.

From Table II, the reverse current flows through a patch region with an area in the order of 1.256×10^{-11} cm^2 and two different BHs close to 0.01 eV at T = 100 K and 0.02 eV in the 120-180 K temperature range. On the other hand, the forward current is originated from a patch region with an area of 3.14×10^{-10} cm^2 and a BH close to 0.15 eV at T = 180 K and 0.1 eV in the 100-160 K temperature range. In reverse bias the cumulative patch radius is estimated in the order of 20 nm and A_p is less by a factor 25 compared to the patch area calculated in forward bias.

We must highlight that, since the *I-V-T* forward and reverse bias curves were simulated always as an unique solution, the patch parameters used in the reverse bias simulations do not affect the device forward bias characteristics and vice versa. In addition, we can consider the forward current flowing through the patch region as the total current flowing through several patches with a size close to the value assumed in the reverse bias.

The simulated *I-V-T* curves in Fig. 6 agree well the experimental results. More in detail, as stated above, in reverse bias the current is basically due to electrons flowing through a patch region with a BH which decreases with decreasing temperature. Similarly, in forward bias and, in particular, in the low-bias range the current is mainly dominated by electrons flowing through patches with a temperature-dependent $\emptyset_p$. This low-bias range extends up to about 0.3 V at T = 100 K and it decreases with increasing temperature, namely when the forward current more and more is originated from electrons flowing through the homogeneous barrier as confirmed hereafter.

The proposed BH analysis, in fact, was also discussed referring to the Norde's study reported in [42]. There, an analytical function $F(V)$ in the form of

$$F(V) = \frac{V}{2} - \frac{kT}{q} ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{7}$$

was proposed to determine different BH values in a Schottky diode. In particular, the plot of $F(V)$ as a function of the forward bias voltage should be a straight line with a negative slope in the bias range wherein the series resistance effect is negligible. Then, $F(V)$ starts to increase. The minimum of this behavior, namely the $F(V_{min})$ value, is a point of interest and the Schottky BH can be calculated as follows:

$$\emptyset_{b0} = F(V_{min}) + \frac{V_{min}}{2} - \frac{kT}{q} \quad . \tag{8}$$

By using the *I-V-T* experimental data, the $F(V)$ plot of the investigated SB is shown in Fig. 7.

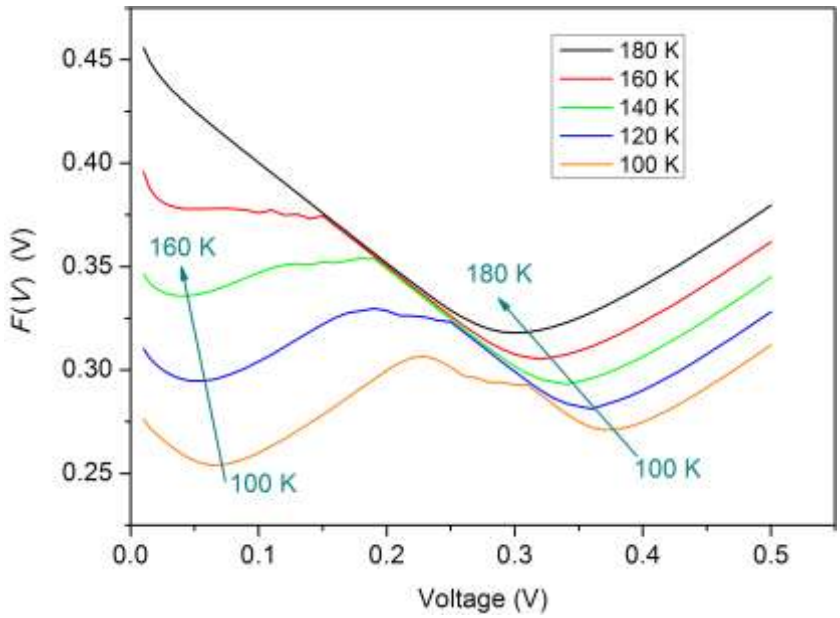


Fig. 7. Norde model of $F(V)$ by using the *I-V-T* experimental data.

As we can see, the $F(V)$ behaviors show two interesting regions. The first region (low-bias) is located below 0.2 V and it represents the bias region wherein the diode current is due to electrons flowing through the patch region. The point of interest (minimum) is well highlighted at T = 100 K and tends to be suppressed with increasing temperature, namely when the forward current becomes dominated by electrons flowing through the homogeneous barrier at any voltage. This current transport mechanism well depicts also to the second region (high-bias) which is located above 0.25 V. The results, in fact, reveal that an increased bias voltage tends

to homogenize the BH distribution. The values extracted by using the Norde's model are listed in Table III.

Table III. $\emptyset_{b0}$ extracted by using the Norde's model.

T (K)	$\emptyset_{b0}$ (eV)	
	Low-bias	High-bias
100	0.277	0.447
120	0.309	0.450
140	0.334	0.451
160	/	0.451
180	/	0.452

As expected, the BH values at the low-bias level are lower than the values extracted in the high-bias regime showing an evident temperature dependence. These results are in accordance with $\emptyset_p$ and $\emptyset_{hom}$ calculated previously.

Finally, it is worthwhile noting that, by fixing the patch role on the device physics, the adopted simulation setup allows an accurate analysis of the diode current capabilities in a wide range of temperature as shown in Fig. 8 ($100 \leq T \leq 300$ K).

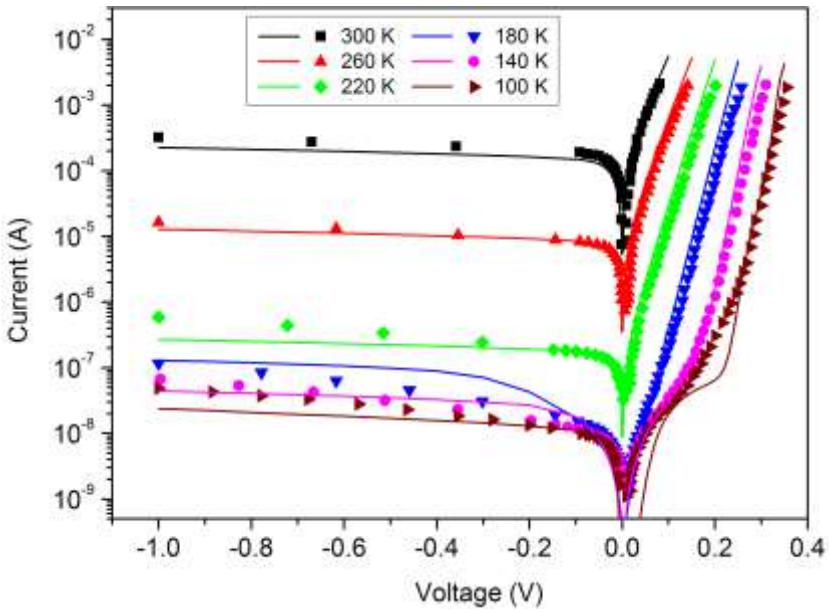


Fig. 8. *I-V* experimental data (symbols) and simulated curves (solid lines) as a function of temperature.

With a good data agreement over several orders of magnitude for current, this work extends and revises the simulation results reported in [20].

CONCLUSION

The *I-V-T* characteristics of Au/*n*-InP SB diodes have been investigated in a wide range of temperature (100-300 K) by taking into account the presence of a native 5 Å-thick oxide layer with nanometer-sized patches embedded at the contact interface. From the experimental results, the behavior of the conventional Richardson's plot and the temperature dependence of the ideality factor confirm the presence of low barrier areas at the MS interface which de facto determine the diode current curves at very low temperature ($T < 160$ K). Starting from the Tung's model, a good agreement between the simulations and the measurements has been achieved introducing in the simulations an overall patch region with fine-tuned parameters. More in detail, it was found that in reverse bias the tunneling current flows through a patch region with a cumulative radius close to 20 nm and a BH depending on the temperature (i.e., 0.01 eV at $T = 100$ K, and 0.02 eV in the range $120 \leq T \leq 180$ K). At the same time, the forward current flows, in principle, through a patch region with radius close to 100 nm and different BH values (i.e., 0.15 eV at 180 K and 0.1 eV in the range $100 \leq T \leq 160$ K). The developed analysis is also in accordance with the results extracted from the Norde's model.

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FIGURE CAPTIONS

Fig. 1. Au/*n*-InP SB structure with a native oxide layer and nanometer-sized patches at the contact MS interface. The drawing is not in scale.

Fig. 2. $\emptyset_{eff}$ vs. $\beta/2$ for the Au/*n*-InP Schottky contact from 100 K to 180 K in steps of 20 K.

Fig. 3. Modified Richardson plot according to the Tung's model in the 100-180 K temperature range.

Fig. 4. *I-V-T* experimental data (symbols) and the simulated characteristics (solid lines) by using the patch parameters in Table I. (a) Forward bias. (b) Reverse bias.

Fig. 5. Richardson plot and ideality factor vs. 1000/*T* for the experimental curves in Fig. 4 (a).

Fig. 6. *I-V-T* experimental data (symbols) and the simulated characteristics (solid lines) by using the patch parameters in Table II. (a) Forward bias. (b) Reverse bias.

Fig. 7. Norde model of *F*(*V*) by using the *I-V-T* experimental data.

Fig. 8. *I-V* experimental data (symbols) and simulated curves (solid lines) as a function of temperature.