Analysis of 4H-SiC MOSFET with distinct high-k/4H-SiC interfaces under high temperature and carrier-trapping conditions

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Abstract

In this work, the reliability of different oxide/4H-SiC interfaces under high temperature and carrier-trapping conditions are investigated carefully. In more detail, the carrier-trapping and temperature effects are considered in the electrical characterization of a low breakdown 4H-SiC-based MOSFET by using in turn SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2 as gate dielectric. A gate oxide with a high relative permittivity notably improves the transistor performance. In addition, HfO_2 assures the MOSFET best immunity behaviors. The obtained results are explained in terms of the carrier channel mobility, device on-state resistance, and oxide electric field. By using HfO_2, however, an increased gate leakage current is calculated. This drawback is overcome by inserting a thin interfacial layer (2nm-thick) in the HfO_2/4H-SiC MOS structure. In particular, two alternative gate stacked dielectrics, involving either SiO_2 or Al_2O_3, have proven their effectiveness in preserving the transistor on-state figures of merit while limiting the gate leakage current in the whole explored gate voltage range. To support the prediction capabilities of the presented modeling analysis, the simulations results are compared with experimental data from literature resulting in a good agreement. Low power MOSFETs are used in several applications for which reliability and durability are as critical as performance. For example, referring to power optimizers for photovoltaic (PV) modules, which fall under the low-load and low-voltage category of DC–DC converters, these devices significantly increase the energy generated by each single PV module operating under harsh conditions and stressing environments. In addition, they have to ensure high reliability over the long term of operation.

Keywords: 4H-SiC MOSFET; power device; trapping effects; temperature effect; gate oxide; numerical simulations.

1. Introduction

The forthcoming MOSFET downscaling imposes oxide thicknesses on the order of a few nanometers which approach the electron tunneling limit also referring to wide bandgap semiconductors like silicon carbide 4H (4H-SiC). This issue causes high leakage currents in the device structure and the investigation of high-k gate dielectrics, which are alternative to the conventional silicon oxide (SiO_2), is nowadays mandatory [1-3]. In addition, although stoichiometric SiO_2 can be yield by thermal oxidation of SiC similarly to the Si technology, the reliability of SiO_2/SiC-based MOSFETs usually requires different nitration process steps to reduce the density of interface states which deeply limit the device on-state current capabilities [4-6]. As well known, in a MOS structure the interface electric field is inversely proportional to the material dielectric constant. SiO_2, with a dielectric constant of 3.9 suffers for a higher electric field of about 2.5 times if compared to 4H-SiC. Consequently, the oxide breakdown constraint to be fixed needs the MOSFET to work at an electric field far away from the real 4H-SiC breakdown condition which is on the order of 2 MV/cm [7]. This leads to the loss of one of the most important features of 4H-SiC especially for high-power applications. On the other hand, high-k gate dielectrics with a lower oxide field could allow the design of MOSFETs operating in close proximity to the 4H-SiC breakdown limit. Recent researches in this field paid an impressive attention to high-k dielectric materials such as Al_2O_3, Ta_2Si, Gd_2O_3, and AlN [8-11]. Stack structures including SiO_2/TiO_2 and SiO_2/HfO_2 layers have been also considered [12-13]. However, the high-k/4H-SiC interface reliability and stability against interfacial traps and temperature effects are true challenges that still need to be addressed.

In this paper, the main purpose is to study the effects of different gate dielectrics on the performance of a low breakdown 4H-SiC MOSFET. In more detail, we consider different designs involving in turn SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3, and HfO_2 as gate dielectrics. The device analysis is focused on the calculation of the oxide electric field, the gate leakage current,

the channel mobility (μ_{ch}), the on-state operation mode resistance (R_{ON}), the transconductance (g_m), the threshold voltage (V_{th}), the threshold voltage shift (ΔV_{th}), and the subthreshold swing (SS).

Moving from recent authors' papers dealing with the design of 4H-SiC MOSFETs for specific applications [14-18], without loss in generality, the presented analysis refers to a transistor dimensioned for a low voltage rating considering the role of different gate dielectrics under high temperature and carrier-trapping conditions. From the obtained results, HfO_2 is a promising material that guarantees the best device performance although a high leakage current can be calculated. To overcome this drawback for the HfO_2/4H-SiC MOS structure, an HfO_2 stacked oxide involving a thin interfacial layer in SiO_2 (or Al_2O_3) is also proposed. This design preserves the transistor on-state figures of merit while limiting the gate leakage current. A comparison with experimental data from literature is reported to support the prediction capabilities of the adopted simulation setup.

This paper is organized according to the following. Firstly, we introduce appropriates physical models to investigate the reliability of different oxide/4H-SiC interfaces under high temperatures and carrier-trapping conditions. Then, we investigate the suitability of a thin interfacial layer in overcoming the high leakage current drawback. Finally, the simulation results are properly discussed with respect to the experimental data.

2. MOSFET structure

The cross-sectional view of 4H-SiC MOSFET half-cell considered in this work is schematized in Figure. 1.

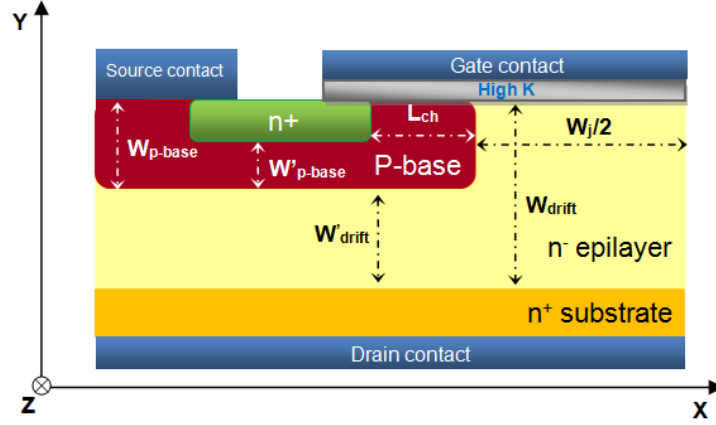


Figure 1. Cross-sectional view of the 4H-SiC MOSFET half-cell (plot not to scale).

Here, the notation adopted for the main geometrical parameters is also reported. In more detail, L_{ch} is the channel length, W_{drift} is the thickness of the n-drift region, $W_{p\text{-}base}$ is the p-based depth, and W_j denotes the gap amid base regions. The physical and geometrical parameters of the primary device are recapitulated in table 1.

Table 1 Mosfet Parameters

Parameter	Value
Gate contact width, W_G (μm)	9.4
Gate oxide thickness, t_{ox} (μm)	0.02
Channel length, L_{ch} (μm)	1
Source thickness (μm)	0.5
Base junction depth, $W_{P\text{-}base}$ (μm)	1.3
Interspace, $W'_{P\text{-}base}$ (μm)	0.8
Distance between the base regions, W_j (μm)	7
Epilayer junction depth, W_{drift} (μm) 150V	1.8
Base-to-substrate distance, W'_{drift} (μm)	0.5
Substrate thickness, W_{sub} (μm)	100
Half-cell width (μm)	7.5
Device footprint area (μm^2)	15
N^+-source doping (cm^{-3})	1×10^{18}
P-base doping (cm^{-3})	1×10^{17}
N-epilayer doping (cm^{-3})	1×10^{15}
N^+-substrate doping (cm^{-3})	1×10^{19}

The epilayer thickness is 1.8 μm assuring a MOSFET blocking voltage (V_{BL}) close to 150 V as verified in [14].

Aluminum (Al) with a work function of 4.26 eV [19] is used as electrode material. To avoid the parasitic bipolar transistors formed by the multiple junction source (n+)/base (p)/epilayer (n)/substrate (n+), the source region and base are short-circuited. Also, the gate contact in Al aids to screen the phonon effects which originate from high-k dielectric materials. The gate oxide physical parameters considered in this work are summarized in Table 2. Here, ε_{ox}, E_g, and ΔE_C refer to the relative permittivity, the material band gap, and the conduction band offset difference, respectively

Table 2 Gate oxide parameters

Oxide	ε_{ox}	Eg (eV)	ΔE_C (eV)
SiO_2 [20]	3.9	9	2.7
Si_3N_4 [20]	7.5	5.3	/
AlN [21]	8.5	6.23	1.7
Al_2O_3 [22]	9.3	8.8	1.7
Y_2O_3 [23]	15	5.6	/
HfO_2 [24]	22	5.9	0.9

3. Physical models

By means of a commercial 2D TCAD simulator [25], the MOSFET structure was finely meshed with mesh spacing scaled down to 0.5 nm in the channel region as well as next to the oxide/4H-SiC interface and all around the p-n junctions. As described in detail in recent papers of ours [26-29], the key physical models used during the simulations include the impact ionization, the incomplete activation of dopants, the doping-dependent carrier mobility and lifetime, the mobility degradation due to scattering mechanisms in the inversion layer, the Shockley-Read-Hall and Auger recombination phenomena, and the 4H-SiC bandgap narrowing [30-34].

More in detail, Auger recombination represents a non-radiative mechanism through which the surplus energy from the recombination of the electron-hole pairs is passed to other electrons

or holes which are eventually stimulated into higher energy states inside the same band rather than giving off photons. The typical Auger expression is in the form [7]

$$R_{Auger} = \left(C_P p + C_n n\right)\left(np - n_i^2\right) \qquad (1)$$

where C_n and C_p refers to appropriate Auger coefficients.

The classic recombination model of the Shockley-Read-Hall (SRH) assumes a defect in the band difference with a single energy point and it is given by [7]:

$$R_{SH} = \frac{pn - n_i^2}{\tau_p\left(n + n_i \exp\left(\frac{E_{trap}}{kT}\right)\right) + \tau_n\left(p + n_i \exp\left(\frac{-E_{trap}}{kT}\right)\right)} \qquad (2)$$

where τ_n and τ_p represent the carrier lifetimes and E_{trap} is the trap energy level.

In order to predict the breakdown voltage accurately, the electron and hole impact ionization rates ($\alpha_{n,p}$) the following expression is used [35]

$$\alpha_{n,p} = \alpha_{0n,p} \exp\left(\frac{-b_{0n,p}}{E}\right) \qquad (3)$$

where $\alpha_{0n,p}$ and $b_{0n,p}$ are specific coefficients [35].

Owing to the wide bandgap of 4H-SiC, not all doping atoms can be considered to be entirely ionised. By means of the Fermi–Dirac statistics, the incomplete ionization of impurities is expressed as in [36]

$$N_{d^+,a^-} = N_{d,a}\left(\frac{-1 + \sqrt{1 + 4g_{d,a}\frac{N_{d,a}}{N_{C,V}(T)}\exp\left(\frac{\Delta E_{d,a}}{kT}\right)}}{2g_{d,a}\frac{N_{d,a}}{N_{C,V}(T)}\exp\left(\frac{\Delta E_{d,a}}{kT}\right)}\right) \qquad (4)$$

where, the subscripts d and a to denote the donor and acceptor terms, $N_{d,a}$ refers to the doping density, $\Delta E_{d,a}$ is the energy level, $g_{d,a}$ is the degeneracy factor of the conduction and valence

band, and N_C and N_V are the conduction and valence states densities, respectively.

Experimentally it is found that the bandgap shrinkage happens when the accumulation of impurities is particularly high. This process is called the narrowing effect of the bandgap attributed to the emergence of overlapping impurity states.

According to Lindefelt's model [37], the bandgap narrowing effect for p-type ($\Delta E_{g,a}$) and n-type ($\Delta E_{g,d}$) regions are expressed as:

$$\Delta E_{ga} = A_a\left(\frac{N_a^-}{10^{18}}\right)^{\frac{1}{2}} + B_a\left(\frac{N_a^-}{10^{18}}\right)^{\frac{1}{3}} + C_a\left(\frac{N_a^-}{10^{18}}\right)^{\frac{1}{4}} \quad (5)$$

$$\Delta E_{gd} = A_d\left(\frac{N_d^+}{10^{18}}\right)^{\frac{1}{2}} + B_d\left(\frac{N_d^+}{10^{18}}\right)^{\frac{1}{3}} + C_d\left(\frac{N_d^+}{10^{18}}\right)^{\frac{1}{4}} \quad (6)$$

The parameters $A_{a,d}$, $B_{a,d}$, and $C_{a,d}$ are listed in Table 3, giving the band edge displacements in eV.

Table 3 Apparent Bandgap Narrowing Model Coefficients

Parameters	**Values**
A_a	1.54×10^{-3}
A_d	1.17×10^{-2}
B_a	1.3×10^{-2}
B_d	1.5×10^{-2}
C_a	1.57×10^{-2}
C_d	1.90×10^{-2}

Based on the experimental validation reported in [38], the Caughey-Thomas model is used to express the carrier mobilities, i.e.

$$\mu_{n,p} = \mu_{0n,p}^{\min} + \frac{\mu_{0n,p}^{\max} - \mu_{0n,p}^{\min}}{1+\left(\frac{N}{N_{n,p}^{crit}}\right)^{\delta_{n,p}}} \quad (7)$$

In (7), N is the local (total) concentration of the ionized impurities, $\mu_{0n,p}^{min}$ represents mobility in the heavily doped material, where scattering of impurities is the main mechanism, $\mu_{0n,p}^{max}$ is the mobility of undoped or unintentionally doped regions, where the primary scattering process is lattice scattering, $N_{n,p}^{crit}$ is the doping concentration at which the mobility is halfway between the $\mu_{0n,p}^{min}$ and $\mu_{0n,p}^{max}$ values, and $\delta_{n,p}$ is an indicator of how rapidly the mobility varies from $\mu_{0n,p}^{min}$ to $\mu_{0n,p}^{max}$. The fundamental model parameters at room temperature are summarized in table 4 [38, 39].

Table 4 Caughey-Thomas Model Parameters

Parameters	n type 4H-SiC	p type 4H-SiC
$\mu^{min}{}_{0}$ (cm^2/V×s)	40	15.9
$\mu^{max}{}_{0}$ (cm^2/V×s)	950	125
$N^{crit}{}_{0}$	2×10^{17}	1.76×10^{19}
δ	0.76	0.34

Furthermore, the mobility decrease at high electric fields, linked to the carrier saturated drift velocity ($v_{sat} = 2\times10^{7}$ cm/s) is described by using the following expression [38].

$$\mu_{n,p}(E) = \frac{\mu_{n,p}}{\left[1+\left(E\frac{\mu_{n,p}}{v_{sat}}\right)^{\kappa_{n,p}}\right]^{\frac{1}{\kappa_{n,p}}}} \tag{8}$$

where E represents the electric field in the current flow path, and $k_n = 2$ and $k_p = 1$ are specific constants that aid to fit the experimental results [25].

In addition, all the simulations are carried out taking into account the multidimensional dependent anisotropic effects. A detailed description of the used model is reported in [25]. Also, to properly consider the scattering mechanisms, such as the phonon scattering, the surface roughness scattering, the impurity scattering, and the coulomb scattering that degrade the

channel mobility, the Lombardi model is set in this work [25]. This model integrates three components of the carrier mobility referring to the Matthiessen's rule as follows:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \qquad (9)$$

where μ_{AC}, μ_{sr}, and μ_b denote the mobility effects caused by the Coulomb scattering, the surface roughness scattering, and the surface phonon scattering, respectively.

To complete the simulation setup, the effects of an explicit density of states (*DoS*) at the gate oxide/4H-SiC interface are modeled as follows. In more detail, the *DoS* is assumed in the form of [30-32]

$$D_{it}(E) = D_{it,M} + D_{it,T} \quad (10)$$

where $D_{it,M}$ and $D_{it,T}$ denote the deep states Gaussian distribution in the mid-gap and the density of band tails next to the valence and conduction band-limits [33,34]. Each term can act either as acceptor-like or donor-like level for free carriers [25].

Finally, in this paper the leakage current in the gate oxide is calculated by using the Fowler-Nordheim (FN) tunneling equation, where non-local dielectric- and dielectric-SiC tunneling is represented by a non-local mesh construction, i.e.,

$$J_{FN} = E_{OX}^2 a \exp(-b / E_{OX}) \qquad (11)$$

where E_{OX} is the electric field in the oxide, and a = 1.82×10^{-7} and b = 1.9×10^{8} are physical constants [25].

4. Prediction capabilities of the simulation setup

It is important to note that the adopted simulation setup and model parameters are already supported by experimental results on 4H-SiC Schottky and p-i-n diodes which were characterized in a wide range of currents (over ten orders of magnitude) and temperatures (300-500 K) [40-42]. Since SiC-based power MOSFETs are usually existing for high-power and medium-to-high-voltage applications ($V_{DS} \geq 600$ V), the simulation setup was tested by comparison with the electrical characteristics of a commercial 900 V 4H-SiC MOSFET [43]. More in detail, similarly to [14], considering a fully depleted drift-region previous to the occurrence of the breakdown (punch-through condition, $W_{drift} \leq \varepsilon_{sc} E_{pn}^{crit} q^{-1} N_{drift}{}^{-1}$), the breakdown voltage BV_{DS} can be calculated using the expression [7]:

$$BV_{DS} = E_{pn}^{crit} W_{drift} - \frac{q N_{drift} W_{drift}^2}{2\varepsilon_{sc}} \qquad (12)$$

where $E^{crit}{}_{pn}$ represents the critical electric field alongside the p-base/n-drift junction, ε_{sc} is the semiconductor permittivity, q is the electric charge, and N_{drift} represents the drift region doping concentration. Therefore, in accordance with (12), we assumed $W_{drift} = 10$ µm to place the breakdown voltage of the simulated MOSFET close to the datasheet value of 900 V as show in Fig. 2.

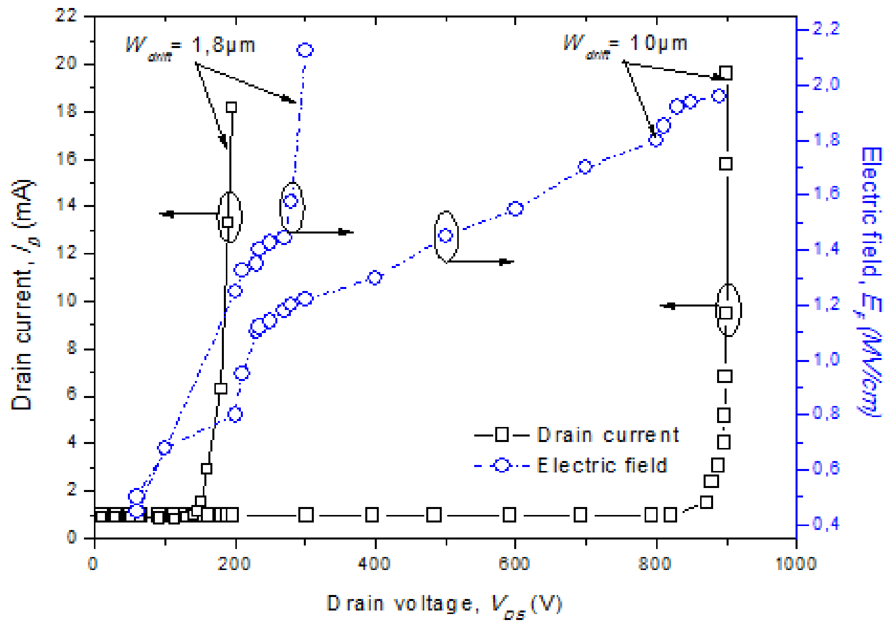


Figure. 2. Breakdown behavior of the simulated MOSFET.

The comparison between the R_{ON} value of the commercial MOSFET and that calculated during the simulations is shown in Fig. 3.

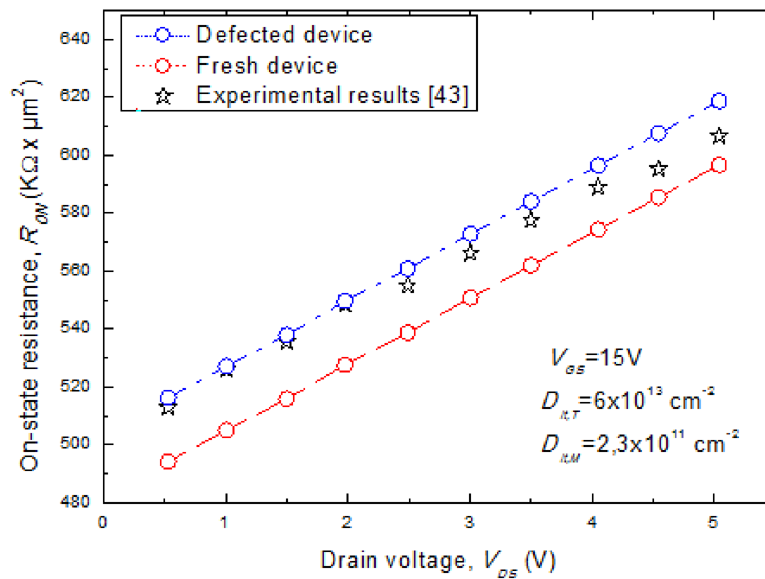


Figure. 3. On-state resistance calculation.

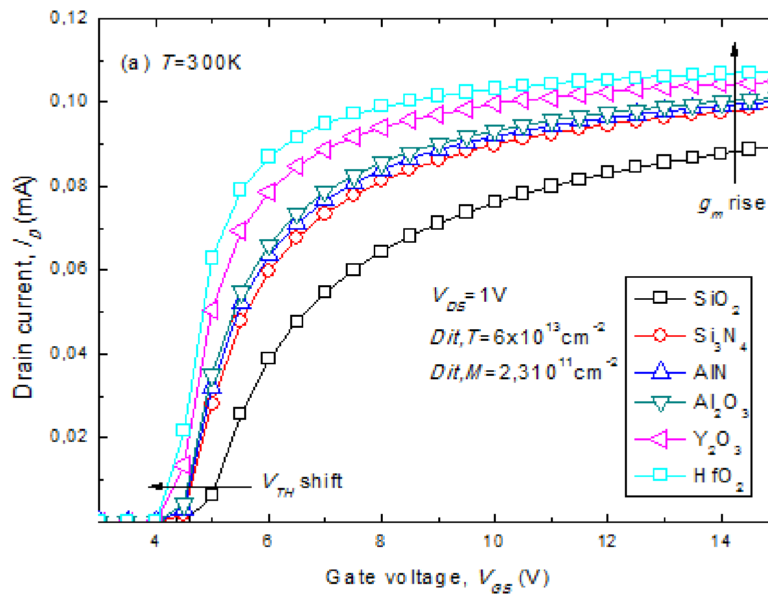
The commercial device footprint is close to 2.1 mm^2 with an effective area of 1.9 mm^2. Starting from a fresh device (no-defects), after several attempts, a good agreement with the experimental data was achieved by assuming the trap density reference values of 6×10^{13} cm^{2}eV^{-1} and 2.3×10^{11} cm^{2}eV^{-1} for the band tail states and mid-gap states, respectively [30].

According to the previous analysis, the thickness of drift region is tuned to the value W_{drift}=1.8µm to put the breakdown voltage of the device close to 150V as shown in Fig. 2. Obviously, the BV_{DS} value becomes smaller as the thickness of the drift region is reduced.

5. Results and discussion

5.1. MOSFET ON-State analysis

The current-voltage I_D−V_{GS} characteristics at 300 K and 423 K of the considered device in table 1, for various gate dielectrics as listed in table 2, are reported in Figure. 4.



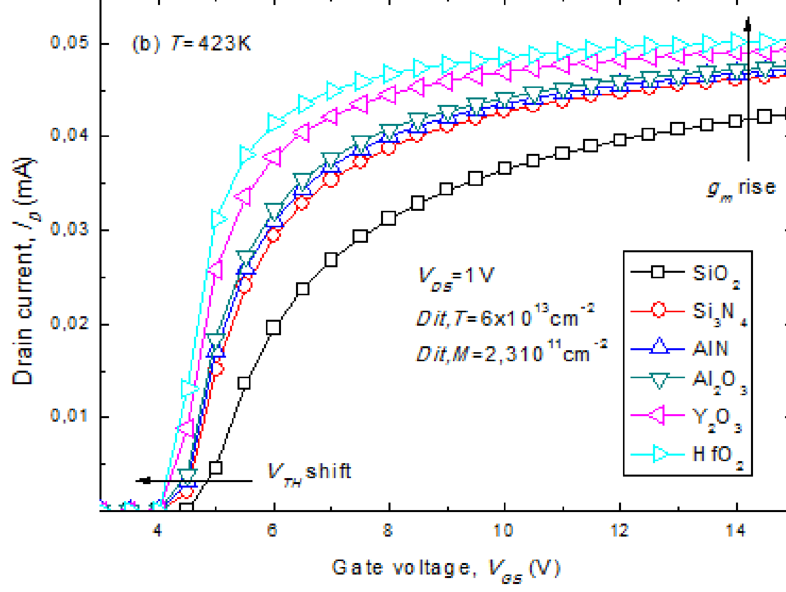


Figure. 4. $I_D - V_{GS}$ curves for the device in Table I with different dielectric value at (a)T = 300 K, (b)T = 423 K.

Here, it is evident that for a fixed oxide thickness (20 nm) the MOSFET threshold voltage (V_{th}) decreases with increasing the oxide permittivity, resulting $3.9 \leq V_{th} \leq 4.5$ V. This result is mainly due to the improved charge density at the conductive channel interface [44].

As verified during the simulations, I_D tends to decrease when increasing the device operating temperature. For example, for T = 423 K we have verified a decrease of the saturated value of I_D on the order of 50%. This is an explicit consequence of the dependence on temperature of the channel mobility along with the overall increase of the device R_{ON} [45-48]. In addition, the raise of intrinsic carrier concentration determines a slight decrease of V_{th} in the limit of 5% for $300 \leq T \leq 500$ K.

The MOSFET transconductance behaviors as a function of the subthreshold swing for different gate dielectrics calculated at T =300 K, 400K, and 500 K are shown in Figure 5. The subthreshold swing represents the necessary gate biasing to shift the drain current by one order of magnitude (one decade). The sub threshold swing is calculated with the standard expression:

$$SS = \frac{d\,(V_g)}{d\,(\log I_d)} \qquad (13)$$

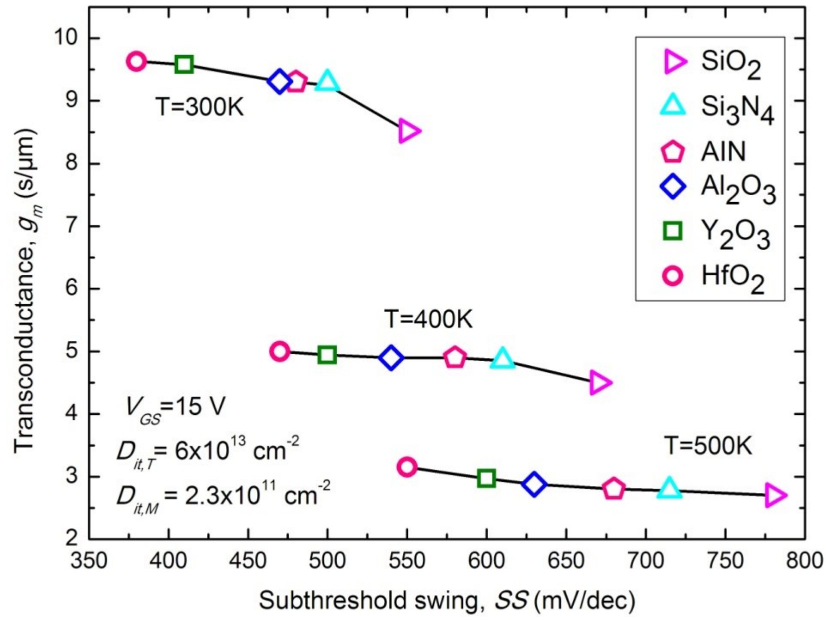


Figure. 5. MOSFET transconductance as a function of the subthreshold swing at different temperatures.

As we can see from this figure, the variations of μ_{ch} and V_{th} determines a severe decrease of g_m with increasing temperatures. Also, at any given temperature the conventional SiO_2 reveals the higher values of subthreshold swing if compared to the other oxide materials. This result is mainly due to the decreased inversion charge density. Obviously, low subthreshold swings aid to get a high on/off current ratio and, for the same V_{GS} difference, we can expect to decrease I_D more efficiently for device switching applications [49, 50].

The effect of temperature on the device channel mobility for different gate dielectric materials is shown in Figure 6.

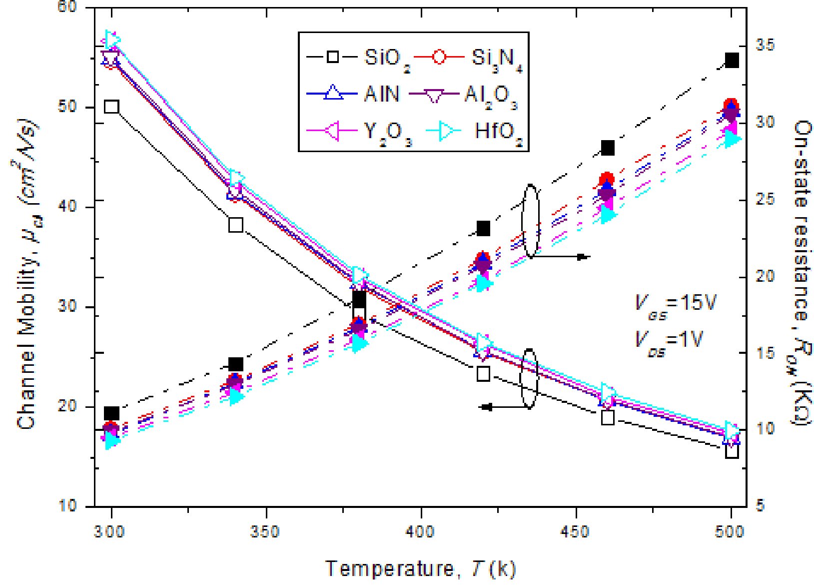


Figure. 6. Channel mobility curve and R_{ON} behavior as a function of temperature.

Here, the channel mobility decreases with increasing temperatures because of the phonon scattering mechanisms occurrence. At the same time, for high-k materials the augmentation of the inversion charge caused by the high value of permittivity helps in screening the traps and reduce the Coulombic scattering phenomena at low temperatures.

The effect of temperature on the device on-state resistance is also depicted in Figure. 6. The more the temperature increases the more the current decrease increasing considerably the R_{ON} value. This fact is due to the phonon scattering mechanisms and Coulomb scattering phenomena originates from the filled traps of mobile charges. In more detail, the gate dielectric with high-k show a R_{ON} value of 11.17 kΩ, 10.1 kΩ, 9.7 kΩ, 9.9 kΩ, 9.5 kΩ, and 9.3 kΩ for SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3, and HfO_2, respectively. These results are due to the role of a higher permittivity that reduce the columbic scattering via screening the traps. Besides, The higher the temperature, the smaller the number of filled traps, therefore the Coulomb scattering decrease and the only mechanism that reduce the mobility and increase the R_{ON} at high temperature is the phonon scattering.

The benefits related to the use of a high-k oxide need to be addressed in terms of the gate

leakage current that certainly affects the MOSFET reliability. The off-state leakage current behaviors as a function of V_{GS} in the subthreshold regime (i.e., $V_{GS} < V_{th}$) are shown in Figure. 7.

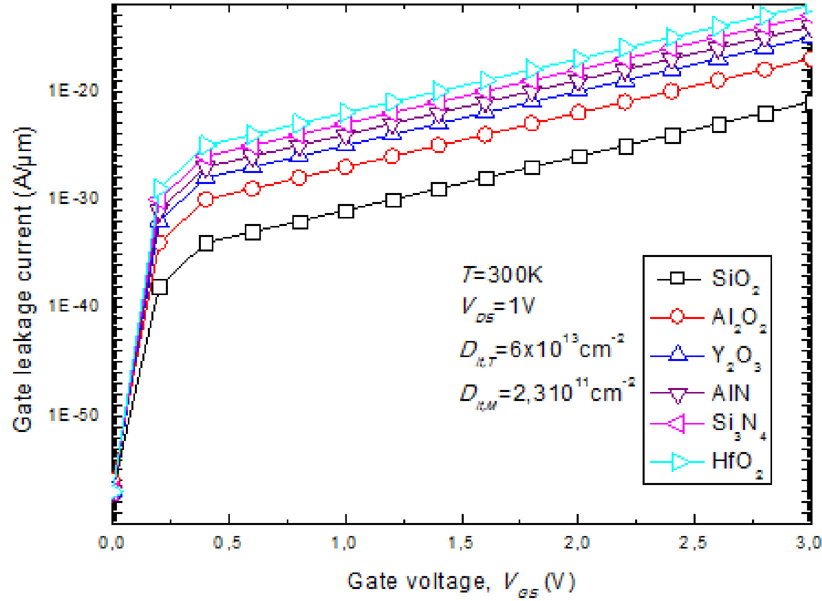


Figure. 7. Gate leakage current in the MOSFET subthreshold regime

As expected, the high-k dielectrics suffer of the higher gate leakage currents that could lead to a premature MOSFET breakdown. This result is mainly due to the reduced ΔE_C which originates in the MOS structure (see Table 2). Although a thicker oxide layer limits the leakage currents showing however undesired detrimental effects on the device on-state figures of merit (e.g. V_{th} shift and g_m drop), as an useful compromise in overcoming this design issue we have supposed a dielectric stack structure where an interfacial layer with a large conduction band offset is inserted at the 4H-SiC interface. For example, by assuming a 2nm-thick SiO_2 interfacial layer in the HfO_2/SiO_2/4H-SiC structure, we have calculated a reduction of the gate leakage current of about 4 orders of magnitude with respect to the results in Figure. 7 in the whole explored V_{GS} voltage range.

The R_{ON} behaviors as a function of V_{GS} for different gate dielectrics are shown in Figure. 8 for $V_{DS} = 1$ V at $T = 300$ K. The imposed bias level places the device in the triode region.

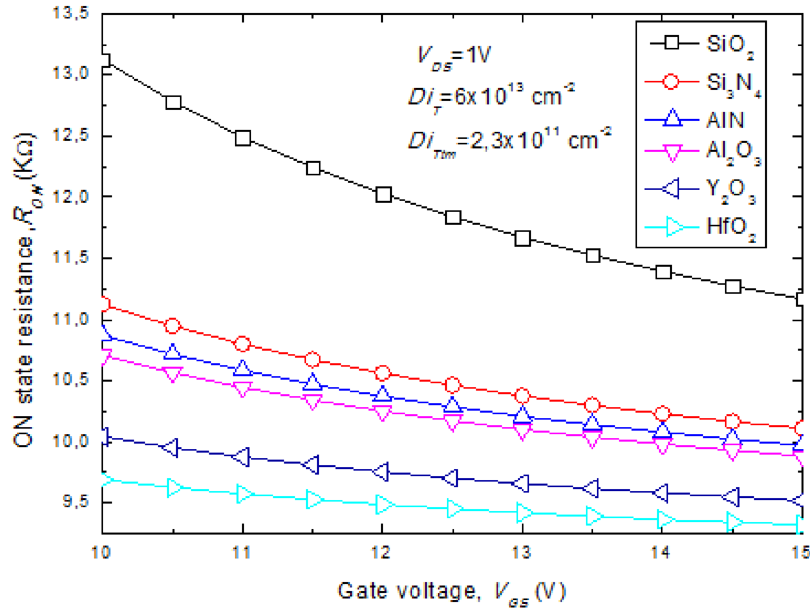


Figure. 8. On-state resistance comparison for $V_{DS} = 1$ V.

The R_{ON} values decrease with increasing V_{GS} because the trap screening effects are enhanced by the increase of free carriers in the accumulation region. However, the R_{ON} dependence on V_{GS} tends to become weaker for high-k dielectrics. This result is a consequence of the increased inversion charge determined by the high permittivity that enhances the conductivity in the channel region. For example, in the case of HfO_2 the R_{ON} mean value results close to 145 kΩ×μm^2. This value increases to about 450 kΩ×μm^2 for $T = 500$ K. In fact, an increased temperature increasingly limits the device current component in the channel region as well as in the drift region [51]. For comparison purposes, we can cite the R_{ON} datasheet value of a commercial Si-based MOSFET (Infineon IPB072N15N3 [61]) dimensioned for 150V which is equal to 216 kΩ×μm^2 for $V_{GS} = 10$ V at $T = 300$ K.

Finally, it is worthwhile noting that, thanks to the effective material permittivity, HfO_2 exhibits the lowest oxide electric field which results in the limit of 60 V/μm for a wide range

of drain voltages. As well known a low oxide electric field decreases the defect density distribution minimizing the induced stress in the gate region.

Figure 9 depicts the oxide electric field variation as a function of the drain voltage for the different gate dielectrics considered in this work.

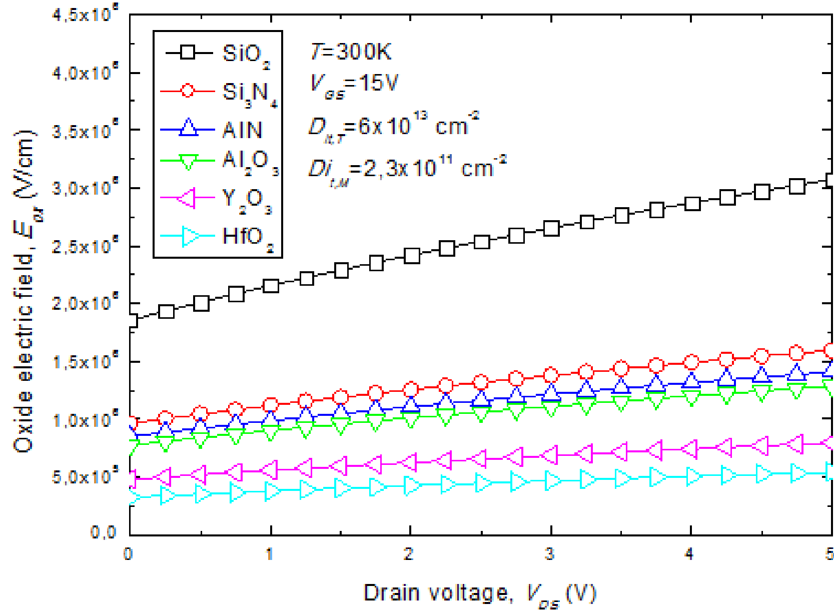


Figure. 9. Comparison of electric fields in the dielectric materials.

It is obvious from Figure. 9 that SiO_2 has a much higher electric field when compared with other dielectrics whereas HfO_2 has the lowest electric field at any drain voltage. Low electric field decreases the electric field stress via minimizing the defect density accumulation during the device operation.

5.2. Analysis of trap effects for different oxide/4H-SiC interfaces

This section is focused on the investigation of the effect of traps on the oxide/4H-SiC interface with an emphasis on the μ_{ch} degradation and V_{th} instability. Firstly, starting from the trap density reference value of 2.3×10^{11} cm^2eV^{-1} for the mid-gap states [30], the band tail trap density is ranged from 10^{12} $cm^{-2}eV^{-1}$ to 10^{14} $cm^{-2}eV^{-1}$ [52,53]. The corresponding variations

of the μ_{ch} and V_{th} behaviors for a device with different gate dielectrics are shown in Figure 10.

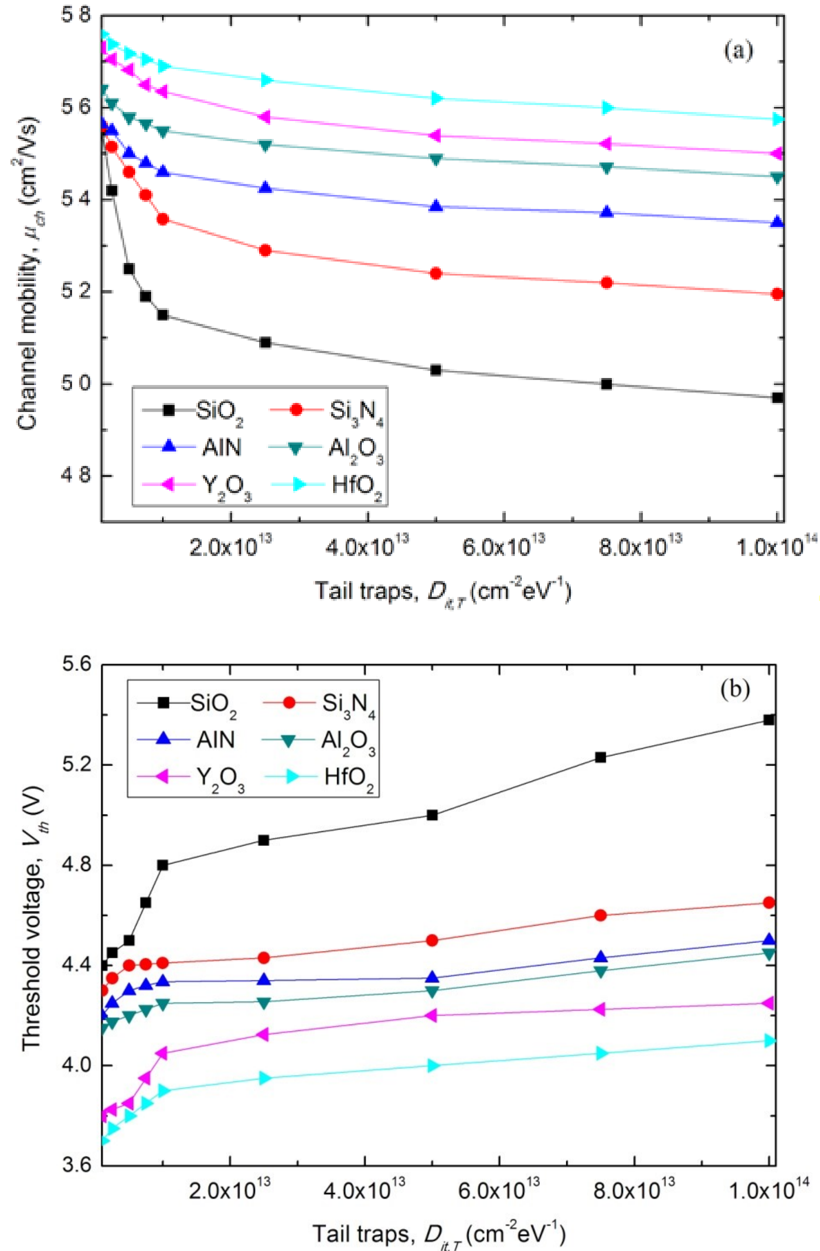


Figure. 10. Tail traps effect on (a) μ_{ch} and (b) V_{th}.

From Figure 10 (a) we can see that higher values of the carrier mobility can be obtained for high-k dielectrics. Also, the μ_{ch} behaviors appear less affected by an increasing tail trap density. In particular, for HfO_2, we calculate a μ_{ch} mean value of 57 cm^2/Vs in the channel region next to the oxide interface. This result is a further effect of a high permittivity gate oxide which assuring a higher charge concentration in the inversion layer increases the device immunity

against the effects of acceptor-like traps for $V_{GS} > V_{th}$. In other words, the effect of acceptor-like traps in excluding electrons from conduction tends to become less evident. From Figure10 (b), the V_{th} curves tend to increase as the tail traps increase. In fact, the increasing number of filled traps increases Coulomb scattering phenomena of free carriers determining a positive shift of V_{th}. Once again, we can highlight an increased immunity against the interfacial traps when using a gate oxide with a higher permittivity than SiO_2. In particular, ΔV_{th} is almost limited to 0.2 eV for a wide range of the term $D_{it,T}$. These V_{th} behaviors are also confirmed by analyzing the deep-level traps effects. In particular, in an additional set of simulations, we have fixed $D_{it,T} = 10^{13}$ $cm^{-2}eV^{-1}$ and we have varied the $D_{it,M}$ term up to a peak density of 10^{12} cm^{-2} eV^{-1} [53]. As expected, the lower ΔV_{th} values have been calculated for the higher permittivity dielectrics. However, it is noticeable that the deep-level traps have a lesser influence in determining the shift of V_{th} due to their position in the mid-gap.

5.3. HfO_2 dielectric stack with an ultra-thin interfacial layer

An improved oxide/4H-SiC interface exhibits low interfacial traps, decreased fringing capacitive effects and a band engineering opportunity. Finally, by investigating the role of the oxide/4H-SiC interfacial traps, we have used an oxide fixed trap density (N_{fix}) located near to the interface in the simulations. In fact, oxide fixed traps are unavoidable defect centres firmly reliant on the 4H-SiC oxidation process. The I_D-V_{GS} characteristics of an HfO_2/4H-SiC MOSFET for different values of N_{fix} are shown in Figure 11.

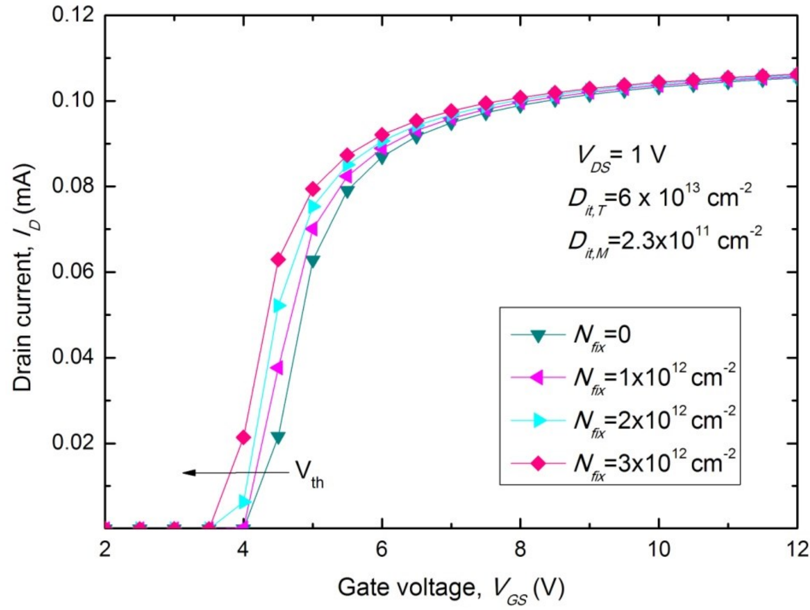


Figure. 11. Oxide fixed traps effect on the $I_D - V_{GS}$ curves of an HfO_2/4H-SiC MOSFET

The assumed range of N_{fix} is consistent with literature [52]. These traps became scattering centres that influence the effective carrier mobility in the channel region [54]. In addition, by acting as positive charges, they determine a band banding at the 4H-SiC interface that induces a lower threshold voltage in the proposed p-type MOSFET [55,56].

The HfO_2 thickness is a key parameter in determining the 4H-SiC MOSFET electrical behaviors. Figure 12 depicts the transfer characteristics variation as a function of the HfO_2 thickness.

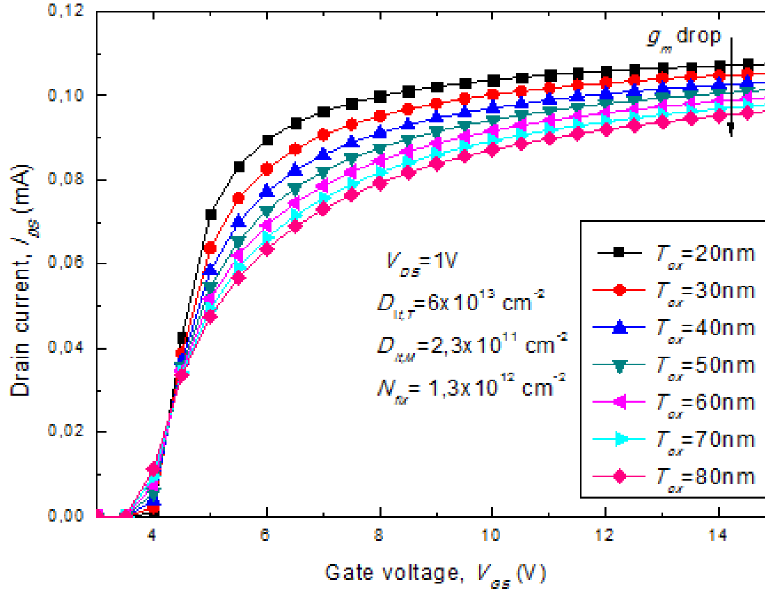


Figure. 12. MOSFET $I_{DS} - V_{GS}$ curves for different values of the HfO_2 thickness.

By varying T_{OX} from 20 nm to 80 nm, V_{th} decreases from 3.75 V to 3.4 V. Also, the transconductance decrease when increasing T_{OX} is attributed to the carrier mobility lessens which is affected by the high fixed traps density in the oxide.

Although the developed analysis always showed the best performance joined to the use of HfO_2, we have already introduced the need to insert a thin interfacial layer with a large band offset in a gate-stacked structure to limit the MOSFET leakage current. In more detail, we have simulated two alternative gate stacked structures involving either SiO_2 or Al_2O_3 with the use of HfO_2. From the simulations, the use of a 2-nm-thick interfacial film in a 20-nm-thick gate stacked oxide preserves the device main figures of merit while limiting the gate leakage current as shown in Figure 13.

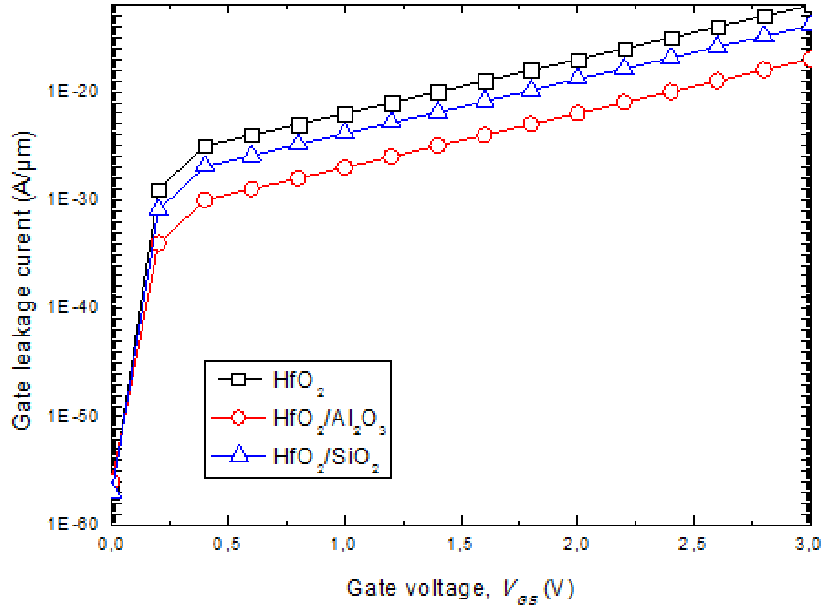


Figure.13. Gate leakage current comparisons.

The improvement in HfO_2/SiO_2 and HfO_2/A12O$_3$ stack combinations is due to the lower amount of conduction band discontinuity variation between the dielectric and 4H-SiC, which cause a noticeable difference in the conduction band offset. However Al_2O_3 (k = 9.3) as interfacial layer shows a decreased electric field in the oxide compared to SiO_2 and high current capabilities in terms of V_{th}, μ_{ch}, and R_{ON} as summarized in Table 5.

Table 5 MOSFET parameters comparison for different gate structures (T=300 K).

	HfO_2	HfO_2/SiO_2	HfO_2/Al_2O_3
Blocking voltage, V_{BL} (V)	150V	150V	150V
Oxide thickness, t_{ox} (nm)	20	20	20
Threshold voltage, V_{th} (V)	3.9	3.95	3.9
Gate to source voltage, V_{GS} (V)	15	15	15
Channel mobility, μ_{ch} (cm^2/Vs)	57	54	58
On State resistance, R_{ON} (kΩ×µm^2)	145	154	148
Transconductance, g_m (A/µm)	9.5	8.85	9.35
Subthreshold swing, SS (mV/dec)	380	405	390

As we can see, the HfO_2/Al_2O_3 structure is a better candidate to overcome the tradeoff between the leakage current and the device on-state operation mode characteristics.

Finally, Table 6 reports the state of the art in term of R_{ON} for different low-breakdown MOSFETs taken from literature including commercial and laboratory 4H-SiC devices [57-61]. Here, the notations DI and SJ stand for dual-implanted and superjunction MOSFETs, respectively.

Table 6 R_{ON} state-of-the-art

MOSFET	BV_{DS} (V)	R_{ON} (kΩ×μm^2)	
DI-SiO_2	100V	67	[57]
SJ-SiO_2	225V	140	[58]
SJ-SiO_2	200V	450	[59]
SJ-SiO_2	220V	150	[60]
DI-SiO_2	150V	216	[61]
DI-HfO_2/Al_2O_3	150V	148	This work

6. Conclusions

The design of a low power MOSEFT dimensioned to be used for example in DC–DC converters for solar power optimizers require high performance, good return on investments, and a long life cycle under any environmental conditions. In principle, all these constraints could be addressed by deploying the fast and rugged SiC technology. For this purpose, in this paper the gate dielectric reliability of a 4H-SiC-based MOSFET against temperature and trapping effects has been predicted via an accurate simulation analysis. An objective assessment of temperature and carrier-trapping effects has been carried out to investigate the electrical parameters variations for different gate dielectrics (i.e., SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2). A gate oxide with high relative permittivity improves significantly the device performance. HfO_2 shows the best immunity against interfacial traps and also good threshold voltage stability. Nevertheless, an excessive gate leakage current has been calculated. This drawback can be overcome preserving the MOSFET electrical characteristics by introducing a thin interfacial layer with a large band offset (e.g. Al_2O_3 or SiO_2) in a gate-stacked structure. The proposed

devices appear particularly well suited to boost up the manufacture of high-performance power modules for PV applications.

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