Numerical simulation study of a low breakdown voltage 4H-SiC MOSFET for photovoltaic module-level applications

F. G. Della Corte, G. De Martino, F. Pezzimenti, G. Adinolfi, and G. Graditi

Abstract— Silicon carbide (SiC) power MOSFETs are available only for high power and medium to high voltage applications, generally above 600 V, because for lower blocking voltages they comparatively provide lower advantages in terms of efficiency. There are applications, however, for which ruggedness and reliability are as important as efficiency, such as power optimizers for photovoltaic modules, which fall within the low power, low voltage category of DC-DC converters. These circuits, which maximize the energy produced by each single photovoltaic module, operate in continuously changing and stressing conditions yet having to assure high performances in terms of efficiency as well as of temperature insensitivity and long-term reliability.

The aim of this study is to predict the basic characteristics of a 4H-SiC MOSFET tailored for this kind of applications and therefore characterized by a breakdown voltage BV_{DS} of 150 V and currents of the order of 10 A. The study, based on numerical simulations, shows that, beside the expected higher ruggedness, the static characteristics would be comparable to those of silicon MOSFETs rated for a comparable BV_{DS}, with an R_{ON} in the order of 100 kΩ×μm², while advantages would results in terms of dynamic characteristics, and in particular in terms of switching times.

Index Terms— 4H-SiC MOSFET; power device; DC-DC converters; numerical simulations.

I. INTRODUCTION

Nowadays trend in photovoltaic (PV) consist in the integration of modules with an on-board electronic circuit. It is named, Smart Maximum Power Point Tracking (SMPPT) and it is a DC-DC converter, generally rated for voltages and currents respectively below 100 V and 10 A, providing the best match between the *I-V* characteristics of a single PV module and the downstream electronics [1]-[4]. As good quality solar modules are generally designed to remain fully functional for 25 years in all operating conditions, the on-board electronics is expected to perform at least the same life expectations. Reaching this goal is not trivial, since SMPPT converters operate in stressing and continuously changing conditions, moreover relaying on basic measures for their thermal control. The choice of suitable SMPPT topology and components is therefore a crucial task for designers [5]-[8]. In particular, the power switching devices, generally MOSFETs, must be highly efficient and rugged to meet the design targets.

MOSFETs made in silicon carbide (SiC), a semiconductor with excellent physical properties such as a high critical electric field E_C, mechanical strength, and high thermal conductivity [9], have gained wide popularity in high power electronics, also for their reliability. In recent years, they have been widely used in DC-DC converters developed for different application fields [10]-[15]. Commercial SiC MOSFETs are currently fabricated with blocking voltages BV_{DS} in the range from 600 to 1700 V [16]-[18]. They provide notably good performances for which it is worth paying more, at least compared to those of their less expensive silicon counterparts.

On the other hand, for lower BV_{DS} devices, SiC loses in part its advantages. For example, in a semiconductor *p-i-n* structure with a given doping of the *i*-layer, the breakdown voltage basically scales with E_C^2 [19], and therefore the lower the desired breakdown voltage, the weaker its dependence on E_C. This means that in low voltage devices, only a little improvement in the blocking capabilities results from use of SiC instead of Si. Therefore, as the higher blocking capabilities of SiC are usually traded off for thinner *i*-layers and consequent lower on-state resistance, it follows in turn that moderate improvements can be expected for the on-state characteristics of low voltage SiC devices. In addition, the latter present costs that, at least to date, make them not convenient to circuit designers and producers.

SiC devices, however, confer robustness on circuits, also in stressing environments. This feature might be worth exploiting also in lower voltage applications, like in SMPPT, for which efficiency, miniaturization, and temperature control represent critical targets.

This work is therefore addressed at predicting the characteristics of 4H-SiC MOSFETs designed for PV power switching converters, for which preliminary results on static characteristics were previously presented [20]. In particular, the design specifications refer to a transistor with a breakdown (or blocking) voltage, BV_{DS}, of 150 V. The attention is focused on the on-state resistance (R_{ON}), the switch-on gate charge

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(Q_g), and the switching times to verify their fitness to the specific application. The device was studied by a TCAD 2D physical simulator.

II. DEVICE STRUCTURE

The schematic cross-section of the 4H-SiC MOSFET elementary half-cell considered in this study is shown in Fig. 1. Although simplified for simulation purposes, the proposed geometry is in principle compatible with a manufacturing process based on doping by ion implantation [21]-[23].
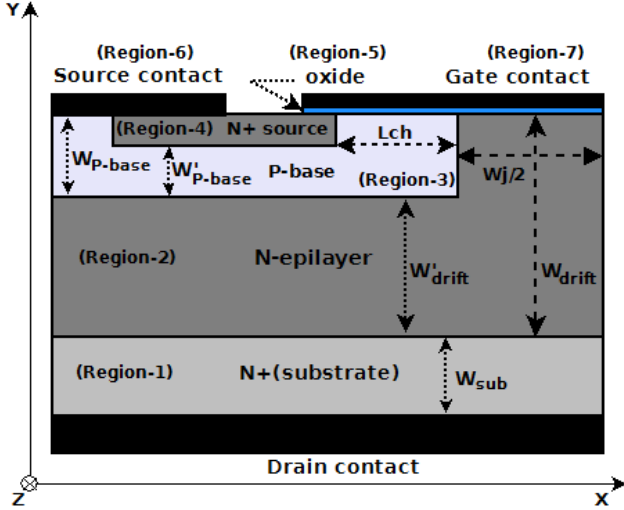

Fig. 1. Schematic cross-sectional view of the MOSFET half-cell. The drawing is not in scale.

Seven regions can be identified in the device structure. Region-1 is a heavily nitrogen-doped N+-region and constitutes the drain of the MOSFET. It coincides with the 4H-SiC substrate on which the drift region of the final device is grown by epitaxy. Substrates are generally produced with a thickness of 350 μm. However, before realizing the bottom contact, they are thinned down to 100-150 μm to cut the resistance and improve heat exchange. We therefore considered a W_{sub} thickness of 100 μm.

Region-2 is the nitrogen-doped drift epitaxial N-layer, with thickness W_{drift}. Doping concentrations for drift regions (N_{epi}) in SiC MOSFETs are generally in the range 5×10^{15} to 10^{16} cm^{-3} [21], [23], [24]. By adapting to our P-base/N-epilayer/N+-substrate structure the well-known formula valid for abrupt junction p-i-n devices that show breakdown in punch-through conditions [19]:

$$BV_{DS} = E_C W'_{drift} - \frac{qN_{epi}(W'_{drift})^2}{2\varepsilon_s} \qquad (1)$$

where E_C is the critical electric field, q is the electron charge, and ε_s is the semiconductor dielectric constant, it follows that the lower is the desired breakdown voltage BV_{DS}, the higher can be the drift layer doping N_{epi}, with consequent advantages in terms of low on-state resistance. Given the specified voltage ratings, the N_{epi} is set to 10^{16} cm^{-3} for the simulations.

Region-3 is the aluminum-doped (10^{17} cm^{-3}) p-base; this region contains the actual MOS structure and the device channel, which is set to $L_{ch} = 1$ μm, just below the gate oxide.

Region-4 is the phosphorous-doped (10^{18} cm^{-3}) source region. The insulating Region-5 of the MOS structure is made of silicon oxide. Region-6 forms the source contact, shorting moreover the source and base regions to prevent the switch-on of the parasitic *substrate(n+)-epilayer(n)-base(p)–source(n+)* bipolar junction transistor. Region-7 is the gate contact.

The geometrical parameters and doping concentrations of the different MOSFET regions are summarized in Table I. The half-cell of Fig. 1 has a length (x-direction) of 6.5 μm, while the width (z-direction) is 1.0 μm by default. The drain contact area is therefore 6.5 μm^2, the source contact area is 1.8 μm^2 and the gate contact area is 3.4 μm^2. The distance between the p-base regions, W_j, was set to 5.0μm, while the W_{drift} thickness (y-direction) of 1.8 μm was chosen to meet the required MOSFET specification in terms of BV_{DS}. In particular, starting from a thickness of 10 μm, which confers to the device a BV_{DS} of about 1 kV, W_{drift} was reduced to get a BV_{DS} of 150 V, as will be described later.

TABLE I
MOSFET STRUCTURE

Silicon oxide thickness (μm)	0.08
Source thickness (μm)	0.50
Channel length, L_{ch} (μm)	1.00
Base junction depth, W_{P-base} (μm)	1.30
Interspace W'_{P-base} (μm)	1.00
Distance between the base regions, W_j (μm)	5.00
Epilayer junction depth, W_{drift} (μm)	1.80 -10.0
Base-to-substrate distance, W'_{drift} (μm)	0.50
Substrate thickness, W_{sub} (μm)	100.0
Device footprint area (μm^2)	6.50
N+-source doping (cm^{-3})	10^{18}
P-base doping (cm^{-3})	10^{17}
N-epilayer doping (cm^{-3})	10^{16}
N+-substrate doping (cm^{-3})	10^{19}

III. PHYSICAL MODELS AND PARAMETERS

Using a 2D TCAD simulator [25], the device structure was modeled and finely meshed wherever appropriate and in particular around the p-n junctions and within the channel region, just below the 4H-SiC/SiO$_2$ interface, where a mesh spacing down to 25 nm was used.

The key physical models used in the simulations include the incomplete doping ionization, apparent bandgap narrowing, impact ionization, Shockley-Read-Hall and Auger recombination processes; carrier lifetime and mobility are function of both doping concentration and temperature.

In more detail, the temperature dependence of the 4H-SiC bandgap is in the form [26]:

$$E_g(T) = E_{g0} - \frac{\alpha T^2}{\beta + T} \qquad (2)$$

where E_{g0} is the bandgap energy at 0 K, $\alpha = 3.3 \times 10^{-4}$ eV/K, and $\beta = 0$ are specific material parameters.

Due to the wide bandgap of 4H-SiC, not all doping atoms can be assumed as fully ionized. Using the Fermi–Dirac statistics, the carrier concentrations N_a^- and N_d^+ (*i.e.*, the number of ionized acceptors and donors, respectively) can be

calculated with the following expression [27]:

$$N_{a,d}^{-+} = N_{a,d} \left(\frac{-1 + \sqrt{1 + 4 g_{a,d} \frac{N_{a,d}}{N_{V,C}(T)} e^{\frac{\Delta E_{a,d}}{kT}}}}{2 g_{a,d} \frac{N_{a,d}}{N_{V,C}(T)} e^{\frac{\Delta E_{a,d}}{kT}}} \right) \quad (3)$$

where N_a and N_d are the substitutional p-type and n-type doping concentrations, N_V and N_C are the hole and electron density of states varying with temperature, $g_a = 4$ and $g_d = 2$ are the degeneracy factors of the valence and conduction band, and $\Delta E_a = 200$ meV and $\Delta E_d = 100$ meV are the ionization energies for acceptor and donor impurities, respectively.

An apparent bandgap narrowing effect as a function of the ionized doping in the p-type and n-type regions is also included during simulations according to the Lindefelt's model of the band edge displacements [28]:

$$\Delta E_{ga,d} = A_{a,d} \left(\frac{N_{a,d}^{-+}}{10^{18}} \right)^{1/2} + B_{a,d} \left(\frac{N_{a,d}^{-+}}{10^{18}} \right)^{1/3} + C_{a,d} \left(\frac{N_{a,d}^{-+}}{10^{18}} \right)^{1/4}. \quad (4)$$

Here, $A_{a,d}$, $B_{a,d}$, and $C_{a,d}$ are specific 4H-SiC constants, reported in Table II [27].

TABLE II
APPARENT BANDGAP NARROWING MODEL COEFFICIENTS

$A_{a,d}$	1.54×10^{-3}, 1.17×10^{-2}
$B_{a,d}$	1.3×10^{-2}, 1.50×10^{-2}
$C_{a,d}$	1.57×10^{-2}, 1.90×10^{-2}

The electron and hole lifetimes, useful to define the Shockley–Read–Hall recombination rate, are modeled as functions of doping by means of the relation proposed in [29].

$$\tau_{n,p} = \frac{\tau_{0n,p}}{1 + \left(\frac{N}{N_{n,p}^{SRH}} \right)} \quad (5)$$

where N is the total impurity concentration for a given device region, $N_{n,p}^{SRH} = 5 \times 10^{16}$ cm^{-3} is a reference constant, and $\tau_{0n} = 500$ ns and $\tau_{0p} = 100$ ns are process-dependent parameters taken from [30]. As it will be confirmed by comparison with experimental data, the above assumptions provide reliable simulation results also without introducing an explicit yet reasonable state density ($D_{it} < 5 \times 10^{12}$ cm^2/eV [31]) at the SiO$_2$/SiC interface.

In order to model the 4H-SiC carrier mobilities, the Caughey-Thomas analytic model at $T = 300$ K, experimentally validated in [32], is used:

$$\mu_{n,p} = \mu_{0n,p}^{min} + \frac{\mu_{0n,p}^{max} - \mu_{0n,p}^{min}}{1 + \left(\frac{N}{N_{n,p}^{crit}} \right)^{\delta_{n,p}}}. \quad (6)$$

In the reported formula N is the local (total) concentration of the ionized impurities, $N_{n,p}^{crit}$ and $\delta_{n,p}$ are fitting parameters, and the μ_0 values reported in Table III are the fundamental model parameters at room temperature taken from [26], [32].

In addition, for high electric fields, the expected mobility reduction due to the carrier saturated drift velocity ($v_{sat} = 2 \times 10^7$ cm/s) is described by using

$$\mu_{n,p}(E) = \frac{\mu_{n,p}}{\left[1 + \left(E \frac{\mu_{n,p}}{v_{sat}} \right)^{\kappa_{n,p}} \right]^{\frac{1}{\kappa_{n,p}}}} \quad (7)$$

where E is the electric field in the direction of the current flow. Here, $k_n = 2$ and $k_p = 1$ can be assumed [25].

TABLE III
CARRIER MOBILITIES FOR THE CAUGHEY-THOMAS MODEL

$\mu_{0n,p}^{min}$	40.0 cm^2/V×s, 15.9 cm^2/V×s
$\mu_{0n,p}^{max}$	950 cm^2/V×s, 125 cm^2/V×s
$N_{n,p}^{crit}$	2×10^{17}, 1.76×10^{19}
$\delta_{n,p}$	0.76 , 0.34

Finally, the electron and hole impact ionization rates, $\alpha_{n,p}$, which are needful to predict in details the avalanche device breakdown voltage, are modelled through the following empirical expression [33]:

$$\alpha_{n,p} = a_{0n,p} \exp \left(-\frac{b_{0n,p}}{E} \right) \quad (8)$$

where $a_{0n} = 2.5 \times 10^5$ cm^{-1}, $a_{0p} = 3.25 \times 10^6$ cm^{-1}, $b_{0n} = 1.84 \times 10^7$ V/cm, and $b_{0p} = 1.71 \times 10^7$ V/cm are the carrier ionization coefficients measured in [34], [35].

Parameters details about the applied 4H-SiC simulation setup are reported in recent authors manuscripts [36]-[38]. Moreover, it is supported by experimental results in a wide range of currents and temperatures obtained on both Al implanted 4H-SiC p$^+$-i-n and Schottky diodes [39]-[41].

IV. RESULTS AND DISCUSSION

A. Blocking Voltage Characteristics

A first set of simulations was performed in order to assess the dependence of BV_{DS} on the epitaxial region thickness (region-2 in Fig. 1). With the device in the off-state ($V_G = 0$ V) and grounded source, V_{DS} was gradually raised up to the occurrence of a critical electric field $E_C = 1.9 \times 10^6$ V/cm somewhere along the border of the P-base/N-epilayer junction.

Under these bias conditions, no channel is formed under the gate at the surface of the P-base region, and the P-base/W-drift junction is reverse-biased to sustain the positive drain voltages. However, despite the short-circuiting of the N$^+$-source and P-base region, the drain leakage current, which remains below any practically detectable value ($J_D < 10^{-17}$ µA/µm^2) until E_C is under 1.9×10^6 V/cm, suddenly rises above 70 µA/µm^2 as soon

as the depletion layer in the P-base punches through the source.

The electric field and drain current behaviors are shown in Fig. 2 as a function of the drain voltage for two devices with different W_{drift} thicknesses, namely $W_{drift} = 5.0$ μm, and $W_{drift} = 1.8$ μm. In particular, the $W_{drift} = 1.8$ μm device was identified as the one meeting the specification of $BV_{DS} = 150$ V for the P-base and N-epilayer doping levels reported in Table I. Note that Eq. (1), valid for abrupt-asymmetrical junctions, predicts for these values the breakdown to start at about 100 V. However, it should be considered that the P-base/N-epilayer junction is weakly asymmetrical in this case (10^{17} cm^{-3} vs. 10^{16} cm^{-3} dopings), and therefore, the electric field in the off-state is in fact sustained by both sides of the junction, namely the N-epilayer (W'_{drift} thickness) and the P-base (W'_{P-base}), with consequent increase of the BV_{DS}.
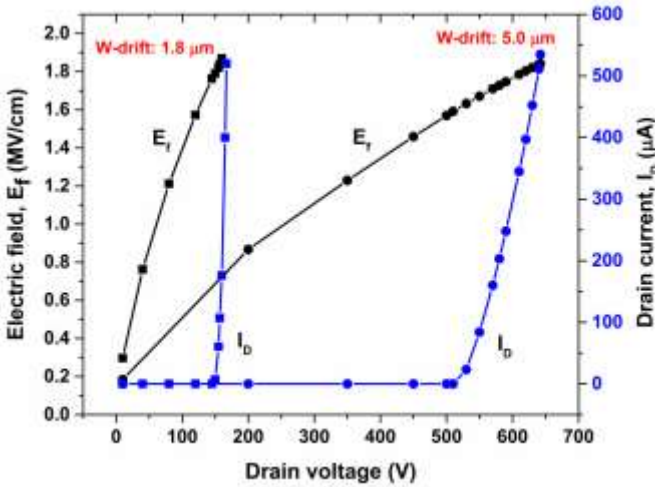

Fig. 2. Electric field (black curve) and drain current (blue curve) as a function of the drain bias for two devices with different W_{drift}. The reported electric field is the highest measured along the border of the P-base/N-epilayer junction (see Fig. 1).

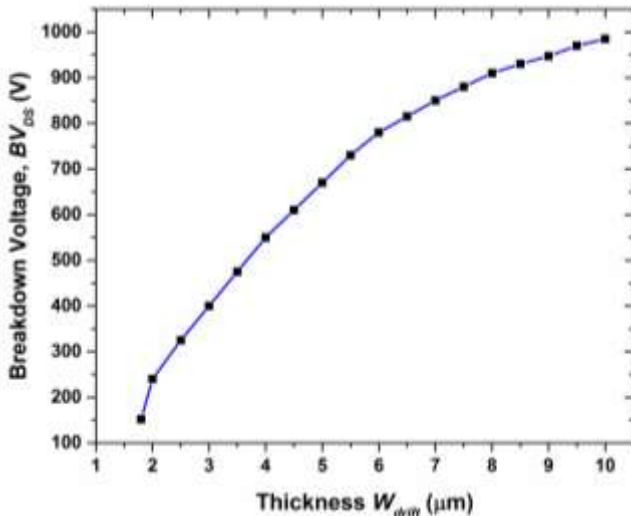A detailed analysis of the MOSFET BV_{DS} behavior vs. W_{drift} is illustrated in Fig. 3.

Fig. 3. MOSFET breakdown voltage as a function of W_{drift}.

B. On-State Analysis

The current density-voltage (J_D-V_{DS}) output characteristics of the $W_{drift} = 1.8$ μm device, nearby and within the triode region, are shown in Fig. 4 for V_{GS} from 7 to 20 V.

The existence of contact resistances was also considered for these simulations. In fact, assuming indicatively a specific contact resistance of 10^{-6} Ω×cm^2 both for P-type and N-type contacts [42], [43], it turns out that a 1 μm^2 footprint device, with contacts scaled as in Fig. 1, would show gate, source, and drain contact resistances respectively of R_G=176 Ω, R_S =325 Ω, and R_D =100 Ω.
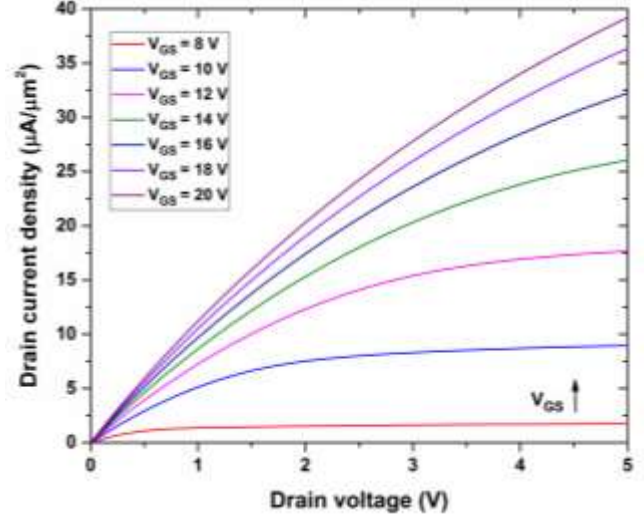

Fig. 4. Forward J_D-V_{DS} characteristics. The geometrical and electrical parameters of the device are those listed in Table I.

The device turns on for a V_{GS} of approximately 8 V, which we can assume to be its threshold voltage V_{th}. At this regime, the resistive path established for electrons flowing from the source contact to drain is characterized by an R_{ON} resistance determined by various terms, namely $R_{ON} = R_{n+} + R_{ch} + R_a + R_j + R_d + R_b$. Here, R_{n+} is the source resistance, R_{ch} is the channel resistance, R_a is the resistance of the accumulation region relative to the distance W_j /2 (see Fig. 1), R_j is the resistance of the depletion layer between the P-base and the N-epilayer region, R_d is the resistance of the drift region and R_b is the drain resistance. However, R_{n+} and R_b are generally negligible because they are localized in heavily doped regions. R_{ch} and R_a mainly depend on the gate bias level. Finally, R_j and R_d are determined by the geometry and doping level of the W-drift region.

Assuming an operating point in the triode region, for $V_{GS} = 16$ V and $V_{DS} = 1$ V the drain current density is close to 10 μA/μm^2, corresponding to an on-state resistance of 100 kΩ×μm^2. The R_{ON} values calculated for different drain-source voltages as a function of V_{GS} are plotted in Fig. 5.

The R_{ON} behavior vs. V_{GS} at V_{DS} = 1 V for different values of the half distance between the P-base regions W_j /2 (see Fig. 1), is shown in Fig. 6. As can be seen, W_j /2 = 2.5 μm represents a good tradeoff for gate drive voltages up to 16 V.

Finally, simulating the MOSFET J_D-V_{DS} characteristics for different values of the channel length (L_{ch} in Fig. 1) in the limit

1 ± 0.2 μm, the results showed that this parameter has a limited impact on the device on-state current capabilities. In full on-state, R_{ON} approximately decreases (increases) in fact by a factor of 5% if L_{ch} is set to 0.8 μm (1.2 μm).
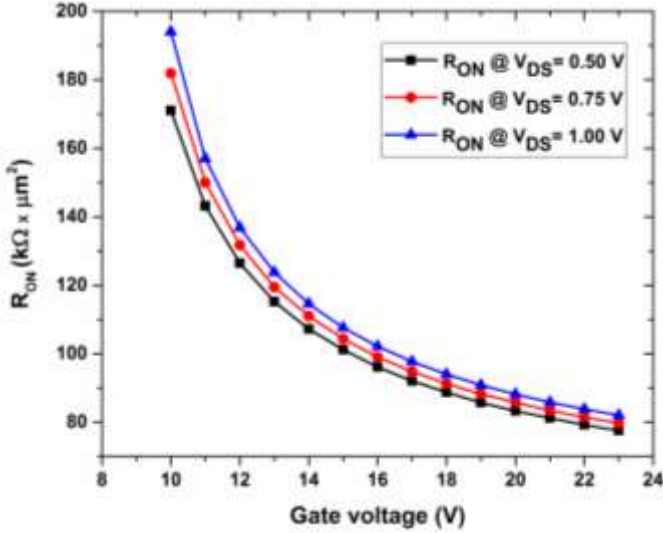

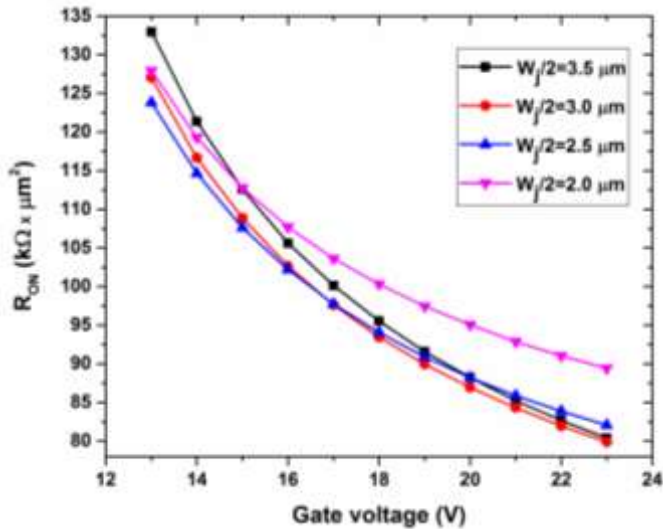Fig. 5. R_{ON} as a function of V_{GS} at different drain voltage levels.

Fig. 6. R_{ON} as a function of V_{GS} for different values of $W_j/2$ at $V_{DS} = 1$V.

It is worth noting that temperature effects were not considered in this study, which was, in fact, performed at room temperature. The introduction of temperature impact in simulations implies a careful tuning of temperature dependent models used to describe several key parameters, among which carrier mobility, dopant ionization, and intrinsic carrier concentration. However, we note that, in spite of a reduction of V_{th}, a temperature increase typically induces a higher R_{ON} in SiC MOSFET, mainly due to the effects, on drift region resistance, of electron mobility degradation [16]-[18]. For this reason, we expect this device to show a weaker temperature dependence of R_{ON}, due to its thinner drift layer.

C. Test of the simulation setup

The prediction capabilities of the simulation setup described above were tested by comparison with experimental data. In particular, simulations of a commercial 900 V SiC MOSFET [17] were performed, starting from the same device topology of Fig. 1. In order to circumvent the lack of information about geometry and doping levels, similarly to [44] we assumed an epilayer doping concentration of 3×10^{15} cm^{-3} and an epilayer thickness of 10 μm. These values place the breakdown voltage BV_{DS} above 900 V. The device footprint was measured, after decapsulation, to be 2.1 mm^2, from which we assumed an effective area, after reasonably excluding a 50-μm-wide ring for junction termination all around, of approximately 1.9 mm^2. The measured R_{ON} of the commercial device as a function of V_{DS}, for $V_{GS} = 15$ V, is shown in Fig. 7 together with that calculated by numerical simulations. Also in this case, a specific contact resistance of 10^{-6} Ω×cm^2 was assumed in the model. It can be seen that simulation results appear in good agreement with experimental data.
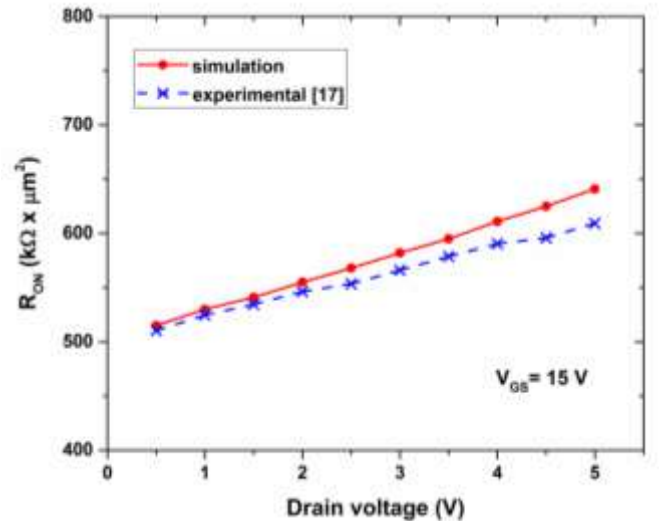

Fig. 7. Comparison between the R_{ON} of a commercial device and that calculated by numerical simulations as a function of V_{DS} for $V_{GS} = 15$ V.

D. Transient Analysis and Switching Times

In MOSFETs employed in high performance switching applications, *e.g.* SMPPT converters (higher than 98% efficiency required), the static power dissipation, due to R_{ON}, is at least as important as the dynamic power dissipation during turn-on and turn-off transients, the latter being governed, in turn, by the charge and discharge times of stray capacitances existing within the device. A common quality factor considered for a power MOSFET is therefore the gate charge ($Q_g = \int i_g \times dt$) that must be transferred to (removed from) the gate capacitor in order to fully turn-on (turn-off) the switch. The gate capacitance C_g is mainly the sum of the gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}). The capacitance C_g, and therefore Q_g, can be reduced by lowering the doping of the drift region (N_{epi}), but this has a negative impact on R_{ON}, so the best C_g value comes from a tradeoff between these parameters. For this reason, a frequently used figure of merit (FOM) for power MOSFETs is the product between the on-state resistance and the gate charge ($R_{ON} \times Q_g$)

at a given BV_{DS} [45], which should be as low as possible. Transient simulations were therefore performed to estimate these quality parameters.

When transient simulation is performed, the carrier continuity equations are integrated in the time domain. The reference circuit is shown in Fig. 8. It includes the device under study, with the characteristics of Fig. 4, and a lumped element for the load. The power source voltage, V_{DD}, and the load resistor, R_L, were chosen to have the MOSFET operate in deep triode region at $V_{DS} = 1$ V, $J_D \approx 10$ μA/μm² (see Fig. 4) when a gate pulse $V_{GS} = 16$ V is applied. It is worth noting that the contact resistances assumed in Section IV-B for gate, drain and source, were also considered during the transient analysis. Simulations were run with and without a lumped gate driving resistance $R_{G,ext}$, to measure both the theoretical ($R_{G,ext} = 0$) and realistic ($R_{G,ext} > 0$) characteristic switching times of the device. This is the simplest circuit through which the device basic switching parameters can be calculated. The device, which has $W_j/2 = 2.5$ μm was driven by voltage pulses with several amplitudes (from 10 to 23 V, in steps of 1 V), with switching times of 100 ps.
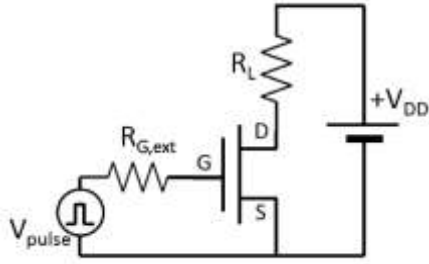

Fig. 8. Circuit for the MOSFET transient analysis: the MOSFET has a 1 μm² footprint, $R_L = 7.5$ MΩ, $R_{G,ext} = 0$ (or $R_{G,ext} = 200$ kΩ), and $V_{DD} = 75$ V.

For a gate control pulse of 16 V applied at the time $t = 5$ ns, the evolution of the drain node voltage, from cut-off ($V_{DS} = 75$ V) to full power ($V_{DS} \approx 1$ V), is shown in Fig. 9. Here, the drain current transient curve is also reported.
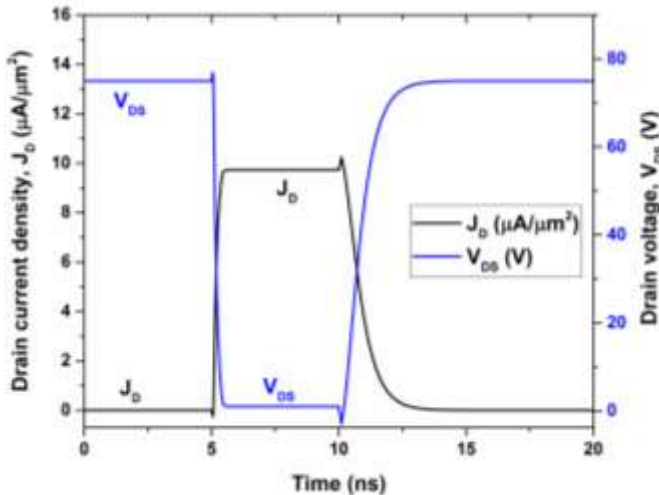

Fig. 9. MOSFET transient analysis (off-on-off) at room temperature ($R_{G,ext} = 0$). The gate control pulse is applied at $t = 5$ ns and it switches from zero to 16 V in 100 ps. $V_{DD} = 75$ V.

The calculated 90%-10% fall and 10%-90% rise times (*i.e.*, t_f and t_r, respectively) of V_{DS} and J_D, for $R_{G,ext} = 0$ are listed in Table IV. The same Table also reports, in parenthesis, the switching times calculated for $R_{G,ext} = 200$ kΩ, corresponding to a gate drive resistance of 2 Ω if the device were upscaled to handle an I_D of 10 A.

TABLE IV
MOSFET SWITCHING TIMES

	t_f (ns)	t_r (ns)
V_{DS}	0.27 (0.54)	1.45 (2.1)
J_D	1.48 (2.1)	0.25 (0.49)

The short switching times, notably smaller than those of state-of-the-art commercial Si-MOSFETs of the same BV_{DS} class, imply advantages in terms of containment of dynamic power dissipation.

The device performances are compared in Table V to those of state-of-the art Si-MOSFET [46]-[52], including commercial [48], [49] and laboratory [50]-[52] super-junction (SJ) devices.

TABLE V
STATIC AND DYNAMIC CHARACTERISTICS OF STATE-OF-THE-ART MOSFETs

	BV_{DS} (V)	t_f (ns)	t_r (ns)	R_{ON} (Ω×μm²)	Notes	
					Static	Dynamic
This study	150	0.27 (0.54)	1.45 (2.1)	8.7	A = 1 mm² $V_{GS} = 20$ V $I_D = 10$ A	$V_{DD} = 75$ V $V_{GS} = 16$ V $I_D = 10$ A $R_{G,ext} = 0$ ($R_{G,ext} = 2$ Ω)
[46]	100	3.9	4.6	6.7	A = 4.5 mm² $V_{GS} = 10$ V $I_D = 20$ A	$V_{DD} = 50$ V $V_{GS} = 10$ V $I_D = 10$ A $R_{G,ext} = 1.6$ Ω
[47]	150	14	35	21.6	A = 30 mm² $V_{GS} = 10$ V $I_D = 100$ A	$V_{DD} = 75$ V $V_{GS} = 10$ V $I_D = 100$ A $R_{G,ext} = 1.6$ Ω
[48] (SJ)	600	4.5	8	80 [49]	$V_{GS} = 10$ V $I_D = 9.7$ A	$V_{DD} = 400$ V $V_{GS} = 13$ V $I_D = 9.7$ A $R_{G,ext} = 5.3$ Ω
[50] (SJ)	225	-	-	14	$V_{GS} = 14$ V $J_D = 2$ A/mm²	-
[51] (SJ)	200	340	180	45	$V_{GS} = 10$ V $I_D = 20$ A	$V_{DD} = 120$ V $V_{GS} = 10$ V $I_D = 7$ A $R_{G,ext} = 4.7$ Ω
[52] (SJ)	220	-	-	15	$V_{GS} = 10$ V	-

In detail, the device reported in [46], rated for $BV_{DS} = 100$ V shows a slightly smaller specific R_{ON} and notably higher switching times, while the MOSFET considered in [47], rated for 150 V, has a considerably higher specific R_{ON}. Commercially available SJ devices, which are always rated for $BV_{DS} > 500$ V [48], [49], also behave slightly poorer.

By integrating the gate current plot over the switching interval, the gate charge Q_g as a function of V_{GS} was extracted

as shown in Fig. 10, which reports also R_{ON} in the considered range for V_{GS}. The reported graph permits to calculate the $R_{ON} \times Q_g$ FOM. It results weakly dependent on the gate bias level, with a mean value of $0.48 \times 10^{-9} \, \Omega \times C$, which is smaller than that of other SiC MOSFETs designed for higher BV_{DS} [53] and comparable to that of [45] ($0.4 \times 10^{-9} \, \Omega \times C$).
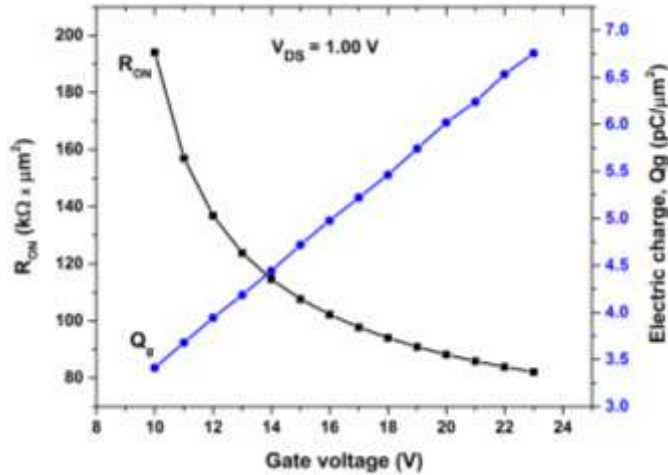

Fig. 10. R_{ON} and Q_g behaviors as a function of V_{GS}. $W_j / 2 = 2.5$ μm. $W_{drift} = 1.8$ μm.

V. Conclusion

The requirements for power optimizers used in PV modules, generally rated for a maximum voltage of 100 V, include high efficiency, for a fast return of investments, and 20 years or longer life span, under any weather conditions. Both these requirements could be addressed in principle by deploying the fast and rugged SiC-based switches, if only they were available for this voltage range.

In this paper, the performances of a 4H-SiC MOSFET with short drift layer, suiting 100-V-class switching converters, have been predicted by numerical simulations.

The device features a 1.8-μm-thick epilayer, with a breakdown voltage of 150 V and an on-state resistance in the order of 0.9 mΩ×cm², which is comparable to that of commercial Si MOSFET rated for the same voltage range.

The switching analysis, performed considering a resistive load at a drain current density close to 10 μA/μm², shows that the rise and fall times for V_{DS} are 1.45 ns and 0.27 ns, respectively. A small $R_{ON} \times Q_g$ FOM of 0.48×10^{-9} Ω×C was also calculated in the best operating conditions of $V_{GS} = 16$ V, $V_{DS} = 1$ V, and $J_D = 10$ μA/μm².

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